Persistent modification of magnetotransport properties in $LaAlO_3/SrTiO_3$ by gate-induced modification of structural domains

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We investigate the influence of large electric fields on the transport properties of nanostructures patterned into the electron gas at the interface between $LaAlO_3$ and $SrTiO_3$ (100). In these nanostructures, the transport is largely dominated by domain walls between structural domains in the $SrTiO_3$ appearing below a structural phase transition temperature. We find that both positive and negative gate voltages applied in a side-gate configuration can induce persistent changes in the sample that are only reversed by warming through the phase transition. These changes include a resistance increase and a change in magnetoresistance in magnitude and sign. Furthermore, a resistance anomaly during warm-up that has been observed in the past can be further increased by briefly applying a side-gate voltage. These effects are typically observed in nanostructures below a certain size limit. The electric fields also increase this size limit from a few-hundred nm to more than 1 μm. All these observations can be consistently explained by a field-induced removal of specific domain-wall types accompanied by an increasing domain size and a reduced number of domain walls in the structures. The results not only show that under certain conditions domain walls can dominate the transport properties even of micron-sized structures, but they also provide an additional tuning knob to induce nonvolatile changes in the transport properties of $LaAlO_3/SrTiO_3$ interfaces at low temperatures.

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For quite some time, it has been known that the conductivity of the interface between $LaAlO_3$ and $SrTiO_3$ (LAO/STO) is not homogeneous [1–3]. Current rather flows through domain walls that form as a result of several structural phase transitions in STO that appear during cool-down at various temperatures. These phase transitions are from cubic to tetragonal at 105 K and tetragonal to orthorhombic at 65 K, and a possible transition to a rhombohedral phase well below 30 K [4,5]. During these ferroelastic phase transitions, three types of domains are created that differ only in the orientations of their longer lattice vector that for each of them is oriented along one of the former cubic axes. For energy reasons, only three different types of domain walls can exist that separate the different domain types. One kind of domain wall is aligned in the plane at either 45° or 135° with respect to [010], but extends perpendicularly into the substrate. The other two types are tilted with respect to the surface normal at an angle of 45°, but their orientation in the plane with respect to [010] is either 0° or 90°, respectively [6]. Ma *et al.* [7] have shown that these domain walls are highly conducting, indicating high carrier concentrations, while the surrounding can be completely insulating, indicating carrier depletion. This was also supported by measurements from Minhas *et al.* [8] that can be explained by carrier accumulation at the domain walls and at least part of the area in between completely depleted. A recent study by Persky *et al.* [9] also confirms the inhomogeneity in the conductivity landscape with insulating areas near the metal-insulator transition. They also describe the possibility that conducting patches exist within the insulating area or that branching of the current path can lead to dead ends reaching in the insulating area. Due to the lack of current flow, however, they were not able to prove their existence by scanning superconducting quantum interference device (SQUID) microscopy. It should, however, be noted that dead-end branches might have been visible in the experiments by Ma *et al.* [7] who were using a different imaging method.

The presence of these conducting domain walls was first shown by scanning SQUID microscopy [1] and since then has been demonstrated in multiple ways [2,3,6]. Several studies have revealed that the domain patterns also affect other STO-based systems as well as bulk STO [10–14]. Especially in nanostructures, the interplay of domain walls and transport properties was also shown, for example, by a huge resistance anomaly around $T = 80$ K [8] or by anisotropic and statistical

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magnetotransport properties [15]. The fact that the resistance anomaly appears between 60 and 80 K indicates that the relevant phase transition that breaks the conducting domain-wall path is the one at 65 K. The loss of polarization of the domain walls at approx. 80 K can then lead to a redistribution of the carriers and to a recovery of large area conductivity [16]. The changes in magnetoresistance (MR), however, only vanish after warming through $T = 105$ K.

In the past, interesting effects of electrostatic gating on domain walls in LAO/STO have also been demonstrated. Early experiments indicate an enhancement of domain-wall mobility by electric fields [6]. Above a certain threshold field, ferroelectricity is induced in the domain walls [7], which is persistent even after switching off the gate voltage. Ma *et al.* [7] also observed that the two dimensional electron gas (2DEG) surrounding the ferroelectric domain walls is depleted within a certain range, similar to a Schottky barrier. Further experiments show that the application of a positive gate voltage enhances the trapping of charge carriers, which in turn results in an irreversible change in sheet resistance [17–19]. Finally, it was demonstrated that by applying a large gate voltage, an irreversible preferential selection of particular domains and domain walls can be achieved [6,20,21]. The latter is explained as follows: The domain formation is driven by an antiferrodistortive (AFD) lattice mode, with neighboring TiO_6 octahedra rotating in antiphase along the [001] axis [22,23]. The motion of domains in an electric field arises from the low-temperature dielectric anisotropy between in-plane and out-of-plane domains in STO [20] that becomes less significant at higher temperatures close to the phase transition. Casals *et al.* [20] show that the polarizability is significantly larger perpendicular to the antiferrodistortive (AFD) tilt axis, suggesting that in-plane domains are energetically favored under an applied electric field. As a result, an electric field leads to an expansion of the in-plane domains and, above a threshold field, a complete removal of the domains with out-of-plane long axis takes place.

In terms of gating, we can distinguish four different types of geometries. Back gating of large area structures requires voltages of 100 V or more in order to achieve sizable electric fields at the LAO/STO interface [24–27]. Back gating of micro- and nanostructures concentrates the field lines at the structure increasing the local field with decreasing structure size [28]. As a result, the gate action is considerably enhanced in nanostructures, thus reducing the back-gate voltage V_{BG} that is necessary to observe similar effects compared to gating of large area LAO/STO. Top-gate geometries allow for large electric fields at low voltages that are less dependent on structure size than on the thickness of the gate dielectric [29,30]. However, in the top-gate geometry, the voltage is applied between the gate and the electron gas, creating a two-plate capacitor. As a consequence, the electric field is between these two plates, but does not penetrate deeper into the STO substrate, making an effect on the domain walls unlikely.

Side gating of micro- or nanostructures allows the strongest gate action and induces large effects even for small voltages of less than 1 V [31]. This may be due to the fact that here the gate dielectric is STO, which has a very large dielectric constant of 25 000 at low temperatures [32,33]. In [31], the authors have shown that for side gating of an LAO/STO nanostructure, the electric field lines penetrate deep into the STO substrate but reach the conducting interface from the bottom side. So, the field lines at the conducting structure have the same orientation as for back gating. As a consequence, the interpretation of results is similar to that of back-gate experiments, although the electric fields that can be reached are much higher. In addition, it should be noted that as a second consequence for symmetry reasons, reversing the gate voltage polarity reverses the field direction at the interface. In the following, this point is important because it allows one to distinguish polarity-independent domain-wall effects from polarity-dependent electron trapping. In addition, the electric field lines are located in the STO substrate, much in contrast to the top-gating geometry. In our work, we use nanostructures and side gates separated from these by no more than 1 μm, allowing us to strongly modulate the electronic structure with a side-gate voltage $V_{SG} < 2$ V.

The sample fabrication starts with growth of 6 u.c. of LAO on top of TiO_2-terminated STO using pulsed laser deposition (PLD) at 850 °C with P_{O_2} of 10^{-3} mbar. After deposition, the sample is slowly cooled down to room temperature while the oxygen pressure is maintained. Nanopatterning is done using reactive ion etching with BCl_3 [34]. To exclude that artifacts caused by defects from dry etching are the cause of our observations, we also investigate samples fabricated by a partial masking with Al_2O_3 with subsequent growth of crystalline LAO [8,35]. After the nanopatterning, 200 nm of gold are deposited using electron-beam evaporation on the sample back side for back-gate experiments. With both of these processes, we are able to fabricate high-quality nanostructures with lateral dimensions down to 100 nm. The resulting patterned structures are stable at ambient conditions. Bonding is done directly on the LAO surface with the bond breaking through to the conducting interface. The gate leakage current for all the measurements discussed here is kept below 1 nA. Four-probe electrical transport measurements are carried out in a ^{4}He bath cryostat with a variable-temperature insert equipped with a superconducting magnet that allows a maximum magnetic field of 10 T. All the measurements shown here are performed at 4.2 K, unless stated otherwise. The sample geometry used for the measurements is shown in Fig. 1(b). The lateral dimensions of the structures vary from 100 nm to 2 μm, respectively, and the length of the conducting channel is 14 μm. The side gates have a width of 10 μm and are separated from the channel by a distance of 1 μm.

As a first step, we investigate the dependence of resistance on side-gate voltage V_{SG}. Figure 1(a) shows that already a small side-gate voltage strongly modulates the resistance of a 200-nm-wide structure. A negative side-gate voltage V_{SG} of less than 1 V increases the channel resistance by four orders of magnitude, which is more than has been demonstrated with any of the four gating techniques. The saturation at approximately 2 GΩ appears only due to an offset in the current measurement that prevents the current measurement to indicate zero current. Increasing the channel width or gate channel separation reduces the modulation (not shown here) because the effective electric field field is reduced in both cases.

Next the magnetoresistance (MR) in the virgin state after cool-down and its behavior under applied gate voltage is

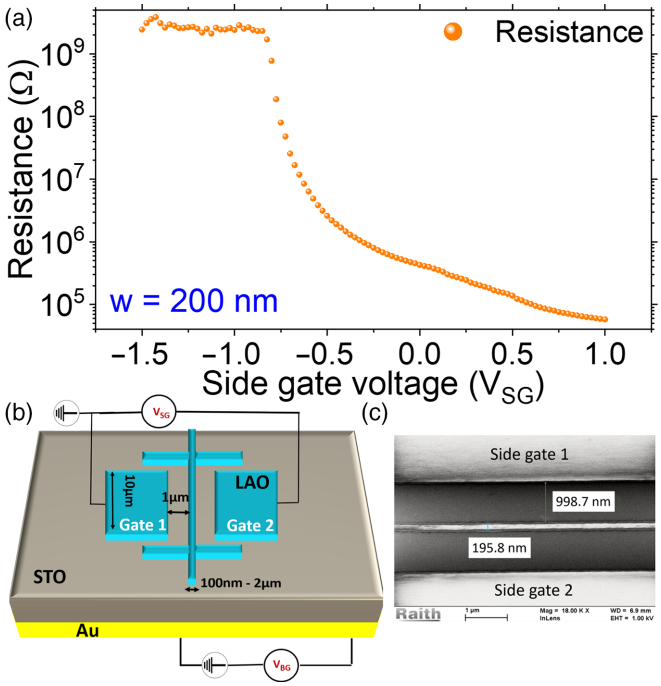

FIG. 1. (a) Resistance vs side-gate voltage for a structure with a 200-nm-wide channel. Saturation occurs because of an offset in the current measurement. (b) Sketch of the sample geometry used for the measurement. The blue area represents the 2DEG. The channel width is varied from 100 nm to 2 μm and the gate-channel separation is 1 μm. Gold on the back side of the sample is used for back gating. (c) A scanning electron microscope (SEM) image of a structure with a 200-nm-wide channel.

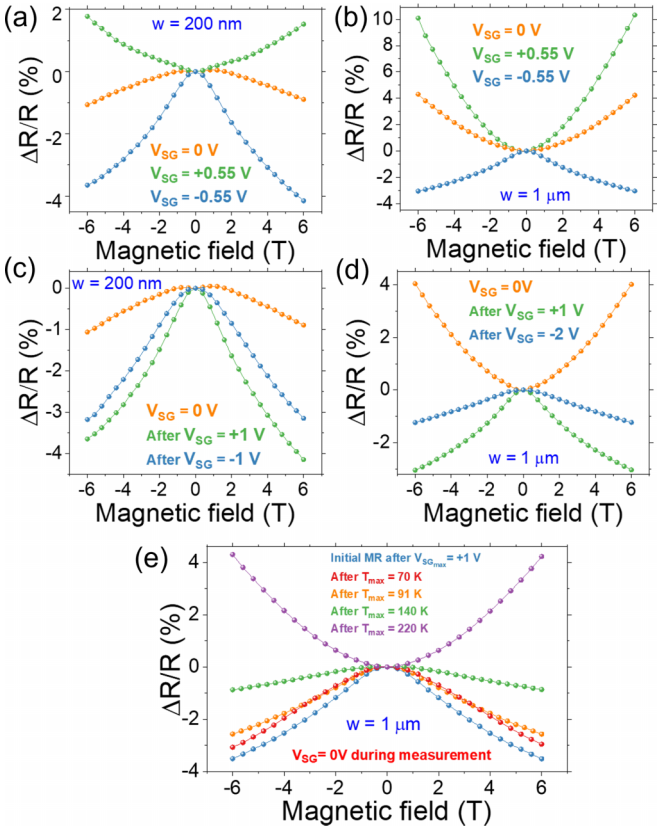

FIG. 2. (a) The MR without gate voltage and with positive and negative applied side-gate voltage, respectively, for a 200-nm-wide channel. (b) Results of the same experiment on a 1-μm-wide channel. (c),(d) The persistent negative MR after application of $+V_{SG}$ or $-V_{SG}$ when V_{SG} is again zero for a 200-nm-wide and 1-μm-wide channel, respectively. (e) The influence of temperature sweeps on the persistent MR. The persistent MR is only slightly influenced by a temperature sweeps to $T = 70$ and 91 K; however, significant changes are observed when a warm-up cycle is performed to $T = 140$ K. Also, a higher-temperature sweep ($T = 220$ K) is required to restore the positive MR observed before any gate voltage was applied.

investigated. For these measurements (Fig. 2), the magnetic field is applied perpendicular to the sample surface. The field is swept from $B = -6$ to $B = +6$ T. The initial MR without applied gate voltage is -1% for a 200-nm-wide and $+4\%$ for a 1-μm-wide structure. This small MR with arbitrary sign is consistent with former observations in [15]. With a small negative V_{SG} applied, the MR reverses sign to negative (1 μm) and becomes more negative for the 200-nm-wide bar [Figs. 2(a) and 2(b)]. This can be attributed to weak localization (WL) [27]. Before applying a positive gate voltage, we warm up the sample to room temperature and cool down again. This is necessary to restore the virgin state, as will be discussed below. For positive $V_{SG} = +0.55$ V, positive MR is observed for both structures, indicating increased electron-electron scattering due to increasing charge carrier concentration or weak antilocalization starting to dominate because of increasing spin-orbit coupling [27]. For the 1 μm structure, gradually the quadratic behavior is restored [Fig. 2(b)], also pointing towards increased scattering.

In order to study gate induced persistent modifications of the MR we use the following protocol: The sample is cooled down from room temperature (RT) to 4.2 K with $V_{SG} = 0$ V. V_{SG} is then swept from 0 V to a value $V_{SG_{max}}$, kept at $V_{SG_{max}}$ for 10 min and then decreased back to 0 V, followed by the MR measurement. Then V_{SG} is swept to a larger $V_{SG_{max}}$ (smaller for negative $V_{SG_{max}}$), repeating the same procedure. This is repeated until the gate leakage current is larger than $|I_G| = 1$ nA. Above a certain threshold of $V_{SG_{max}}$ we always observe persistent modifications [Figs. 2(c) and 2(d)] that qualitatively are independent from the sign of V_{SG}. After V_{SG} is switched off always a negative MR is observed that becomes larger with increasing $|V_{SG_{max}}|$. The magnitude of this effect is smaller for 1 μm than for 200 nm or for 300 nm. This is understandable taking into account that the influence of domain walls decreases with increasing structure width [8,15].

To check the interplay of the persistent MR and the phase structural phase transitions, we have investigated the effect after applying $V_{SG_{max}}$ at $T = 4.2$ K and warming up to a temperature T_{top}, keeping the temperature for one hour, and then cooling down again to $T = 4.2$ K. For $T_{top} = 70$ K, which is slightly above $T_{PT_1} = 65$ K, we observe a small reduction of the negative MR. Warming up to $T_{top} = 91$ K (still below $< T_{PT_2} = 105$ K) only slightly increases this tendency. For $T_{top} = 140$ K, the negative MR is almost neutralized, and at $T_{top} = 220$ K, only the ordinary MR is observed.

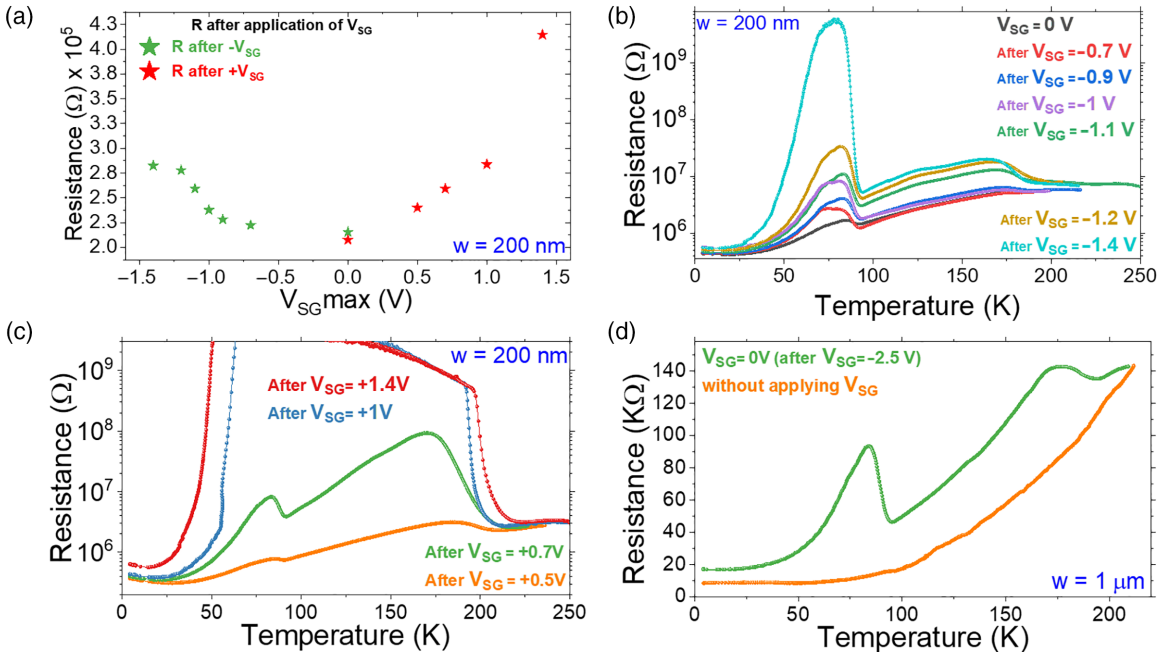

FIG. 3. (a) The persistent change in resistance after application of different positive or negative V_{SG}, respectively. (b) Temperature-dependent resistance anomaly during warm-up in various persistent resistance states induced by a different negative respective V_{SG}. Larger $|V_{SG}|$ leads to a larger peak during warm-up. (c) Temperature-dependent resistance anomaly during warm-up after persistent modification by applying different positive V_{SG}, respectively. Similar to (b), larger $|V_{SG}|$ leads to a larger peak. In addition, the peak at $T \approx 170$ K is increased. (d) Even in a 1-μm-wide structure where the anomaly is normally not observed during warm-up in a virgin state, it appears after the application of $V_{SG} = -2.5$ V.

Besides the modification of the MR, applying either large positive or large negative gate voltages also induces a persistent increase in the base resistance at $B = 0$ [Fig. 3(a)]. To gain a deeper insight, we perform warm-up temperature sweeps at $V_{SG} = 0$ after setting the high resistance state at $T = 4.2$ K by applying a suitably high side-gate voltage. These sweeps are inspired by [8], where the domain-wall structure led to large resistance peaks during warm-up for 100-nm-wide structures. After gating, we see this huge anomaly even for a structure width of 200 nm, which was not possible for ungated structures in [8]. Gate voltages of $V_{SG} \leqslant -1.4$ V or $V_{SG} \geqslant +1$ V both cause a massive resistance increase of more than three orders of magnitude that appears at $T \approx 80$ K [Figs. 3(b) and 3(c)]. Interestingly, positive gate voltages cause a further anomaly at $T \approx 170$ K that was also observed in [36,37]. Even for a 1-μm-wide structure, a resistance peak (+100%) can be induced by applying $V_{SG} = 2.5$ V [Fig. 3(d)].

A key to our observations is the independence from gate voltage polarity. Recent studies [17,18] demonstrated an irreversible increase in resistance after back gating with positive back-gate voltages. This was explained by the trapping of electrons in in-gap trap states, which are generated as a result of electromigration and clustering of oxygen vacancies in STO. A change in carrier concentration may also explain a change in magnetoresistance [27]. However, both of these explanations only hold for one orientation of the electric field. The fact that we observe persistent changes for both field polarities immediately discards these explanations. Furthermore, we observe that in all our experiments, applying a large side-gate voltage to a structure in the virgin state after cool-down induces a negative MR; however, with a random magnitude. This is consistent with the picture of a random domain-wall pattern after cool-down that nevertheless always reacts in a qualitatively similar manner to the gate voltage. However, it would be inconsistent with a pure trapping phenomenon. The preferential selection of domain walls [6,20] in large electric fields, however, is independent from the field direction. As a consequence of this selection process, the number of the domain walls is reduced, but the average domain size and thus the average length of continuous domain walls with no branching increases, which results in increased baseline resistance. In addition, the MR behavior is changed because the domain-wall patterns change from a mixture of perpendicular and tilted domain walls to preferred perpendicular orientation. In this case, theory predicts a suppression of the positive ordinary magnetoresistance and emerging negative MR by localization effects and electron-electron interaction [15], which is consistent with all our measurements. It should be mentioned that increased resistance after the application of side-gate voltage was reported to enhance the WL effect [27,31]. After removing the gate voltage, the domains are again equally stable and none of them is energetically favorable, making the effect persistent with respect to gate voltage removal. In addition, the ferroelectricity of the domain walls, which is induced above a threshold gate voltage [7], may hinder the restoration of the initial domain configuration as supported by the observation of a threshold back-gate voltage to induce the irreversible motion of domain walls [6]. Figure 4 shows a simplified sketch of a scenario in which gate-induced growth of structural domains can modify the transport properties in an LAO/STO nanostructure.

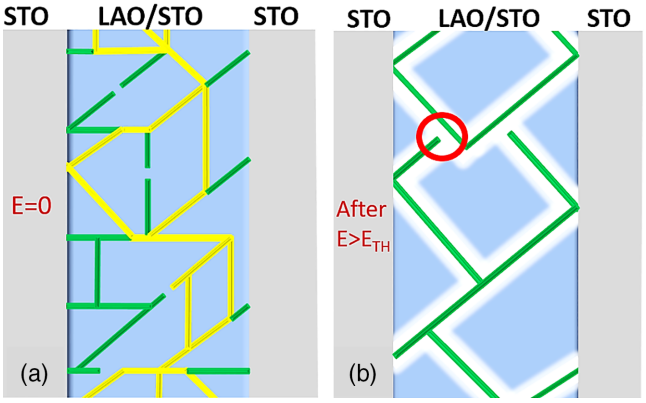

FIG. 4. Simplified sketch of a scenario in which gate-induced growth of domain size changes the transport properties of an LAO/STO nanostructure. (a) In the original domain-wall pattern, even some breaks that may appear close to the phase transition will not interrupt the current path (yellow). (b) When several domains are pushed out and the domain size increases, it is much more likely that in a nanostructure, a single break interrupts the current path and effectively suppresses the current flow. Although logical, this picture is speculative because it does not include possible dead-end filaments or conducting patches in insulating areas that may exist according to [9]. Nevertheless, these would neither carry current nor contribute to the experimental observations.

Even the temperature-dependent resistance anomaly during warm-up is in agreement with the theory. Here we have to take into account two details. Without a gate voltage, the effect is suppressed in structures larger than approximately 200 nm because of the mazelike domain structure with many parallel current paths. An increase in mesh size by the growing domains is consistent with the observation of the effect even up to a structure size of at least 2 μm. It should be noted that all the data presented here are reproducible in a qualitative manner. Also we observe that for small structures, large effects are observed, while with increasing structure

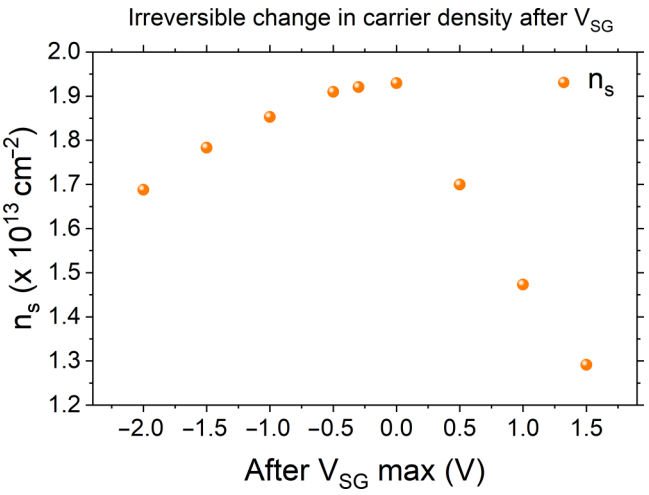

FIG. 5. Persistent modification of carrier density with the application of side-gate voltage. The carrier density was obtained from Hall measurements after applying and removing the respective side-gate voltage.

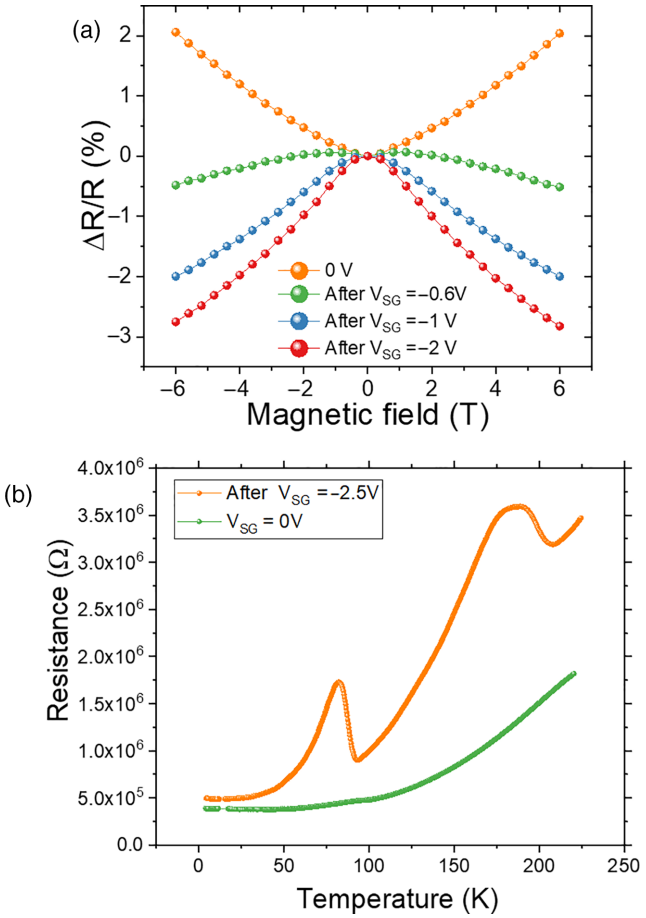

FIG. 6. (a) The MR in the virgin state after cool-down and after applying different side-gate voltages V_{SG}, respectively, for a 300-nm-wide structure. (b) The gate-induced resistance peak around 80 K for the 300-nm-wide structure and the warm-up curve from the virgin state for comparison.

size, the effects become smaller and finally vanish. This is due to the number of parallel domain walls that decreases with decreasing structure size. As a consequence, a vanishing domain wall leads to large effects if only one or two domain walls are present, while for larger numbers, the relative effect decreases dramatically and finally averages out for a large number of domain walls. The absence of a general quantitative reproducibility is explained by the underlying mechanism. The persistent modification of the domain-wall pattern can only be reset (to repeat the experiment) by warming through the structural phase transition to remove all domain walls and cooling through the phase transition to create a new pattern. This pattern, however, will have a different number, length, and type of domain walls than the state obtained after the last initialization. The dependence on structure size and the absence of any effect for large structures is another indicator that charging or trapping effects are not the main cause of the observed changes. This is in good agreement with the claim by Persky *et al.* [9] that the domain pattern only influences the transport for finite-size structures, but not in large areas. Although nanostructures allow for additional depletion effects that could explain the observations, this idea can be discarded for the following reasons. It is known from past

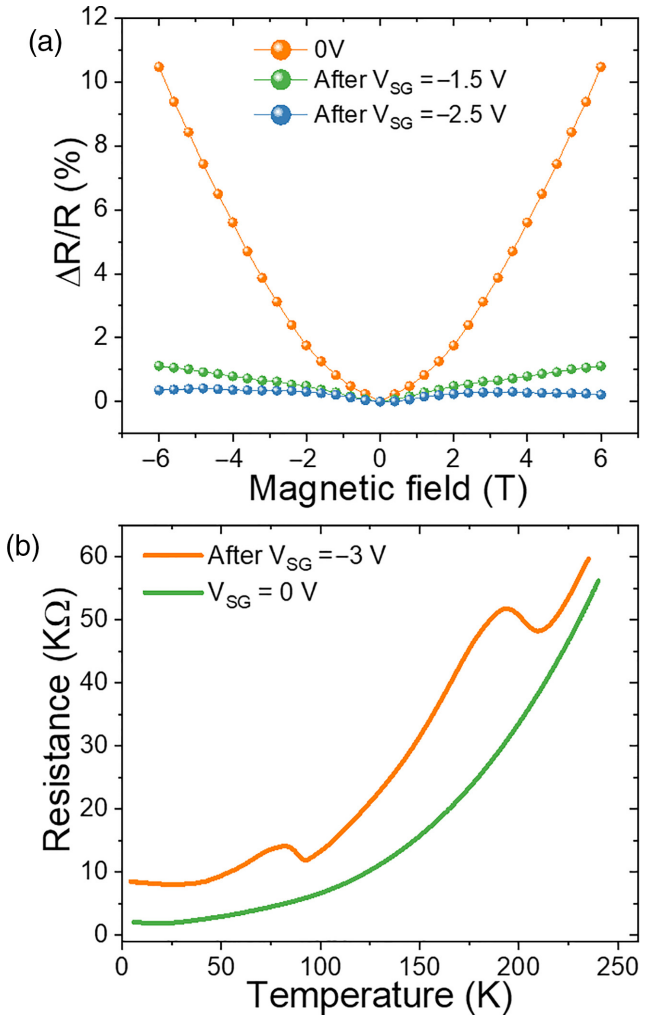

FIG. 7. Even for a 2-μm-wide structure, a side-gate voltage V_{SG} leads to the nonvolatile appearance of domain-wall-related transport effects. (a) The MR in the virgin state after cool-down and after applying different side-gate voltages V_{SG} for the 2-μm-wide structure. (b) Gate-induced resistance peaks during warm-up for the same structure. Without side gating, this feature has up to now only been observed for structures of less than 500 nm in width.

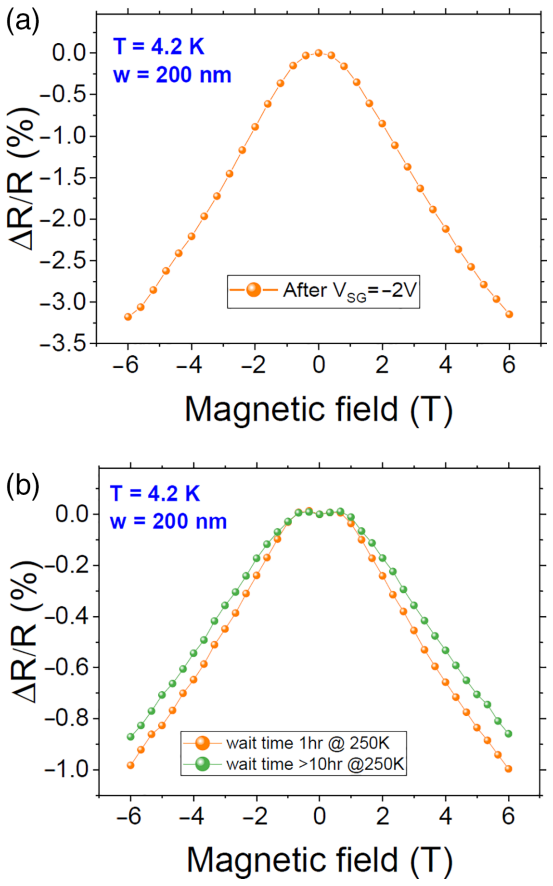

FIG. 8. Here we show how the waiting time at higher temperature affects the ground-state MR. (a) The side-gate-induced negative MR at 4.2 K. (b) Two experiments were done in which a sample was warmed from the (a) state to 250 K, then remained at this temperature for two different respective times (1 hour and 10 hours), and then cooled again to 4.2 K without side gating to observe if shorter or longer waiting times have any influence on the virgin ground-state MR. We observe that in both cases the ground-state MR is reduced by the temperature cycle; however, there is almost no difference due to the different waiting times.

work [34] that sidewall depletion takes place on a scale of tens of nanometers. The effects described here are even observed in structures as large as 2 μm. With an electron gas of, at most, tens of nm beneath the surface, any depletion effect observed for micron-sized structures should appear in a similar way in large area samples, which is not the case.

The temperature sweeps combined with MR measurements further strengthens the argument. When a temperature sweep is performed up to 70 K, we pass the lower phase transition which, according to Minhas *et al.*, leads to the breaking of some domain walls, but will not remove the complete domain-wall pattern. So most of the domain walls remain in their current orientation. Further warm-up to 90 K modifies the polar nature of the domain walls at around 80 K [16], but still keeps their orientation. So, in both cases, no major change in MR is observed. Only when warming to $T = 140$ K (above $T_{PT_2} = 105$ K) do the domain walls disappear. Still, the ordinary MR is not fully recovered because the complete charge redistribution only happens at higher temperatures, as can be seen for the sweep to $T = 220$ K. It is noteworthy that the resistance anomaly appearing around $T_{PT_1} = 65$ K is not in contradiction to these results because it is caused by the disappearance of a few domain walls, rather than reorientation and carrier redistribution.

We should mention that the additional peak that often appears at $T \approx 170$ K is of slightly different origin. Most likely, it is related to a different cubic-tetragonal structural transition that was observed at STO surfaces or interfaces that occurs at higher temperature, as reported by Salman *et al.* [38]. This could well be the reason for the requirement of higher temperatures to restore the ground-state MR. Finally, while for both polarities increasing gate voltage increases the resistance peak, the effect is even more pronounced for positive gate voltages. This is in good agreement with existing theory. Although we observe an effect due to domain walls, this does not exclude the existence of trapping at positive

voltages that apparently appears in addition to the domain-wall-related modifications. The latter is further supported by Hall measurements after the application of different side-gate voltages (Fig. 5). For both gate voltage polarities, we observe a persistent reduction of the carrier density. It should be mentioned that in the presence of domain-wall conductance, a quantitative analysis of the Hall voltage is almost impossible. Nevertheless, the apparent reduction of carrier density above a certain threshold for negative gate voltages is consistent with a reduction of the number of domain walls. The immediate and much more pronounced reduction for positive gate voltages can be explained by additional electron trapping that affects the Hall measurement much more than the domain-wall effects. Circumstantial evidence can also be obtained from the fact that these persistent effects do not appear for top gating, where the electric field does not penetrate the volume below the electron gas [39].

To further elucidate the size dependence of the effect and the range in which the gate-induced modifications can be observed, we have investigated structures with 300-nm-wide (Fig. 6) and even 2-μm-wide (Fig. 7) channels. In both cases, the applied side-gate voltage leads to a considerable change in MR and leads to the appearance of a sizable resistance anomaly during warm-up that is not observed in the virgin state. We have also tested whether, after the application of a side-gate voltage of $V_{SG} = -2\,\mathrm{V}$, warm-up to $T = 250\,\mathrm{K}$ and cool-down to $T = 4.2\,\mathrm{K}$ with different respective waiting times at $T = 250\,\mathrm{K}$ leads to different results (Fig. 8). Both waiting times of 1 hour and 10 hours, respectively, lead to a similar reduction of the side-gate-induced MR with only slight differences in absolute value. This indicates that warming through the phase transition is more important than staying at higher temperatures for a longer time span.

These results show that by using a side gate, small gate voltages can be used to obtain large persistent modifications of the domain-wall structure in LAO/STO that result in persistent MR modifications of resistance, its temperature dependence, and MR. This result also has consequences for the interpretation of low-temperature transport experiments in LAO/STO. Up to now, it seemed that large transport or magnetotransport effects only appear in structures that are 200 nm in width or less, a size that is not often used in the literature. Our results indicate, however, that electrostatic gating can shift this size limit to well above 1 μm or more where structures are usually assumed to be in the large area limit. So the interpretation of transport experiments always requires one to consider the low-temperature history of the measurements.

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