TEMPLATED FABRICATION OF PERIODIC NANOSTRUCTURES

BASED ON

LASER INTERFERENCE LITHOGRAPHY

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von Herrn M. Sc. Ran Ji
geboren am 06.12.1977 in Liaoning, China

Gutachter:

1. Prof. Dr. Ulrich Gösele
2. Prof. Dr. Ulrich Kunze

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ABSTRACT

The fundamentals laser interference lithography (LIL) and the experimental setup - Lloyd's-Mirror Interferometer- are described, which allows the parallel fabrication of periodic nanostructures, such as grating and hole/dot arrays, with a period ranging from 170 nm to 1.5 μm on 4-inch wafer areas. The following novel nanostructured applications have been developed: (1) Combined with electrodeposition or atomic layer deposition techniques, large-scale nanowire and nanoring arrays have been fabricated. (2) Wafer-scale Si_3N_4 and Ni imprint stamps with periodic imprint structures have been replicated from master structures generated by LIL. They were employed for the prestructuring of the aluminium surfaces prior to the anodization process and thus wafer-scale long-range ordered porous alumina membranes have been obtained; (3) Fin-like nanostructure arrays, nanogroove arrays and sealed hollow nanochannel arrays in silicon with EBL competitive resolutions have been obtained in combination with oxidative size-reduction strategy. Nanochannel arrays with square channel profiles are available with sacrificial resist method based on LIL generated grating structures.

CONTENTS

1 INTRODUCTION

Nowadays, the development of integrated circuits (IC) in industrial production points towards integration of more devices per chip area. In addition, materials in nanometer dimensions show novel physical and chemical effects. The pattern generation technologies realize the circuit design data into actual physical structures. Therefore, the IC industry and scientific research rely more and more on nanofabrication technologies, which are outgrowth and extension of microfabrication.

Optical lithography is well established as the manufacturing technology of choice for the IC industry which has already achieved gate lengths of 65 nm and less in production. The resolution of projection optical systems is approximated by the Rayleigh relation [1, 2] (Equation 1.1), where k_1 is a system constant, λ is the exposure wavelength and NA is the numerical aperture. However, this ultimate resolution requires an expensive light source (now a laser source with 193 nm wavelength and in the future even soft x-ray) and optics (immersion lithography).

$$resolution = k_1 \lambda / NA \qquad \text{Equation 1.1}$$

Usually for nanoscience research, with low cost light source and mask fabrication conditions, optical lithography is only the technique of choice for the generation of structures with μm-dimensions. Electron-beam lithography (EBL) allows the fabrication of nanostructures with very high resolution, but limited by its throughput. Its main applications are to create prototype of nanostructures for fundamental research on small-scale and photomasks.

Fortunately, many applications, such as magnetic storage, photonic crystals, definition of nucleation sites for the growth of nanowire and nanotube arrays, property investigations of compact material elements, require only a periodic pattern. Laser interference lithography (LIL) is a simple laboratory-scale and maskless technique for patterning regular arrays of fine features without the use of complex optical system. The benefit of interference lithography is the quick generation of dense structures over a

large-area at a low cost with considerable pattern flexibility as well. In combination with other patterning techniques, LIL expands dramatically the available range of patterns and feature sizes.

In this work, a simple but flexible LIL configuration has been set up for lithographic exposures. The detailed description of the LIL process and related techniques can be found in Chapter 2. Novel applications of LIL generated periodic patterns have been developed to overcome the difficulties of traditional lithography techniques. LIL has been introduced for the fabrication of nanoring arrays, imprint stamps for long-range ordered AAO membranes and nanograting or nanochannel arrays, respectively. In each application LIL shows its unique advantages.

LIL FOR NANORING ARRAYS (CHAPTER 3)

For the first time, LIL was introduced into the fabrication of large-scale nanoring arrays. LIL has the convenience of parallel fabrication of hole arrays with easy control over hole size, arrangement and shape, especially for elliptical-shaped hole arrays in photoresist layer on Si substrate. These structures were utilized as templates for the synthesis of nanoring arrays by depositing desired materials along the edges of the holes. The as-prepared (magnetic) nanoring arrays on planar substrates could be easily studied with conventional bulk-characterization techniques.

LIL FOR IMPRINT STAMPS (CHAPTER 4)

As a novel process route large-area imprint masters have been developed, which are applied for hard imprint lithography on aluminium surfaces. Subsequently, the pre-patterned Al substrates are anodized and can form perfectly ordered AAO membranes. LIL is a very powerful tool for the definition of 2D matrix imprint stamp structures with different arrangements for the prepatterning the aluminium surface prior to the anodization process. Compared to other structuring techniques for the stamp fabrication in the literatures, such as optical lithography and EBL, LIL has advantages in resolution and throughput, respectively.

LIL FOR GRATING AND CHANNEL ARRAYS (CHAPTER 5)

It is worth noting that LIL allows the fabrication of grating structure with lengths across the whole wafer, which is impossible with EBL. Such grating structures are suitable for fabricating fin-like structures, nanogroove arrays and nanochannel arrays. In combination with the oxidative size-reduction strategy, oxidative self-sealing strategy and sacrificial material methods, large area fin-like or groove arrays and channel arrays are parallel generated with EBL competitive feature sizes (down to 30 nm). Especially, the nanochannel structures obtained by the sacrificial resist method are highly desirable for templated synthesis of planar arranged arrays of nanotubes with square cross-section.

2 LASER INTERFERENCE LITHOGRAPHY (LIL)

Laser interference lithography [3~22] (LIL) is a method to produce periodic structures using two interfering highly-coherent light beams. Typically, light from a source is divided and recombined, forming a periodic intensity pattern that can be recorded by the exposure of a photosensitive substrate. The primary focus of this thesis has been the setting up of a Lloyd's-Mirror Interferometer. In this chapter, the fundamentals of laser interference lithography will be introduced step by step: The description of the basic theory of LIL, can be found in section 2.1; the working principle of the "Lloyd's-Mirror Interferometer" and the whole optical setup are introduced in section 2.2; the preparation of the substrates before lithographic exposures and the design of the resist stack for LIL are explained in section 2.3; the aspects of the exposure process are discussed in section 2.4; finally, the structural transfer from the soft resist into a hard substrate by means of reactive ion etching (RIE) and wet chemical etching will be discussed in section 2.5.

2.1 BASIC THEORY: INTERFERENCE OF TWO BEAMS

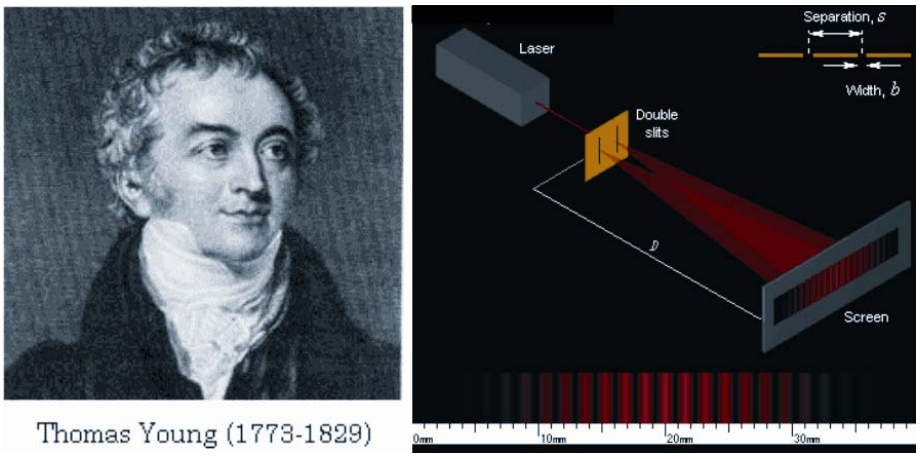

Figure 1: Thomas Young and a laser interference setup adopted from his famous experiment.

Thomas Young (1773-1829), first demonstrated the interference of light in 1801 (Figure 1). [23,24] His famous interference experiment gave strong support to the wave theory of

light. This experiment (diagramed above) shows interference fringes created when a coherent light source is shining through double slits. Light sources available in 1800 were essentially flames. He produced coherent light by letting nearly monochromatic light through a pinhole, then using the light from that pinhole to fall on two other pinholes that were very close together.

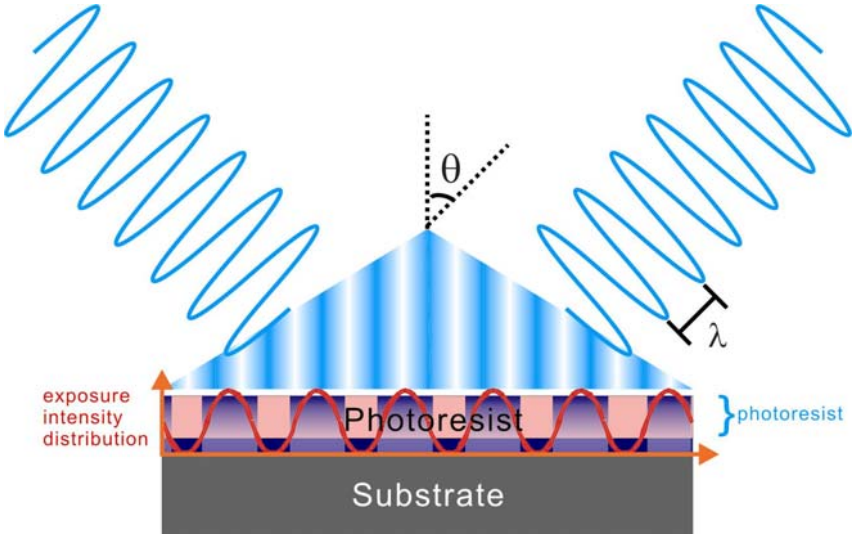

Figure 2: Interference of two coherent light waves and the intensity profile in a photoresist layer.

Nowadays, lasers produce intense beams of monochromatic (single frequency) light. All the waves across the beam are in phase. If we use a laser beam to illuminate the slits, which are narrow to ensure adequate diffraction, the diffracted beams from the two slits overlap causing the superposition of two light waves, which appears on the screen as alternate dark and bright bands, called fringes. The bright fringes are caused by constructive interference and the dark fringes by destructive interference.

For lithographic applications, the most intuitive way to form a set of interference fringes is simply to split a beam into two, and then recombine the two beams. The intensity distribution of a superposition of two plane-waves will give a spatial structure that is non-uniform, known as sinusoidal form (Figure 2). Under the assumption of symmetry of incidence angle, the periodicity (p) of the fringe pattern of two interfering beams can be simply described with Equation 2.1, where λ is the wavelength of the beams and θ is the half angle between the two incidence beams.

$$p = \frac{\lambda}{2\sin(\theta)}$$ Equation 2.1

Figure 3 shows a simplified configuration of a Mach-Zehnder Interferometer [25] for lithographic exposures. An UV laser is split in two arms which are recombined using a set of mirrors. Spatial filters in each arm serve to expand the beams for dose uniformity over a large area and to remove the spatial frequency noise. Due to the long propagation distance and the lack of additional optics after the spatial filters, the beams interfering at the substrate can be accurately approximated as spherical. A set of sensors and a compensation system are used to correct the phase errors. The whole setup should be placed on an actively damped optical table in order to filter the vibrations.

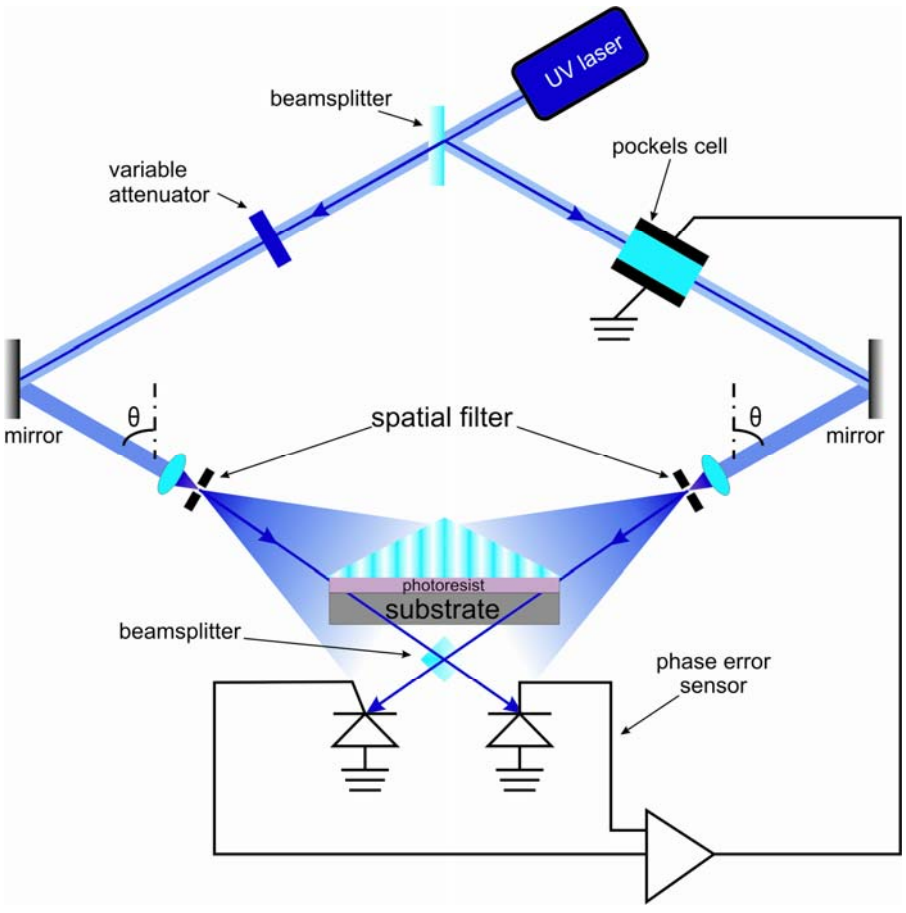

Figure 3: Schematic illustration of a Mach-Zehnder Interferometer [25].

However, accurate positioning and precise alignment are required to produce a single grating structure with Mach-Zehnder Interferometer. When the grating periodicity has

to be changed, a complete and time-consuming re-adjustment of the whole optical setup has to be pursued, which limits the flexibility of Mach-Zehnder Interferometer in many cases.

2.2 EXPERIMENTAL SETUP

2.2.1 LLOYD'S-MIRROR INTERFEROMETER

As introduced above, the versatility of the Mach-Zehnder Interferometer is limited. Furthermore, beyond gratings, there are a number of periodic patterns that can be created through multiple exposures, for example, hexagonal or square arrays. Applications that require a multitude of different periods, such as nanostructures with an anisotropic shape, are difficult to realize using the traditional Mach-Zehnder Interferometer.

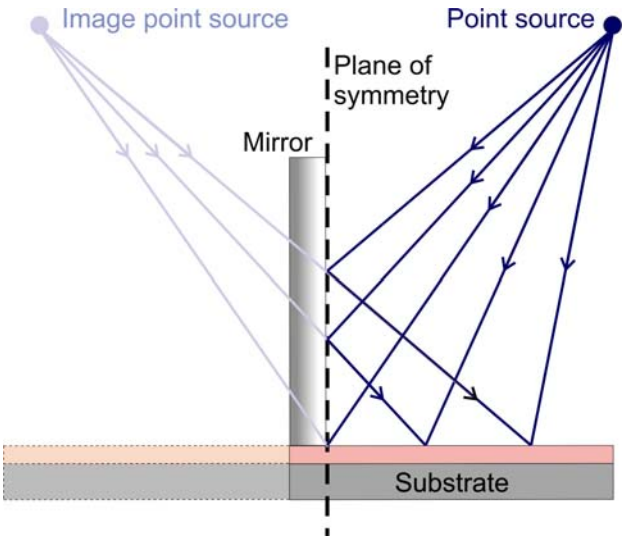

Figure 4: Schematic illustration of the principle of Lloyd's-Mirror system comparing it to the Mach-Zehnder Interferometer [25].

Mach-Zehnder Interferometer and Lloyd's-Mirror Interferometer, both systems are designed to produce high-contrast interference pattern with a high spatial-frequency over a large exposure area. In fact, as shown in Figure 4, the ideal Lloyd's-mirror is optically equivalent to half of a Mach-Zehnder Interferometer. Consider the plane of

symmetry for the Mach-Zehnder located halfway between the two sources and which determines the angle of interference. The system on either side of this plane is a mirror image of the other side. Thus, if indeed we would place a mirror in this plane, the resulting set of interference fringes would remain unchanged. [25]

In this work, the Lloyd's-Mirror Interferometer (Figure 5) was utilized for the lithographic exposures. The Lloyd's-Mirror Interferometer consists of an aluminum mirror (Linos), which has a roughness $\leq \lambda/2$ and a very high reflectivity (> 92%) for the HeCd laser, placed perpendicular to the sample holder. The aluminium mirror was chosen due to its enhanced UV reflectivity compared to other mirrors and for its essentially constant reflectivity over a broad range of angles. Our interferometer was designed to expose up to 4 inch substrates. To minimize the effects of edge scattering and diffraction, it would be desirable to use a mirror which is larger than the exposed substrate. The mirror currently in use is 10 ×15 cm.

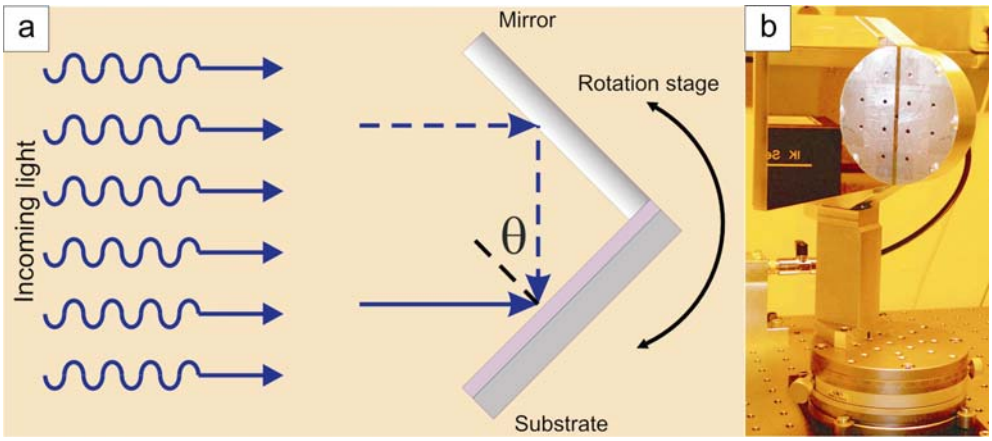

Figure 5: (a) Schematic illustration of the basic principle of Lloyd's-Mirror Interferometer; and (b) a photograph of our interferometer.

The laser is expanded and spatially filtered through a pinhole to generate a coherent beam with a ca. 30 cm in diameter at the interferometer. The UV beam illuminates both the mirror and the sample. Part of the light is reflected on the mirror surface and interferes with the portion of the beam that is directly illuminating the sample. This interference will give a line pattern with a periodicity given by Equation 2.1, where λ is the wavelength of the laser beam (here fixed at 325 nm) and θ the angle between the incidence light and the sample normal. By changing the incidence angle θ with the

rotation stage, the periodicity (p) can easily be adjusted from 170 nm to 1.5 µm in this case.

2.2.2 OPTICAL SETUP

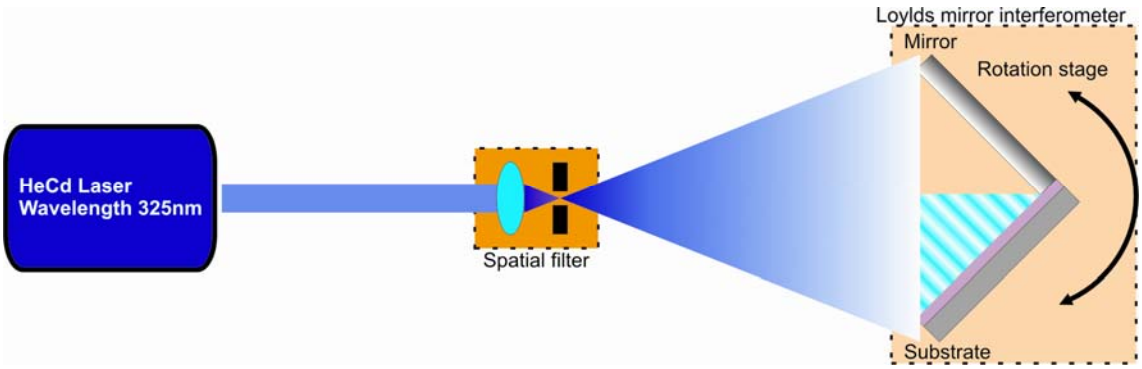

Figure 6: Schematic illustration of optical setup of LIL.

A simplified diagram of the optical setup is shown in Figure 6. In this work, we have used a HeCd laser with a wave length of 325 nm and an output intensity of 60 mW as a light source. HeCd offers a long (30 cm) coherence length at a mid-UV wavelength in a more robust package and at a lower cost than other options, such as argon-ion and excimer lasers. This UV laser is optically filtered with a commercial spatial filter (Newport) consisting of a UV objective lens with a focal distance of 5.77 mm and a pinhole of 5 µm in diameter, which allows high spatial-frequency noise to be removed from the beam to achieve a near-Gaussian beam. The Lloyd's-Mirror Interferometer itself, consisting of a sample holder, mirror and rotation stage, is placed approximately 2 meters from the spatial filter. To prevent vibrations, which could disturb the interference pattern, the complete setup is built on an actively damped optical table of 1.5×2.5 m. The optical components are placed in a closed cabinet to avoid air movements, which could affect the stability of the interference pattern.

As a Gaussian beam expands, it changes in three ways [25]. The intensity decreases, the diameter of the beam increases, and the radius of the phase front increases. Lowering the intensity leads to increased exposure times. Because of the Gaussian intensity profile, increasing the beam diameter ensures that the entire interferometer could be illuminated and creates a more uniform intensity distribution over the exposed area.

With this setup highly regular grating patterns can be produced over 2/3 of 4 inch wafer areas. Finally, the increase in radius of the phase front means that the beam more closely approximates a plane-wave over the exposure area, which is a very important assumption for the two-beam interference system. Thus, by maximizing the beam expansion, the exposed grating will have a more linear spatial phase and a more uniform line width, at the expense of a longer exposure time.

2.2.3 CALIBRATION OF THE EXPERIMENTAL SETUP

In stark contrast to the Mach-Zehnder Interferometer, the fringe period can be varied by simply rotating the interferometer. However, two conditions must be met to guarantee that to be optically equivalent. One is that the mirror is truly mounted perpendicular to the substrate. The other is that the interferometer axis defined by the intersection of the mirror surface and the substrate surface is the axis of rotation. The Lloyd's-Mirror Interferometer must be calibrated by exposure experiments and investigations with SEM or AFM. These issues will be discussed further in the following sections.

2.2.3.1 ANGULAR ALIGNMENT OF MIRROR

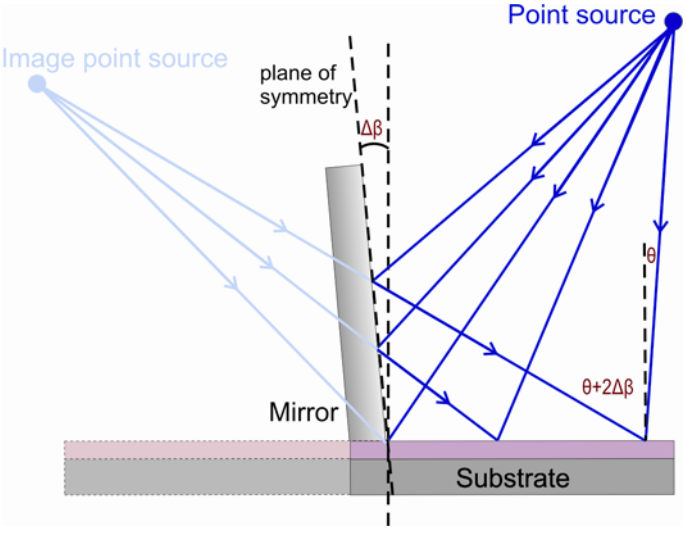

Figure 7: Misalignment of the mirror from normal by an angle of Δβ. [25]

For mirror angles not equal to 90 degrees, the symmetry will be broken and the image light source will be placed in a different position relative to the substrate than the real

source (Figure 7). This will result in a different incidence angle on the substrate for the reflected portion of the beam while the direct beam remains unchanged. The fringes will not form perpendicularly to the substrate and their periodicity will change. For a mirror angle which is equal to $\beta=90°+\Delta\beta$, the angle of inclination of the fringes will also be $\Delta\beta$. The periodicity $P_{\Delta\beta}$ of the fringes can be described with Equation 2.2. [25]

$$P_{\Delta\beta} = \frac{\lambda}{2\sin(\theta + \Delta\beta)} \qquad \text{Equation 2.2}$$

The fringe period recorded on the substrate P_s, shown in Equation 2.3 [25] will be the projection of the new fringe period $P_{\Delta\beta}$ into the substrate plane.

$$P_s = \frac{P_{\Delta\beta}}{\cos(\Delta\beta)} \qquad \text{Equation 2.3}$$

Combining the two equations, we can solve for the grating period on the substrate, shown in Equation 2.4 [25].

$$P_s = \frac{\lambda}{2\sin(\theta + \Delta\beta)\cos(\Delta\beta)} \qquad \text{Equation 2.4}$$

For a tiny deviation $\Delta\beta$ of the mirror from normal, the cosine term can be approximated as unity, leaving $\Delta\beta$ as a calibration error. [25]

2.2.3.2 ALIGNMENT OF ROTATION AXIS

An exaggerated cartoon of the misalignment of rotation axis is show in Figure 8. Under the assumption that the incident light is planar, the direction of the incident wavefronts will be determined by the location of the pinhole or point source. If the axes of the interferometer and the rotation stage are misaligned, there will be a lateral shift of the point source ΔP as a function of the rotation angle α which creates an error α' in the interference angle θ, where the maximum error will occur when the incidence angle is 90° (Equation 2.5 [25]).

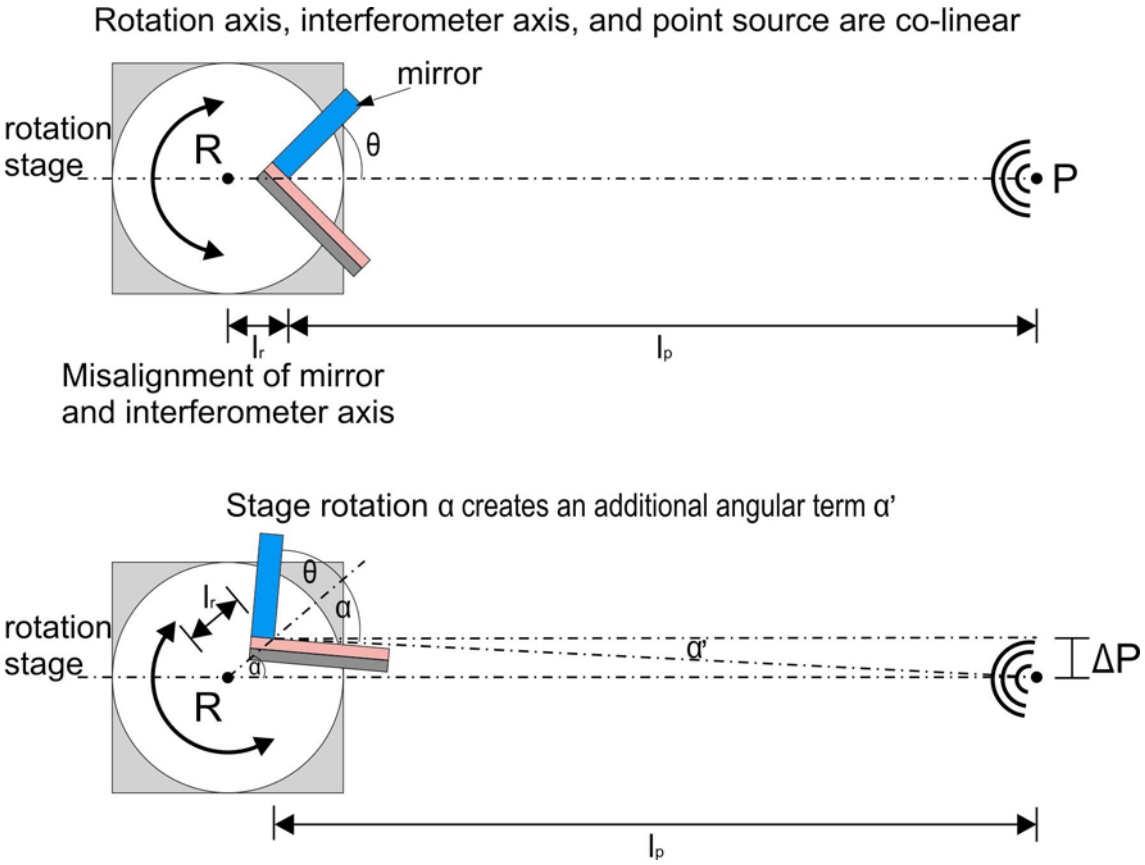

Figure 8: When the axes of the interferometer and the rotation stage are misaligned, there will be a lateral shift of the interferometer ΔP as a function of the rotation angle α which creates an error α' in the interference angle [25].

$$\Delta P = l_r \sin(\alpha) \qquad \text{Equation 2.5}$$

2.2.3.3 CALIBRATION WITH EXPOSED STRUCTURES

If we consider the misalignment of mirror angle and rotation axis, we can summarize the misalignments to a general constant error p' and an angular error θ' to the period of the structures generated by LIL exposure (Equation 2.6).

$$p = \frac{\lambda}{2\sin(\theta + \theta')} + p' \qquad \text{Equation 2.6}$$

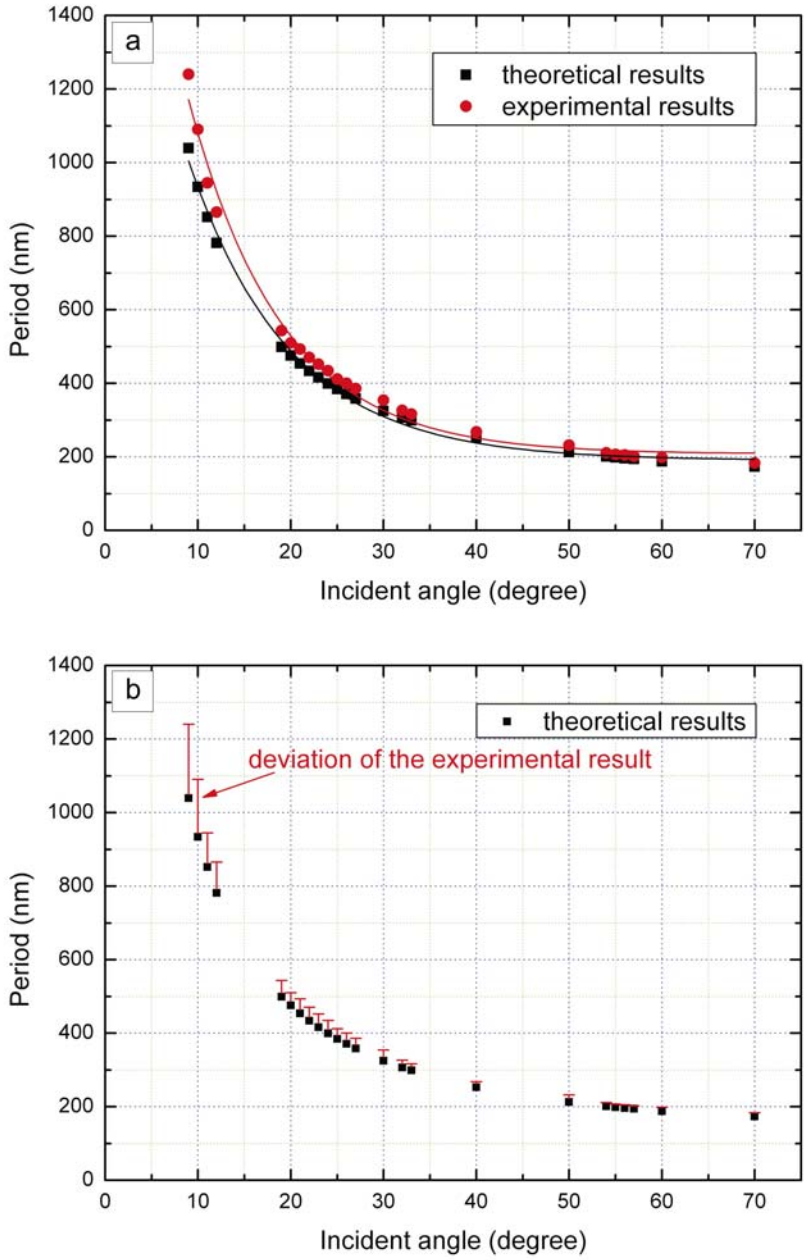

Figure 9: (a) Comparison of experimental results to theoretical results; (b) deviation of the experimental results as error bars.

Lines structures were exposed under different incident angles with our interferometer and the periods of the samples were measured with an AFM. The calculated theoretical results comparing with the experimental results are shown In Figure 9a. From the curve it is apparent that all the experimental results are always larger than the corresponding

theoretical results with our interferometer. We can deduce that there must be an initial constant error *p'* of ~10 nm, which can be deducted from the results. The angular error *θ'* ranging from 2° to 4° could be calculated from Equation 2.6. The deviations of the measured periods are characterized as error bars in Figure 9b. In case of structures with a period smaller than 500 nm, a deviation of less than 5% could be obtained, which is acceptable for most of the lithography techniques.

2.3 PRETREATMENT OF THE SUBSTRATE

2.3.1 GENERAL INTRODUCTION TO THE SUBSTRATE

In this work, silicon wafers have been mainly used as substrates for the performance of LIL exposures. The preparation, i.e., the cleaning processes of the wafers will be introduced in section 2.3.2. A SiO_2 or Si_3N_4 layer was usually deposited between silicon wafer and resist stack or on the interface of resist stack for the further structure transfers. The oxide layer on the silicon wafer was thermally oxidized, whereas the SiO_2 layer on the interface between resist layers was sputter deposited. As in common lithography techniques, photoresists are employed to record the lithographic pattern. However, the optical reflections on the interfaces could affect the lithographic results in the LIL process. ARC was employed to minimize the negative effects of the unwanted reflections on the interfaces, which will be detailed discussed in section 2.3.4. The typical substrate stack design is schematically illustrated in Figure 10. The polymer layers were realized using spin-coating technique in this work, which will be introduced in section 2.3.3.

Figure 10: Schematic illustration of the cross-section of typical substrate stack used in this work.

2.3.2 WAFER PREPARATION

As a pre-treatment, silicon wafers were always chemically cleaned in the MPI cleanroom facilities. Standard cleaning procedure, known as RCA-clean, [1,2] which consists of a sequence of different wet clean processes, has been utilized in this work. RCA-1, RCA-2 and HF dip are each effective in removing different types of contaminations. Table 2.1 [1] lists the main processes and information for the RCA-clean commonly in use.

Table 2.1 Wafer cleaning processes

	Process	Treatment/Chemical composition	Comments
1	RCA-1	$NH_4OH:H_2O_2:H_2O$ (1:1:5)	75 °C, 10 min removal of organic dirt
2	Rinsing	DI-water	Room temperature, 5 min
3	RCA-2	$HCl:H_2O_2:H_2O$ (1:1:6)	75 °C, 10 min removal of metal ions
4	Rinsing	DI-water	Room temperature, 5 min
5	HF dip	1% aqueous HF	Room temperature, 30 sec removal of SiO_2 layer
6	Rinsing	DI-water	Room temperature, 5 min
7	Drying	Spinning with nitrogen blowing	1st step: 1800 U/min, 2min 2nd step: 600 U/min, 2min

Standard chemicals come in the following concentrations:

NH_4OH	29%

HCl	37%
H_2O_2	30%

2.3.3 RESIST FILM DEPOSITION: SPIN-COATING

The polymer films, such as photoresist and anti-reflection coatings, were deposited on the substrates by using the spin-coating technique. Spin-coating is a very widely used method for resist spinning. It is a reliable process for the deposition of thin films of viscous materials (e.g. polymers or sole gels) with precise control over film thickness on large substrate. A spinner (SÜSS MicroTec) with a typical spin speed up to 6000 rpm was used in this work. The dominant parameters for film thickness control via spin-coating are viscosity, solvent evaporation rate and spin speed. The principle of this technique is schematically illustrated in Figure 11.

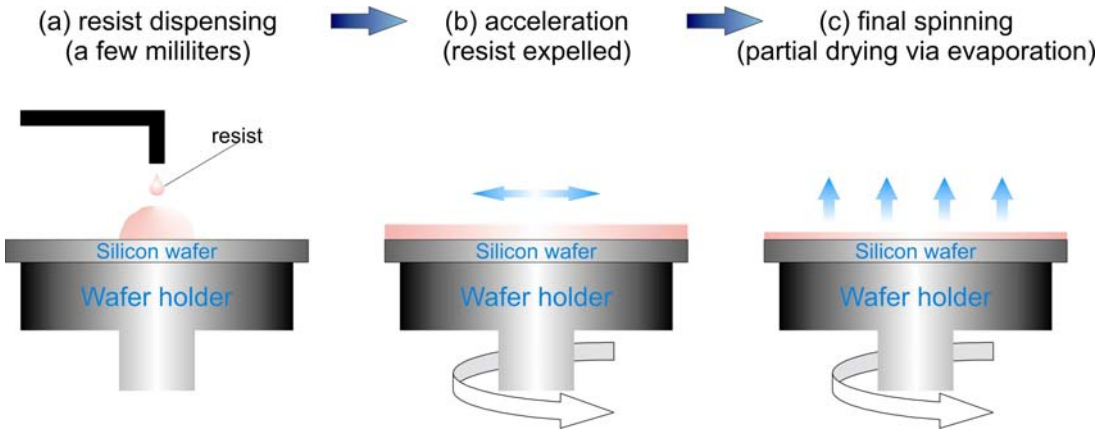

Figure 11: Schematic illustration of spin-coating process.

First, depending on the wafer size and the desired film thickness, a few milliliters of photoresist is dispensed on the substrate surface with clean-room pipettes in static mode or at slow rotation of ca. 300 rpm. Acceleration to the wanted spin speed spreads the liquid resist towards the edges. Half of the solvent can evaporate during the first seconds, but the whole spinning process is usually performed for 1 min. A room temperature spin-coating is always accompanied with a baking step of the resist on a hot

plate in order to achieve a solid resist film. Since the baking is performed before the lithographic exposures, it is called “Pre-bake”. (The spin-curves of the photoresist and Anti-reflection-coating used in this work can be found in Appendix: Spin-curves of PR and ARC)

2.3.4 ANTI-REFLECTION-COATING (ARC)

During interference lithography exposure, in addition to the primary standing wave formed parallel to the substrate, standing waves are also formed perpendicular to the substrate. Because the silicon (or SiO_2) substrate is reflective, the vertical components of the incident light and the light reflected at the interface of substrate and the photoresist layer interfere with each other and form vertical standing waves (Figure 12).

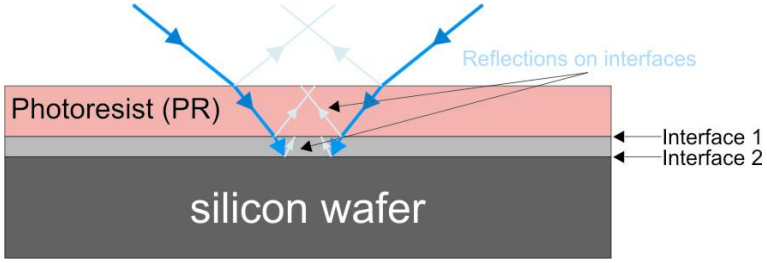

Figure 12: Reflections on the interfaces.

This standing wave can severely degrade the resist profiles after development if it is not sufficiently suppressed. The period of the vertical standing wave is determined by the following factors: the wavelength of the light, the interference angle and the refractive index (n) of the photoresist (Equation 2.7 [25]).

$$P_{vertical} = \frac{\lambda}{2n \cdot \cos(\theta)} \qquad \text{Equation 2.7}$$

The vertical standing wave can “scallop” the sidewalls of the resist structure to form a narrow waist. This waist can sufficiently weaken the resist structure so that it could break during the wet chemical development or washing process. In a more extreme case, this waist can actually cut through the resist structure and cause the top section to separate. The severity of the vertical standing wave will vary with the contrast of the wave. Obviously, one way to decrease the effect of this standing wave is to minimize

the reflectivity at the interface. Standard procedure is to use an anti-reflection coating (ARC) underneath the resist layer. An interlayer between the resist and the ARC is also sometimes employed to facilitate pattern transfer (will be discussed in section 2.5.2). In general, the ARC works through a combination of absorption and cancellation through interference. [25] Thus, both the thickness and the optical constants of an ARC play a role to suppress the vertical portion of standing wave.

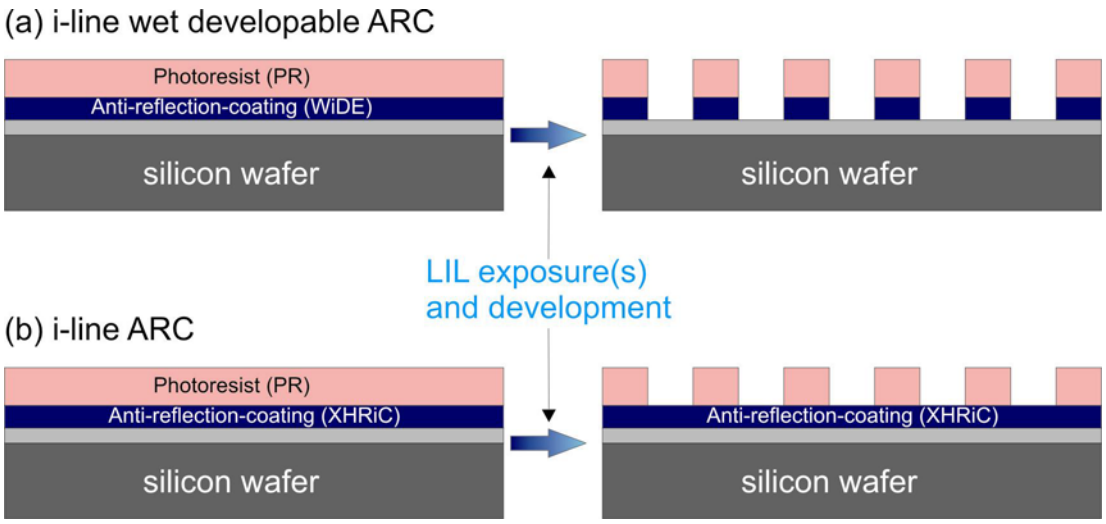

Figure 13: Schematic illustration of the difference between (a) wet-developable and (b) non-wet-developable ARCs.

We have used the commercial i-line ARCs of Brewer Science, Inc. in this work. Two kinds of ARCs were chosen for the interference lithographic exposures: wet developable ARC (WiDE-B) and standard ARC (XHRiC). The difference between wet- and non-wet-developable ARCs is schematically illustrated in Figure 13. It is worth pointing out that the process window for the wet-developable ARC WiDE-B is severely dependent on the pre-baking temperature subsequent to the spin-coating deposition.

A simulation program based on “Matlab” written by the MIT Nanostructure Laboratory (Freeware) was employed for calculation of the optimum thickness of each layer of the substrate stack in order to minimize the reflectivity at the interface between resist and substrate. Figure 14 illustrates a typical substrate stack in cross-section view.

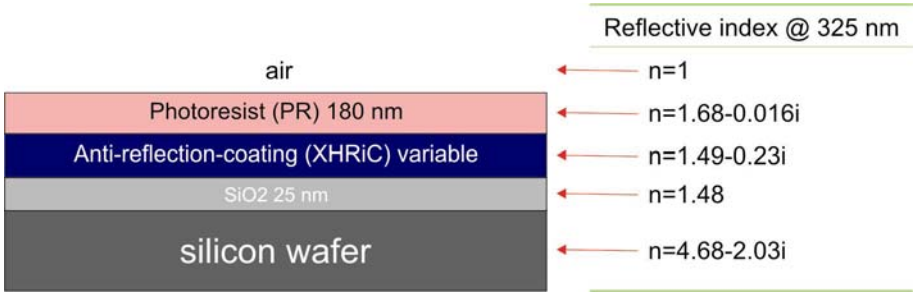

Figure 14: Schematic illustration of a typical substrate stack with the optical constants of each layer.

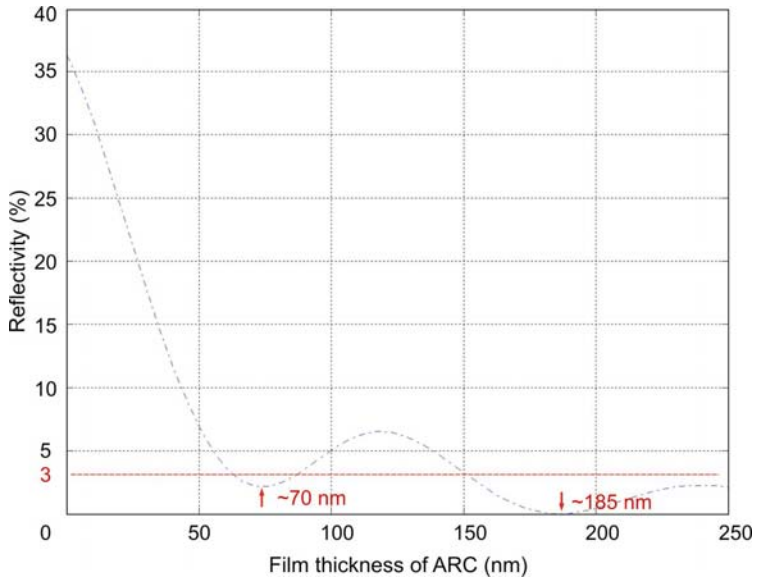

Figure 15: The simulated result corresponding to the stack design illustrated in Figure 14.

The optical constants of each layer and the desired period of the structure are led into the program. The thickness of the ARC layer is the variable for the calculation. The software simulated reflectivity curve relative to the ARC thickness. In this case the software simulated reflectivity curve relative to the ARC thickness is plotted in Figure 15. Usually the reflectivity below 3% is acceptable from experimental aspects. Thus two process windows (ARC thickness at ca. 70 and 185 nm) have been found. In other words, if the ARC thickness is chosen at these values, the vertical standing wave will be most sufficiently suppressed and therefore a high contrast resist profile could be obtained by LIL exposure. In Figure 16, a clear contrast of sufficient and insufficient suppression of the vertical standing wave by using ARC layer has been demonstrated with SEM images.

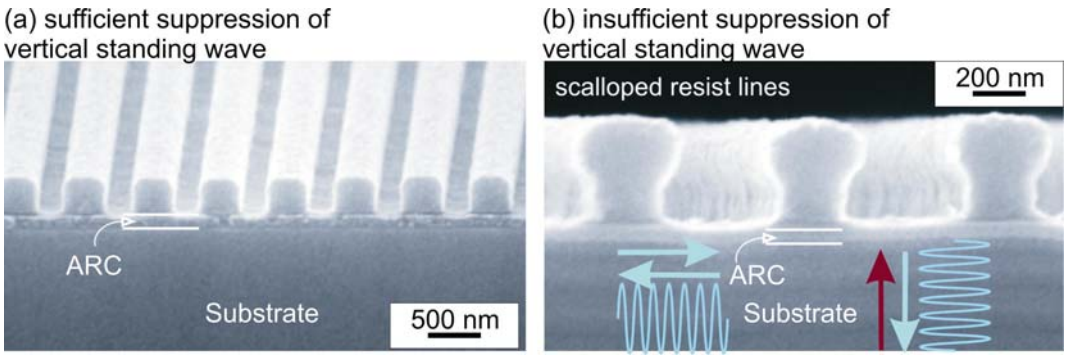

Figure 16: SEM images of the resist profiles of line pattern in case of (a) sufficient and (b) insufficient suppression of vertical standing wave by using ARC layer.

2.3.5 PHOTORESIST (PR)

As introduced in section 2.1, the periodic fringe pattern produced by interfering of two beams is recorded by the photoresist. Due to its highly non-linear dissolution rate as a function of exposure dose, the sinusoidal intensity pattern becomes a periodic array of individual lines in the developed photoresist.

Commercial i-line (365 nm) positive photoresists: TDMR-AR80 HP and negative photoresist TSMR-iN027 PM (produced by Tokyo OHKA KOGYO Co., Ltd.) were used as a basis in this work. In some cases, in order to improve the resist adhesion to the substrate, an adhesion promoter, hexamethyl disilazane (HMDS, $(H_3C)_3$-Si-NH-Si-$(CH_3)_3$) is applied to form a monomolecular layer on the substrate surface, making the substrate hydrophobic, which prevents moisture condensation. For the development of the exposed resist, a standard i-line organic developer (NMD-W, TMAH 2.38%) has been used in this work.

2.4 LIL EXPOSURE

2.4.1 EXPOSURE DOSE: DUTY-CYCLE

$$DC = \frac{W_{line}}{P_{grating}}$$ Equation 2.8

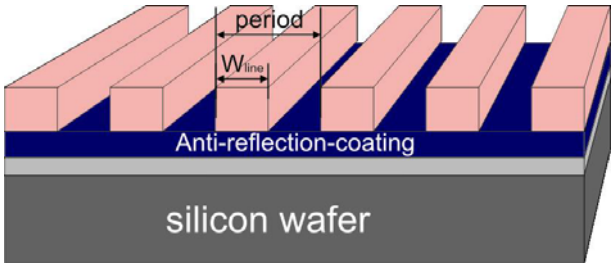

Figure 17: Schematic illustration of duty cycle.

In order to evaluate exposure the results and the resist contrast, an important index of the LIL technique, the so-called "duty-cycle" (DC) is introduced in this section. The definition of DC, the ratio of the feature size (line width) of the periodic structure generated by LIL in a given period to the period, is described by Equation 2.8 and schematically illustrated in Figure 17. As introduced in Equation 2.1, the periodicity of the structure depends on the wavelength of the laser and the incident angle. Assuming a fixed period, the feature sizes could be controlled by changing the DC value, which depends on the exposed dose.

As schematically illustrated in Figure 18, the spatial variation of the exposure dose generated by LIL could be considered as a sinusoidal distribution. The simplest and most common model for photoresist is the ideal binary response: assuming a negative PR, above a certain threshold value D_{clip} the resist is fully exposed and could be maintained in the resist developer, while below that threshold the resist is fully unexposed and could be dissolved during development. In terms of our systematic investigations, three factors have been found, which can affect the DC value of LIL exposures: incident angle, exposure time and postbake temperature. These factors will

be discussed in the following sections.

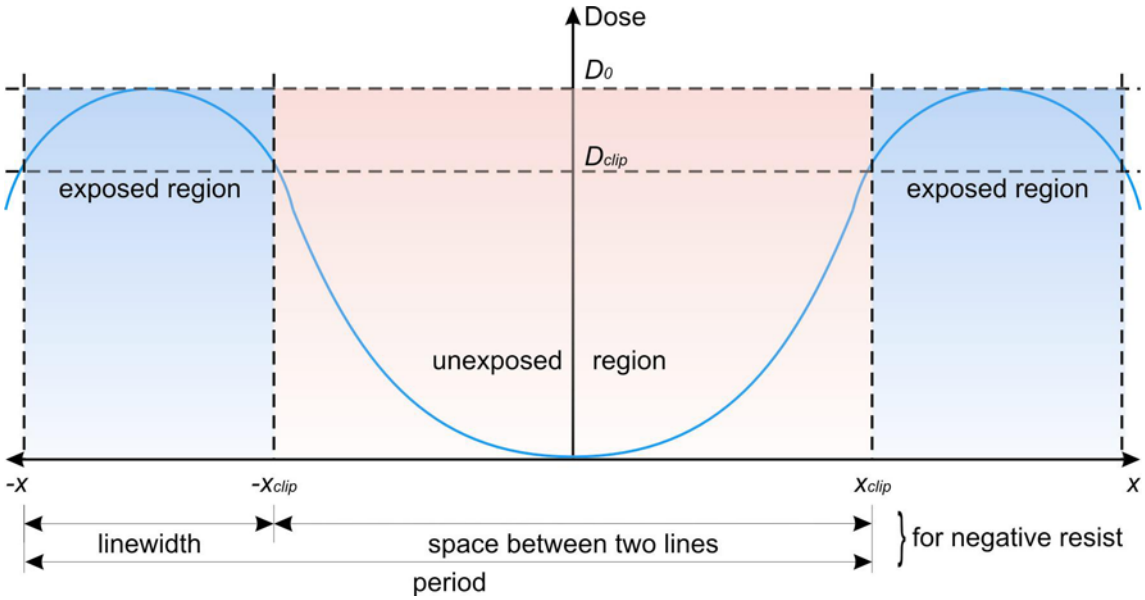

Figure 18: Schematic diagram of the binary model for response of the photoresist exposure. [25]

2.4.1.1 DUTY-CYCLE TO INCIDENT ANGLE: EQUIVALENT DOSE

The incident dose, defined as the total energy of the exposure, is the product of the incident power per unit area I_0 and the exposure time t.

$$D_{incident} = I_0 \times t \qquad \text{Equation 2.9}$$

The source power I_0 at the initial stage (after pinhole) could be considered as a constant. Thus, the exposure time is the only parameter which can be easily varied. The relationship between exposure time and duty-cycle will be discussed in the next section. For LIL exposure, one cannot simply assume a constant dose for exposures of different periods, even under identical exposure conditions. There are three parameters which determine the actual dose experienced by the photoresist:

- angle of incidence of the laser beam
- the reflectivity of the top surface of the resist
- the reflectivity of the bottom surface of the resist

As schematically illustrated in Figure 19, the power density on the substrate surface in case of oblique incidence is lower than that of normal incidence because of the exposed area by the laser is larger by oblique exposure. It can be deduced that for smaller structure period longer exposure times are required, because the incident angle for smaller period is larger than that for larger period.

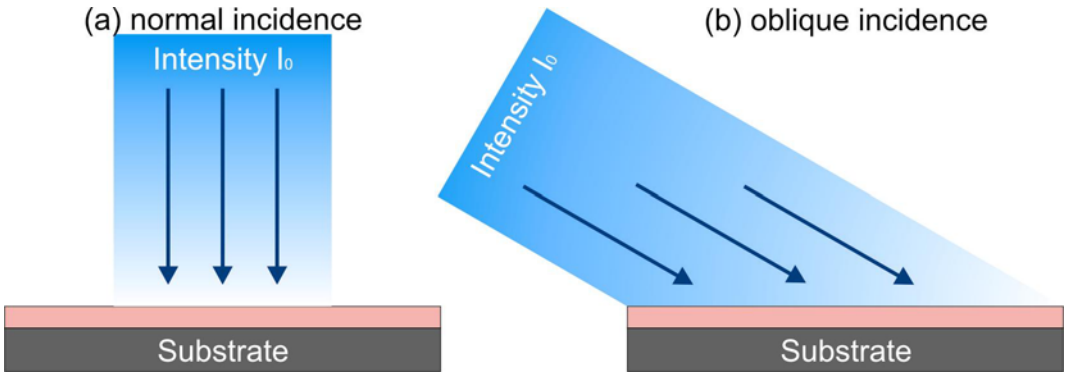

Figure 19: For fixed laser intensity, the power density on a substrate will be highest at normal incidence. The substrate area illuminated by the laser will be larger at oblique incidence angles.

In addition, the energy reflected off the substrate surface (R_1) should be also considered into the reduction of the effective exposure dose, while the reflectivity at the lower surface (R_2) will increase the effective intensity. It is apparent that both R_1 and R_2 depend on the incident angle. These effects are schematically illustrated in Figure 20.

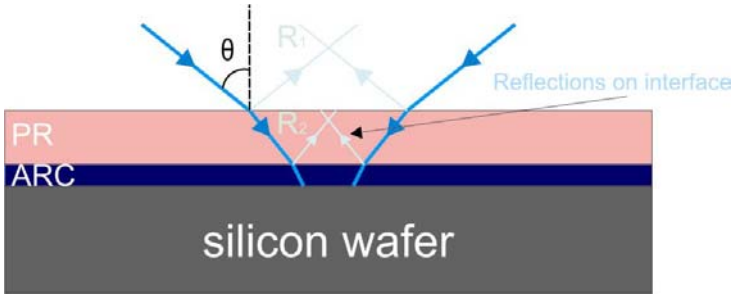

Figure 20: Schematic illustration of the light reflection on the interface.

Summarized above, the concept of the "equivalent-dose" [25] ($D_{equivalent}$) is always employed for the description of the effective exposure dose in LIL technique. The incident angle θ, reflections on the top surface and interfaces are all considered in this concept (Equation 2.10 [25]). As introduced in section 2.3.4, the reflections on the

interfaces R_2, which can damage the structure profile, have been minimized to <3% by using an ARC layer, thus it could be ignored in this case. The dominated factors, which affect $D_{equivalent}$, are the incident angle and the reflectivity on the PR top surface; thereby affecting the duty-cycle.

$$D_{equivalent} = D_{incident}\left[(1-R_1)(1+R_2)\cos(\theta)\right] \qquad \text{Equation 2.10}$$

2.4.1.2 DUTY-CYCLE TO EXPOSURE TIME

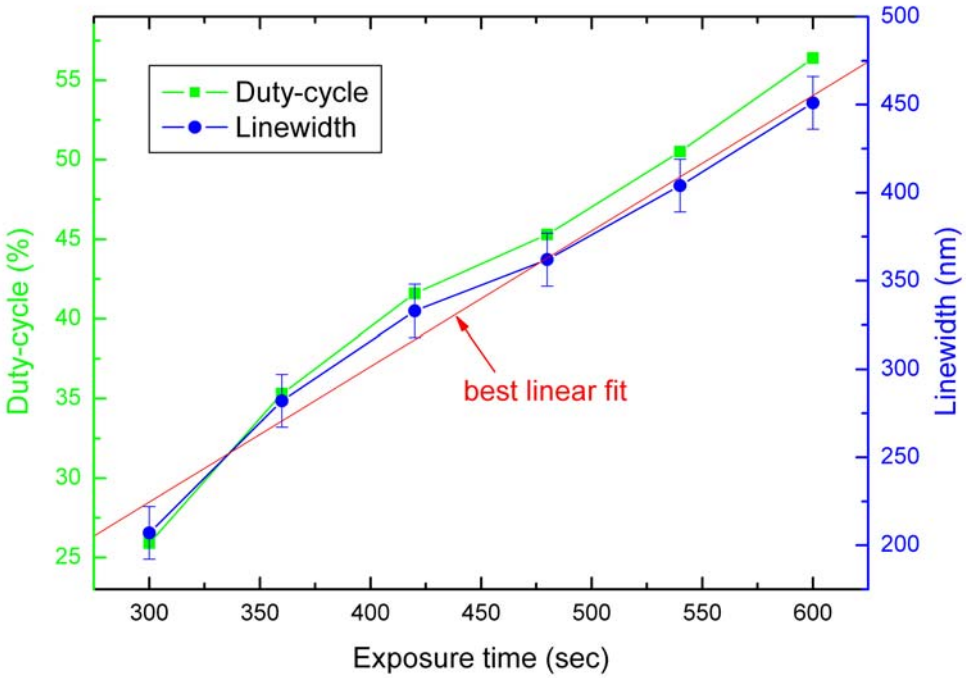

Figure 21: Duty-cycle as a function of exposure time for 800 nm period gratings structure.

The famous Burns-Roscoe reciprocity relation has pointed out: the resist responds equally to high-intensity over short times and low-intensity over long times. It can be deduced that the intensity and exposure time are the most important parameters which can influence the exposure result. For the LIL exposure, it is obvious that there is a linear relationship between equivalent dose and exposure time. To control the DC value, the most direct way is to vary the exposure time at a fixed incident angle. Systematic

investigations have been performed in this work in order to calibrate the resist response: silicon substrates coated with 70 nm thick WiDE-8B ARC and 180 nm thick negative resist TSMR-iN027 have been exposed for various times at 800 nm period. As shown in Figure 21, considering the influences of the misnomer of the SEM measurements, the line width and therefore the duty-cycle increase quasi-linearly by increasing exposure times.

2.4.1.3 DUTY-CYCLE TO POSTBAKE TEMPERATURE

Besides the incident angle and the exposure time, another parameter which can strongly affect the DC value is the postbake temperature (T_{PB}). As schematically illustrated in Figure 22, e.g. for negative resist, if we increase the T_{PB} value, the threshold value of the resist D_{clip} will be decreased. Therefore, the width of the effectively exposed region becomes wider, while the space between two adjacent exposed regions becomes narrower. The DC value increases thereby.

Systematic experiments were performed in this work to investigate the relationship between DC value and T_{PB}. A sample was exposed at 800 nm period and broken into 6 pieces for different T_{PB} ranging from 100 to 110 °C. The results are shown in Figure 23: for negative PR, the DC value increases by higher T_{PB}. The line width/DC value varied from 207 nm/25.8% to 451 nm/56.3% within this 10 °C interval of T_{PB}.

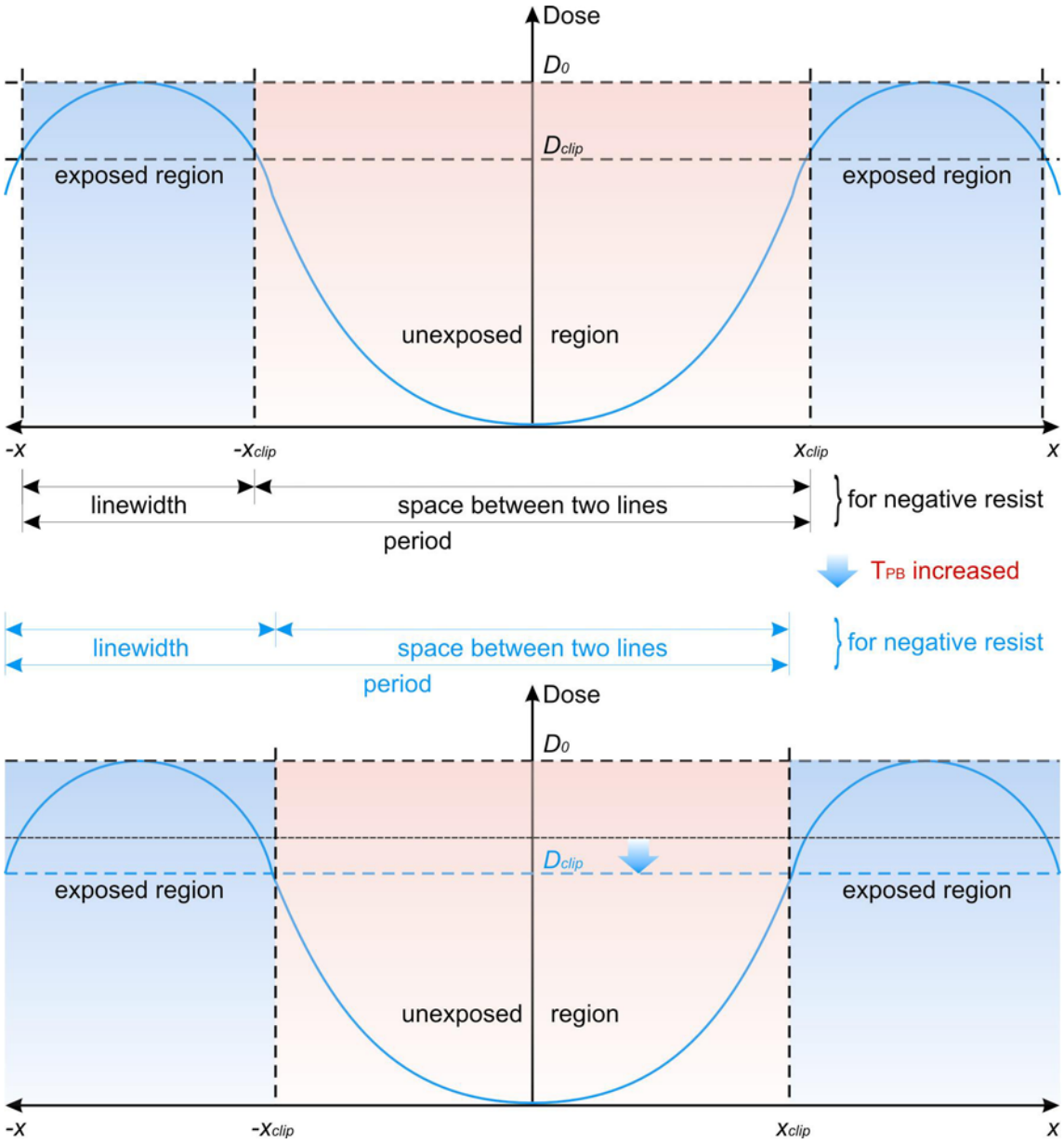

Figure 22: Schematic illustration of the influence of T_{PB} on the threshold value of the resist and therefore on the duty-cycle of the exposure results.

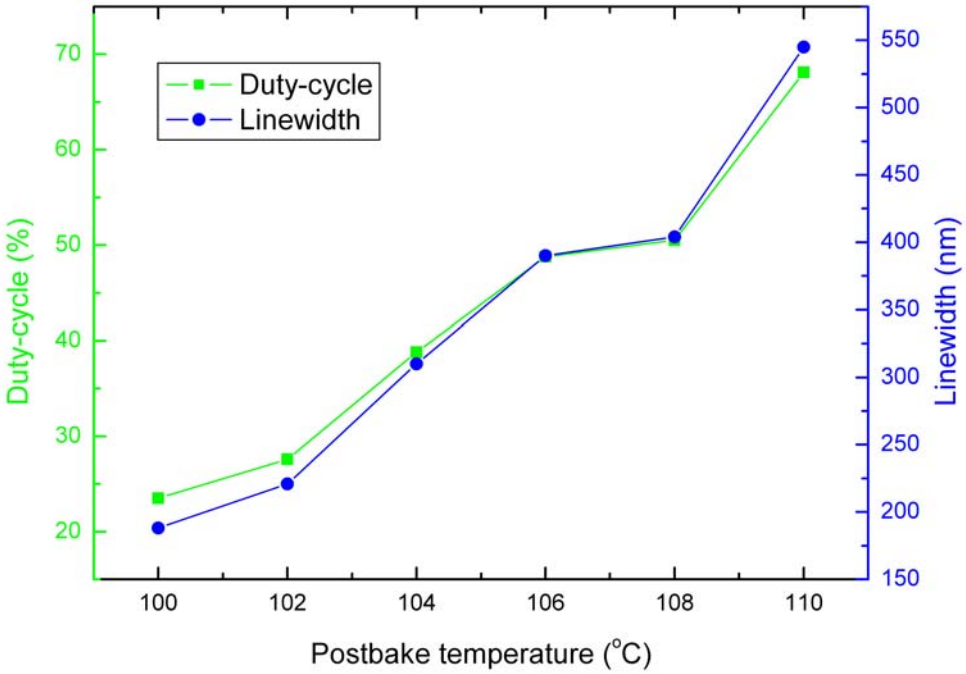

Figure 23: Duty-cycle as a function of post-bake temperature for 800 nm period gratings structure.

2.4.2 EXPOSURE ASPECTS: SIMULATION AND EXPOSURE RESULTS

For LIL exposures with our Lloyd's-Mirror Interferometer, a single exposure forms a grating structure with a certain period. Furthermore, patterns with cubic, hexagonal or another arrangement are made by double exposure with the sample rotated by 90°, 60° or a certain angle between the exposures, respectively. [15] However, circular dot or anti-dot arrays are only available by cubic arrangement, while patterns with another arrangement show elliptical shape with different aspect ratios (long axis: short axis). The shape or the aspect ratio and the arrangement of the structures are determined by the rotation angle between the two exposures. From the other aspect, they are also determined by the exposure dose distribution over the substrate surface. Typical exposure aspects have been simulated with the software "Mathematica" and are shown in Figure 24. Figure 25 shows representative SEM micrographs of LIL exposure results. For double exposure, hole arrays are formed when DC value is <50%, while dot arrays are obtained when DC >50%.

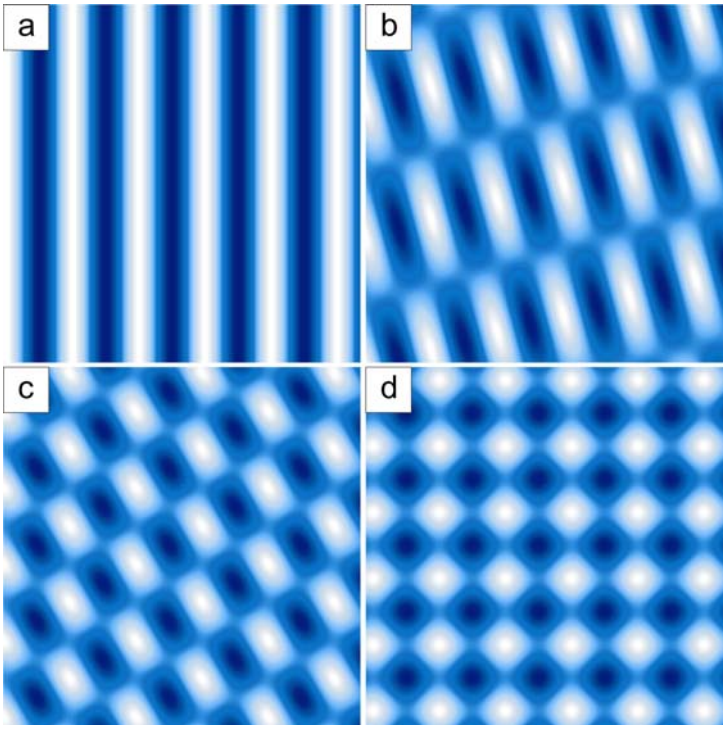

Figure 24: Simulated exposure intensity distribution of (a) single exposure, (b), (c) and (d) double exposure with sample rotation by 30°, 60° and 90°, respectively.

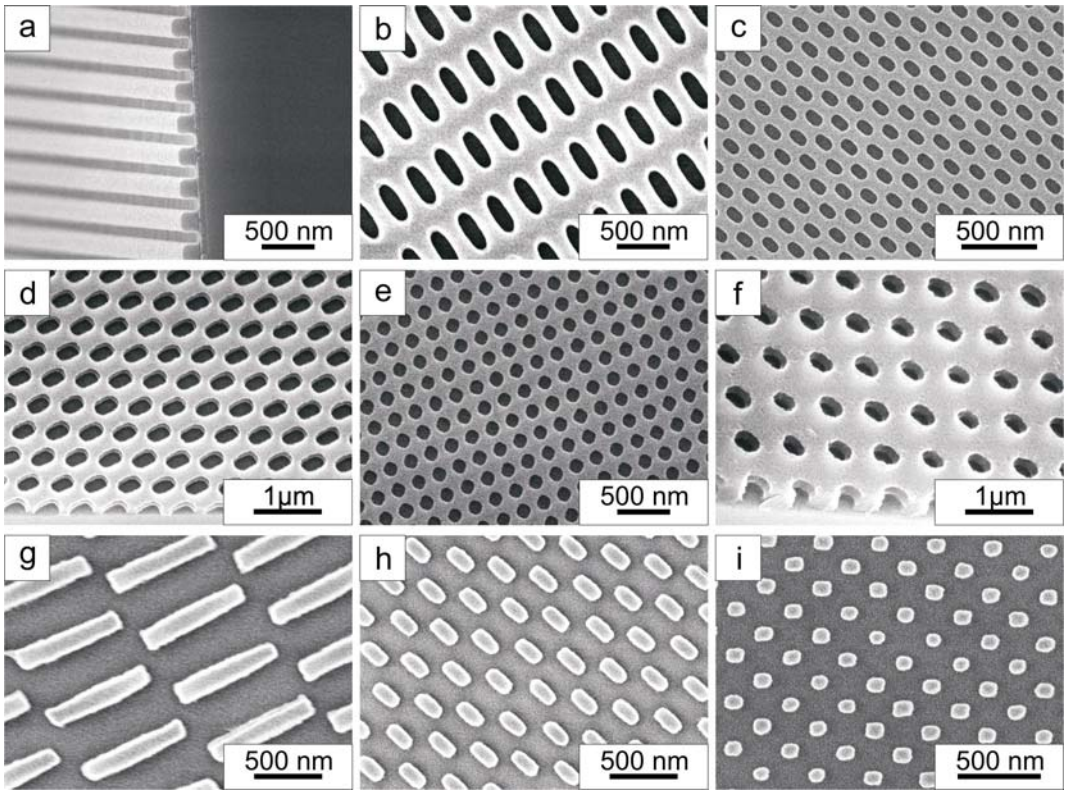

Figure 25: Representative SEM micrographs of LIL exposure results in photoresist layer.

2.5 STRUCTURE TRANSFER

2.5.1 REACTIVE ION ETCHING (RIE)

After LIL patterning of polymers (PR and/or ARC), the large-scale periodic structures are usually transferred into a suitable functional substrate for further applications. Reactive ion etching (RIE) [1,2,26] is a most common structure transfer technique in semiconductor industry. During the RIE process, reactive gases are used as atmosphere in sputter etching. Cations are produced from the reactive gases, which are accelerated with high energy to the substrate and as well can react chemically with the substrate material. From the reactive gas ions and reactive neutral particles are formed that support the etching process. Choosing adequate etching gases and excitation conditions, RIE combines the specific advantages of plasma etching (high selectivity) and of sputter etching (anisotropic removal). Compared with the wet-chemical etching methods, RIE provides the conveniences of high resolution and anisotropy, which is independent of crystal orientation.

After LIL patterning of polymers (PR and/or ARC), the large-scale periodic structures are usually transferred into a suitable functional substrate for further applications. In this work, a RIE machine of Sentech SI220 with a fluorine-chamber is employed for Ar^+-bombardment and the reactive ion etching of silicon, SiO_2, Si_3N_4 and polymers. The principle and the appearance of the machine are illustrated in Figure 26 schematically. The etching recipes are controlled by computer with user-friendly software. The etchings with chlorine gases are performed with an ICP-RIE machine in the clean-room in our institute. The RIE recipes used in this work are listed in Table 2.2. The etching rate depends on the etching gases, flow rate of the gases, HF power and chamber pressure.

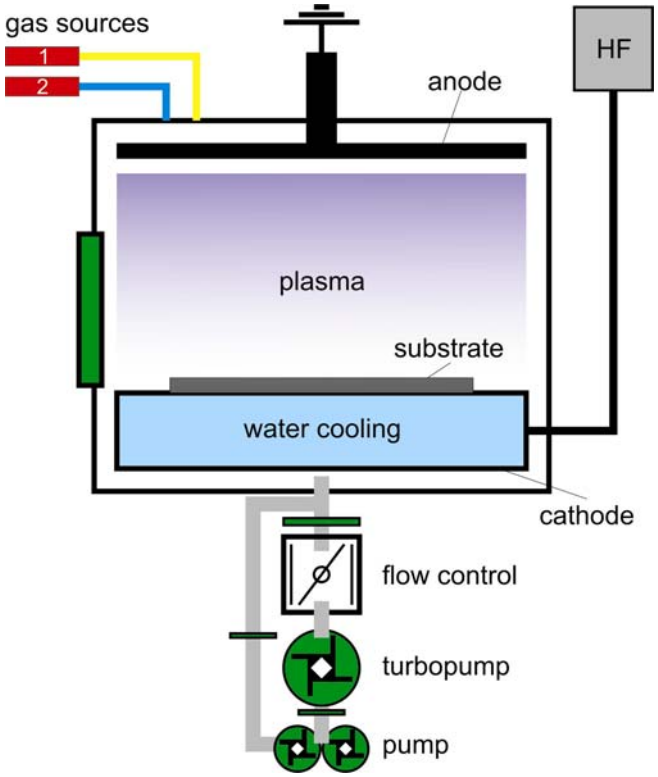

Figure 26: Schematic illustration of the principle of a RIE machine.

Table 2.2 RIE etching recipes

Material	Etchant	Comments
PR & ARC	O_2	For the removal of residual PR or opening of ARC layer
SiO_2	CHF_3	Fluorine, polymer mask
Si_3N_4	CHF_3	Fluorine, polymer mask
silicon	SF_6	Fluorine, SiO_2 mask
	Cl_2	chlorine, polymer mask
aluminium	$BCl_3/CH_4/Cl_2$	Chlorine

Al_2O_3	Cl_2/Ar	Chlorine
TiO_2	CF_4	Fluorine
chromium	O_2/Cl_2	Chlorine
	Cl_2	Chlorine

2.5.2 SiO_2 INTERLAYER FOR RIE

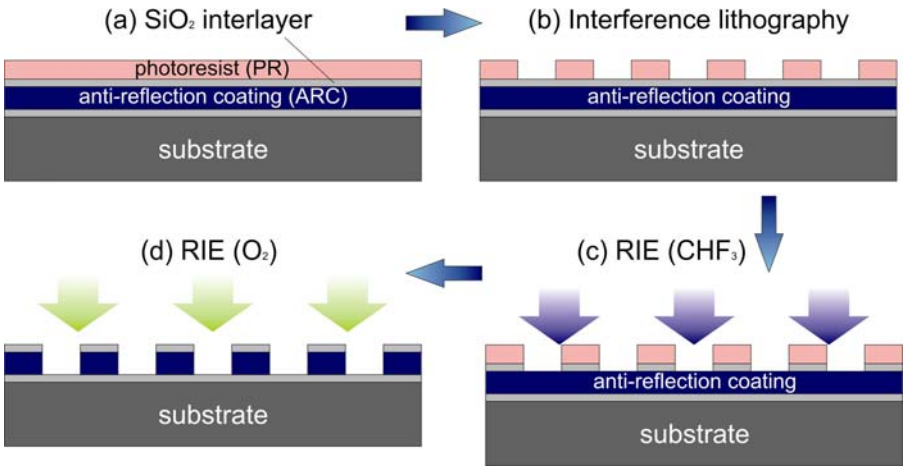

Figure 27: Schematic illustration of the use SiO_2 interlayer for structure transfer through the non-wet-developable ARC layer. (a) The stack design with SiO_2 interlayer; (b) LIL patterning of the PR; (c) RIE of the SiO_2 interlayer with CHF_3 gas; (d) opening of the ARC layer by RIE with O_2 plasma.

For the exposure of smaller structures (period < 300 nm) we have to use standard ARC with non-wet-developable properties. In this case, the structure transfer from PR structures through ARC layer can not be selectively etched with O_2-plasma. Usually, the PR layer is etched also faster than the ARC layer, therefore the PR structures generated by LIL can not be transferred into the substrate directly.

In this work, a SiO_2 interlayer [25] is deposited between PR and ARC before the LIL exposures. The PR structures were firstly transferred into the SiO_2 interlayer by RIE with CHF_3 plasma. The patterned SiO_2 interlayer was used as a mask to open the ARC

layer with O_2-plasma and the structures can be transferred into the substrate subsequently. Due to the imperfect anisotropy of the O_2-plasma etching of the ARC layer, a widening of the ARC structures comparing to the SiO_2 mask occurred. This profile is very suitable for a lift-off process for the fabrication of dot arrays.

2.5.3 ANISOTROPIC KOH ETCHING OF SILICON

Wet anisotropic silicon etching [27~31] is a well-established technology and one of the most important processes in the realization of micromechanical structures in IC industrial productions. In combination with LIL technology, large-area perfectly ordered V-grooves in (100) silicon and U-grooves in (110) silicon are simply available. The LIL patterned polymer or SiO_2/Si_3N_4 layers can serve as a mask for the further wet or dry etchings into the substrate. KOH is the common anisotropic wet etchant for silicon. During KOH etching, the rates of different crystal planes can differ by a factor of 200. Silicon (100) planes could be fast etched in KOH solution, whereas the etching rate of (111) planes are very low. Thus the (111) planes could be considered as etching stop in KOH etchings. With different crystalline orientation of silicon substrates, large variety of shapes could be produced, such as grating and inverse pyramid structures (schematically illustrated in Figure 28). The as-prepared nanostructures have smooth side-walls on an atomic scale, which is unavailable by RIE methods. The applications of the inverse pyramids and grating structures obtained by LIL-tailored anisotropic KOH etching will be introduced in Chapter 4 and 5, respectively.

In this work, typically 40 wt% KOH solution was used to perform the etching of the above introduced structures. Usually an ultra-sonic assistance was employed during the KOH etching of nanometer-scale structures in order to improve the infiltration of the structures and remove associated gas bubbles which could block the etching process. The main features of the etchant are listed in Table 2.3.

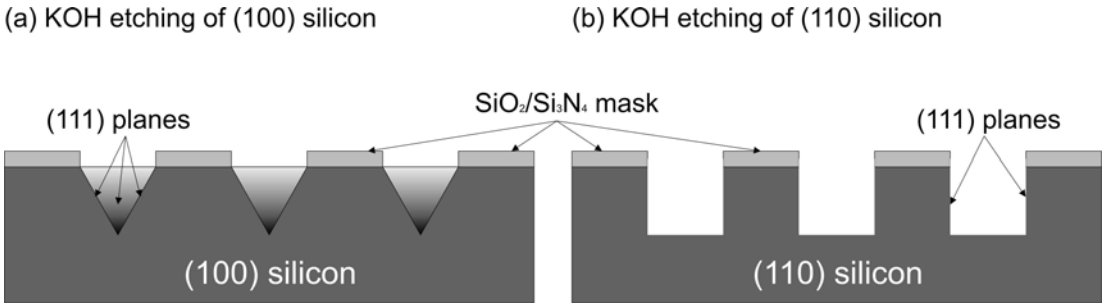

Figure 28: Orientation of structures relative to wafer crystal planes for the anisotropic KOH etching: (a) inverse pyramid structures formed in (100) silicon; (b) grating structure formed in (110) silicon.

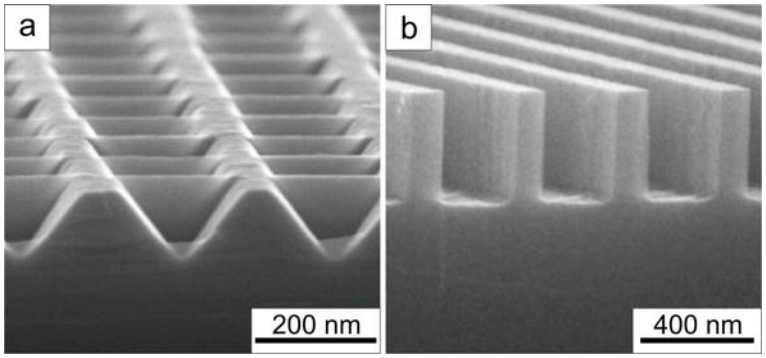

Figure 29: SEM micrographs of KOH etched structure in (a) (100) and (b) (110) silicon substrates.

Table 2.3 Main features of the anisotropic KOH etching.

Etchant	KOH: H_2O: isopropanol at a weight ratio of 2:2:1
Etching rate (@ 80 °C) μ/min	1
Selectivity (100): (111)	200:1
Selectivity (100) Si: SiO_2	200:1
Selectivity (100) Si: Si_3N_4	2000:1

3 TEMPLATED FABRICATION OF NANORING ARRAYS BASED ON LIL

Nanorings, artificial nanoscale clusters, have recently attracted considerable attention both theoretically and experimentally. Lithographically defined arrays of metallic or semiconductor nanorings are particularly interesting for applications due to their unique magnetic, [32~47] optical [48] or electrical properties.

For example, for the application in data storage devices, magnetic memory devices based on flux-closure magnets were first introduced during the early 1950s. [49] These non-volatile devices used macroscopic ring-shaped ferrite magnets connected in a grid using Ni wires, and bits of information are stored by magnetizing each ring structure clockwise or counterclockwise. The most modern version of magnetic storage is Magnetic random access memory (MRAM). Recently, beyond elongated or bar-shaped elements, high density MRAM devices based on ring-shaped magnetoresistive elements have been proposed. [50] In the last three years, much attention has been drawn towards elliptical magnetic rings [44~47] with an in-plane magnetic anisotropy. Due to the existence of more than two stable magnetic states in an elliptical magnetic nanoring structure, more than one bit to be stored in each element is allowed, for potential application in novel elliptical-ring-shaped MRAM devices.

Motivated by the application potential, efforts to construct mesoscopic nanorings have led researchers to explore and develop a variety of fabrication methods. Conventional lithography techniques such as optical lithography and EBL are limited in spatial resolution and writing speed, respectively. Alternatively, low-cost template-based synthesis approaches for ring-shaped nanostructures have been developed very recently. Nanosphere lithography [51~55] and nanoporous templates [56~59] have been employed for the fabrication of nanoring arrays.

In case of nanosphere lithography for nanoring arrays, usually self-assembled polymeric or silica nanospheres or nanoparticles are positioned on planar substrate. Metallic thin

films are subsequently deposited onto the nanospheres. Metallic nanorings are obtained by perpendicular ion-beam bombardment and chemical removal of the nanospheres. However, the arrangement of the thus obtained nanorings is often random, or ordered only in small areas when self-ordering strategies are applied for the nanosphere assembly.

Membrane structures were also utilized for the fabrication of nanoring arrays such as porous anodic aluminium oxide (AAO) [56~58] and nanochannel glass (NCG). [59] They are scalable and suitable for the large-area fabrication of arrays of circular-shaped nanorings. However, the template preparation is cost- and time-consuming. Moreover, fabrication of elliptical nanoring arrays is not possible with these templates.

As an alternative approach a templated deposition method of perfectly ordered nanoring arrays based on LIL will be introduced in this chapter. These templates with perfectly ordered hole array structures were fabricated by LIL exposures and structure transfer techniques. Electrochemical deposition and atomic layer deposition (ALD) were employed for the deposition of ring materials. In section 3.1, two novel methods for the electrodeposition of metallic nanoring or nanowire arrays on patterned highly doped silicon templates and sacrificial Cr layer electrode are discussed, respectively. The nanoring arrays generated by ALD and subsequent perpendicular Ar^+ sputtering are introduced in section 3.2.

3.1 ELECTROCHEMICAL DEPOSITION OF NANORING AND NANOWIRE ARRAYS

3.1.1 TEMPLATED ELECTROCHEMICAL DEPOSITION

Electrochemical deposition combined with resist patterning techniques provides a powerful tool for the fabrication of micro- and nanostructures. Although in the IC industry, one tends to avoid wet chemistry, both IC and micromachining needs are forcing reconsideration of electrochemical deposition as a viable solution. Nowadays, the electrochemical deposition based LIGA [60] process is a standard technique for the fabrication of micro devices. The principle of templated electrochemical deposition

(ECD) [61~67] is the selective electrodeposition of metals or semiconductors on a conductive seed layer through openings in an insulating mask. This deposition technique is characterized by a very high fidelity to the mask.

Penner *et al.* have recently reported a fabrication approach for lateral nanowire arrays, combined templated electrodeposition technique and edge lithography strategy, called electrochemical step edge decoration (ESED). [68~71] Highly oriented pyrolytic graphite (HOPG) was used as a template substrate for electrochemical deposition of hemicylindrical nanowires on the atomic step edges with diameters ranging from 10 nm to 1 μm. Due to the potential difference on the step edges, the highest deposition rate of metals occurs at the step edges during the electrodeposition process. However, the step edges of HOPG substrate are not perfectly aligned; therefore electrodeposition of perfectly ordered nanowire arrays is not feasible. Furthermore, deposition of nanoparticles occurs frequently on the graphite terraces.

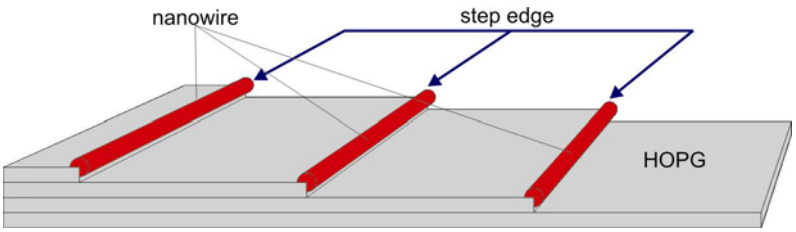

Figure 30: Schematic illustration of electrochemical step edge decoration (ESED).

3.1.2 PATTERNED HIGHLY DOPED Si TEMPLATE

In this work, a large-area fabrication technique for ideally ordered lateral metallic nanowire or nanoring arrays over wafer-scale areas on highly doped silicon substrate has been developed. This approach is based on the generation of Si_3N_4 nanohole arrays or grating structures on silicon wafers by LIL and the selective electrochemical deposition on the step edges of periodic Si_3N_4 patterns.

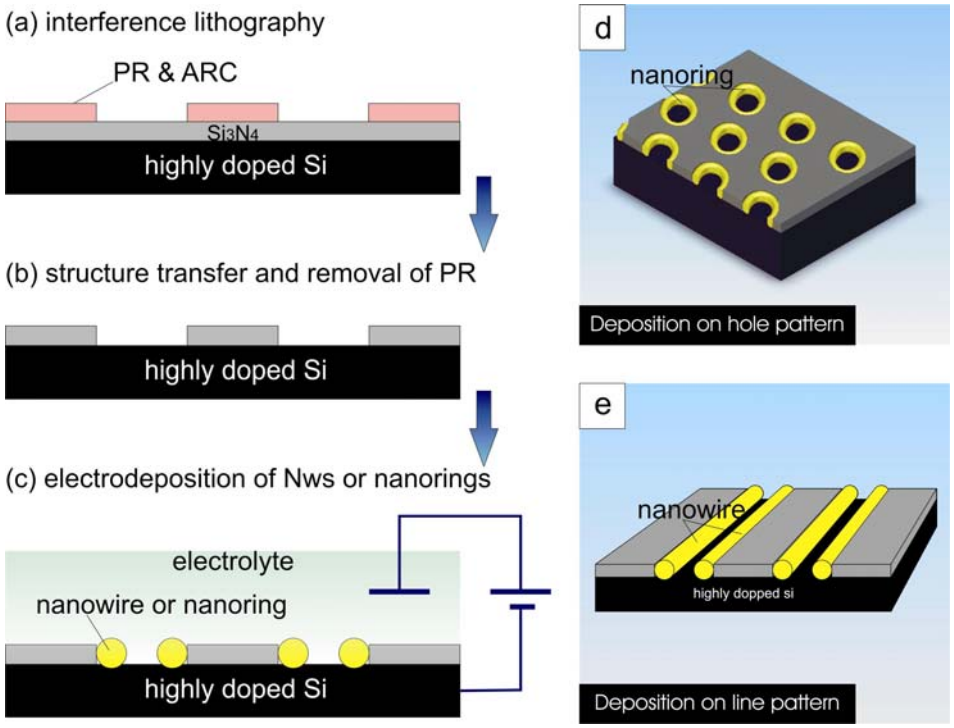

Figure 31: Schematic illustration of lithographically guided electrodeposition of ideally ordered metallic nanowire or nanoring arrays on a highly doped silicon substrate. (a) LIL patterning of PR and ARC on the substrate; (b) pattern transfer through the underlined Si_3N_4 and into the highly doped silicon substrate by RIE with CHF_3 gas, removal of the remaining polymer with O_2 plasma, and subsequent treatment of the substrate with 5% HF solution; (c) selective electrodeposition of metal along the step edges; (d) nanoring array deposited on the substrate with hole patterns; (e) nanowire array deposited on line patterns.

Figure 31 (a-c) schematically illustrated the fabrication procedure. PR and ARC on highly doped silicon (resistivity ca. 0.01-0.02 Ω-cm) wafer covered with a 35 nm thick Si_3N_4 layer were first patterned by LIL into periodic lines or holes patterns. The polymer (PR and ARC) structures generated by LIL served as etching masks for an anisotropic RIE through the Si_3N_4 layer and they were also overetched into the Si substrate. After the pattern transfer process the remaining polymer resists were removed by O_2 plasma, which also leads to the formation of silicon oxide in the opened parts. Prior to the electrodeposition process, the sample was treated with 5% HF solution for 90 sec to remove partly the thin oxide layer at the step edges caused by native oxidation or O_2 plasma treatment. Subsequently, the silicon substrate with the Si_3N_4 pattern was utilized as the working cathode for the electrochemical deposition of metals. The insulating layer of Si_3N_4 on the mesas and the native oxide layer in the valleys ensured

that the electrochemical deposition of metal occurred exclusively on the etched undercuts of the patterns and not everywhere on the top surface of the template. The current density was adjusted according to the area and structure density of the templates. In the present method, on samples with hole (Figure 31d) and line patterns (Figure 31e), arrays of nanorings and nanowires were obtained, respectively.

With this novel approach, the thickness of the nanoring/nanowire in cross-section could be controlled by monitoring the amount of total integrated charges involved in the electrochemical reaction, i.e. the current density and the deposition time. The shape and the arrangement of the nanorings/nanowires could be controlled by the LIL patterning process. Typically, feature sizes ranging from 50 to 300 nm and nanorings with different aspect ratios in shape can be obtained by our approach.

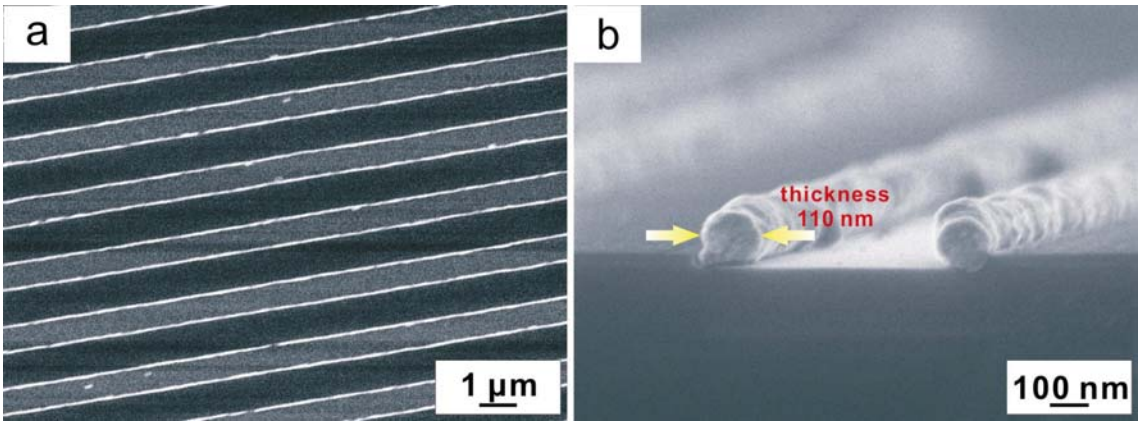

Figure 32: SEM images of Au nanowire array with a wire diameter of 110 nm in (a) top-view and (b) cross-section view.

Fabrication of nanowire arrays by using substrates with lines patterns has also been demonstrated (Figure 32). Arrays of ideally ordered metal nanowires on Si substrates of several centimeters were realized in our experiments. In comparison with the ESED method, in our approach the arrangement of the nanowires can be varied over a broad range and the length of the nanowires can be extended over a whole wafer. In addition, it is worth noting that in each groove, two parallel nanowires were deposited on both edges. This enables us to achieve nanowire arrays with half of the periodicity of LIL-defined pattern.

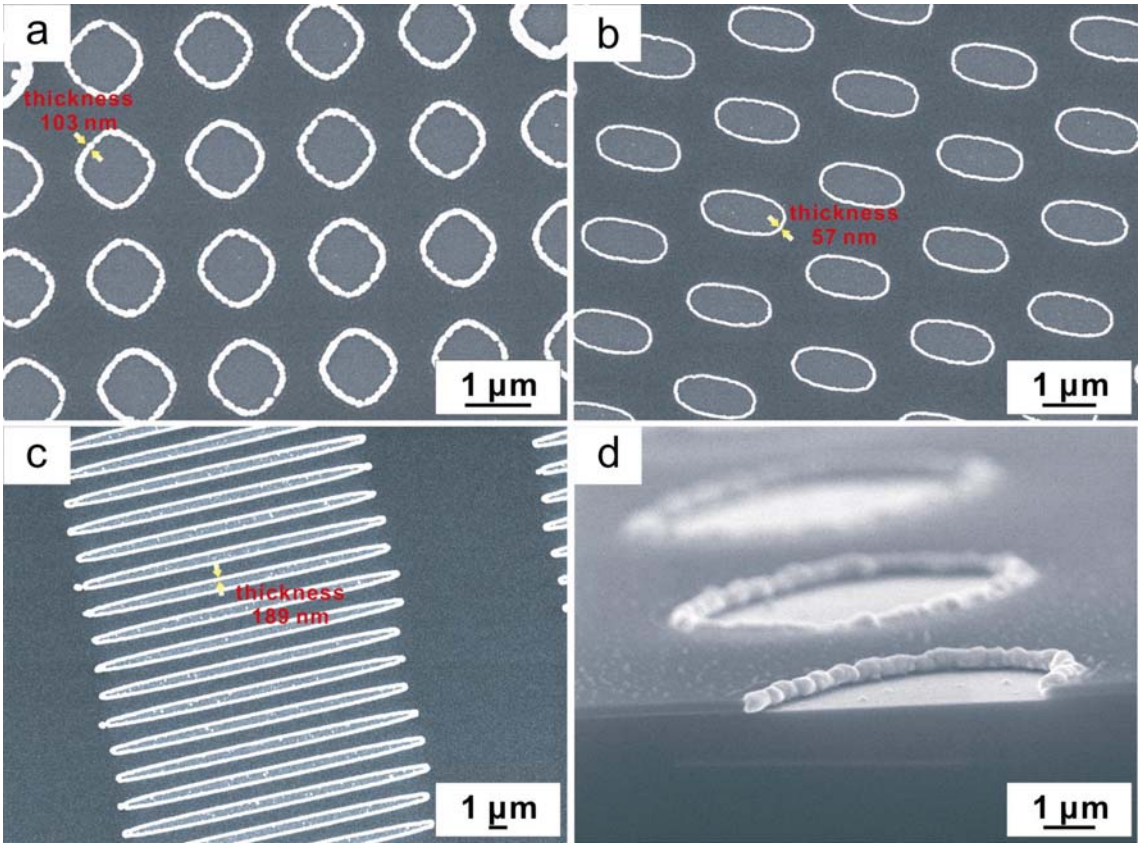

Figure 33: Representative SEM images of arrays of Au nanorings with different geometries. (a) Circular ring array; (b) hexagonally arranged elliptical ring array in top view and (d) in cross-section view; (c) elliptical ring array.

Figure 33 shows representative SEM images of Au nanoring arrays with different feature sizes and aspect ratios in top- and cross-section views. Figure 33a shows an array of circular-shaped rings, which have a wire thickness of 103 nm, a ring inner diameter of 1070 nm and a 1300 nm periodicity. Figure 33b and d are top- and oblique-views showing a hexagonal array of elliptical rings with a wire diameter of 57 nm, a long-axis diameter of 1250 nm, a short-axis diameter of 680 nm and a center-to-center spacing of 1330 nm. Figure 33c demonstrates elliptical rings with high aspect ratio (11:1 in long-axis:short-axis) and a wire diameter of 189 nm.

In order to investigate the mechanisms of the selective deposition on the undercuts of the structures, TEM specimens of the topographic profile of the sample shown in Figure 33b has been prepared and images have been taken with a Phillips CM 20 STEM. The cross-section of the silicon substrate, the step edges and the gold nanowires can be seen

in Figure 34a. Detailed information and corresponding schematic illustrations are shown in Figure 34b. In the pattern-transfer step, a RIE recipe of CHF_3 plasma with 30 sccm, 10 mTorr (1 Torr=133.3 Pa), -320 V) has been performed. As can be seen from the TEM image, it is apparent that the Si_3N_4 layer was opened and the pattern was successfully transferred into the underlying highly doped silicon substrate by the RIE. An undercut of about 9 nm was formed in the silicon substrate.

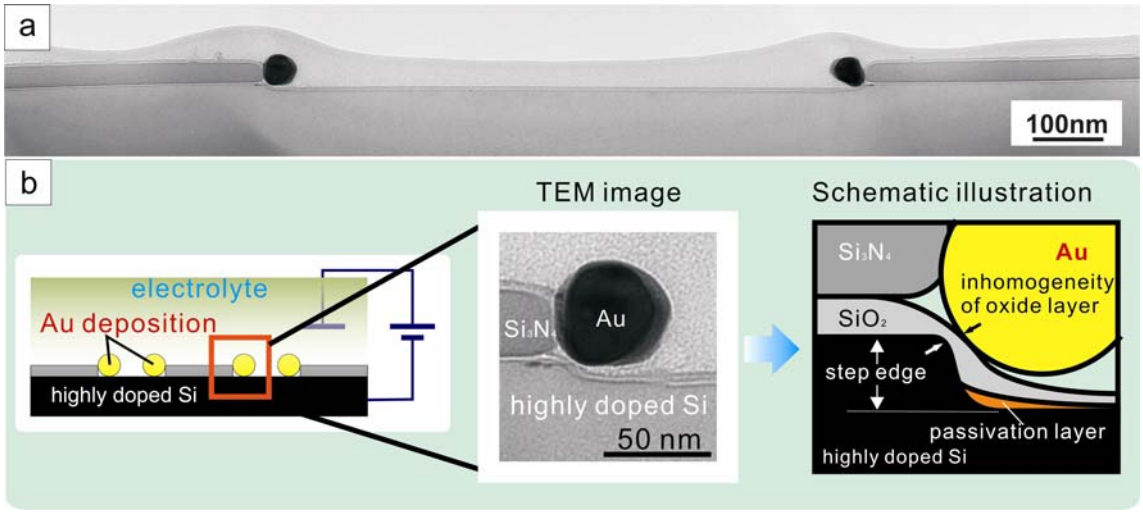

Figure 34: (a) TEM image of an Au nanoring on the substrate showed in Figure 33b in cross-section view; (b) magnified-view of (a) and the corresponding schematic illustrations.

As in case of ESED, nucleation of metal occurs preferentially along the step edges at the initial stage of electrodeposition because the electrical field is focused on the edges due to the geometric effect. [68~71] It is believed that the electrical charges were also focused onto the undercuts, reducing metal ions at the step edges in our case (Figure 35).

It is also believed that the inhomogeneity of the thickness of the native oxide layer plays an important role in the selective deposition of metal along the step edges (Figure 36). We assume that the native oxide layer, which can block the electrodeposition, at the shoulder of the step edge is thinner than that on the terrace. In order to get an insight into this phenomenon, systematic experiments were performed by electrodepositing gold on patterned substrates that were etched by using 5% HF solution for different periods of time prior to the deposition (Figure 36). For the substrate etched for 90 sec, the metal deposition occurred only along the step edges and metallic ring structures

were successfully formed. Whereas electrodeposition on the substrate etched for 120 sec results in a high density of metallic dots on the Si valley surfaces.

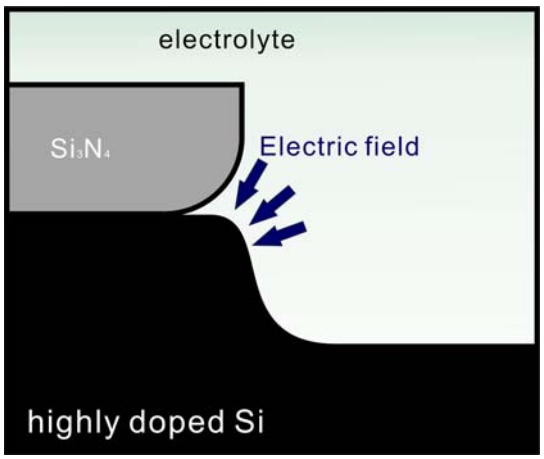

Figure 35: Schematic illustration of focusing of the electric field on the overetched undercut due to geometric effect during the electrodeposition.

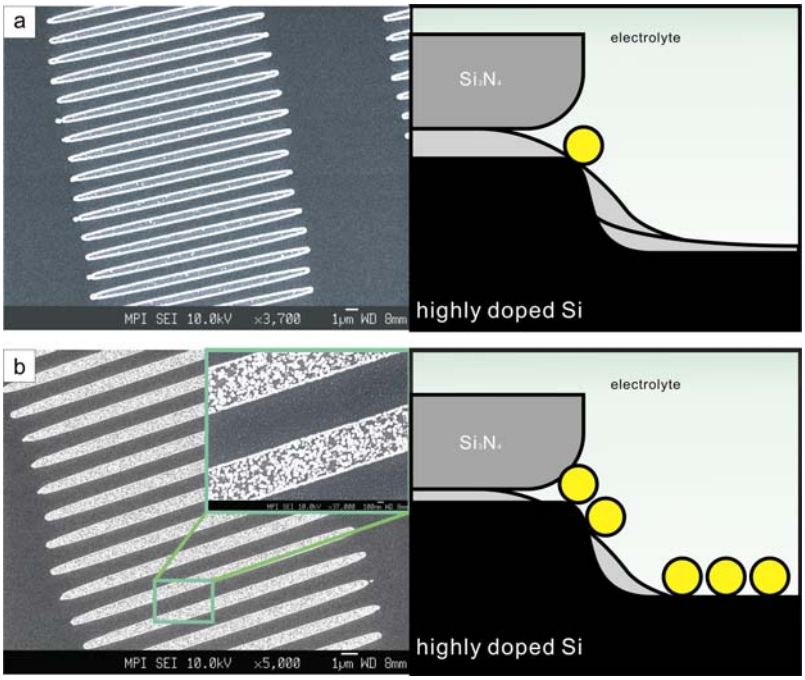

Figure 36: SEM micrographs and the corresponding schematic illustrations of the effect of HF treatment on the deposition results. (a) Successfully selective metal deposition; (b) granular gold films on the patterned Si substrates. Before electroplating, the samples were treated with 5% HF solution for (a) 90 sec and (b) 120 sec.

The SiO_2 layer along the step edges is preferentially removed by a short HF etching

(<90 sec), whereas the Si valley surfaces were still covered with an oxide layer, i.e., only the step edges were exposed to the electrolyte and the deposition took place there (Figure 36a). After 120 sec HF etching, the oxide layer on the valley surface was also completely removed. As a result, a selective electroplating can not be achieved, and metal deposition could take place on the entire surface uncovered with the Si_3N_4 mask (Figure 36b). As can be seen from the insert of Figure 36b, the density of metal deposition along the step edge is clearly higher than in the Si valley. We can deduce that the topography of the step edges leads to a preferential nucleation during the electrodeposition process, although the oxide layer has been completely removed. The geometric effect produced an energetic disparity for the electrodepostion.

If we summarize the mechanism of the selective electroplating in this work (recall Figure 34b), five major arguments could be considered to positively affect the forming of nanoring and nanowire arrays:

- The resist pattern was transferred into the conductive silicon substrate for 5~10 nm by RIE. The topographic profile induced a preferential nucleation at the step edges;
- During the removal of the polymer by RIE with O_2 plasma, an amorphous passivation layer could be generated in the valleys of the Si substrate, which has the potential to prevent the valley surfaces from direct electrodeposition;
- The inhomogeneity of the oxide layer enables the preferential exposure of the step edges to the electrolyte, which leads to a selective electroplating;
- The strong focusing effect of the electric field at the shoulders of the step edges during the electrodeposition results in selective reduction of metal ions there;
- The electric-field-assisted fast diffusion of metal ions towards the step edges guides strongly the selective deposition.

3.1.3 DEPOSITION OF NANORINGS ON METALLIC ELECTRODES

The major difficulty of the method introduced above is that the etching of the native SiO_2 layer on a highly doped silicon substrate prior to the electrodeposition is difficult to be precisely controlled. Therefore, a second generation of templates with a metallic electrode contact has been developed. Figure 37 schematically illustrates the process of this method in cross-section view. A Cr layer with a thickness of 20 nm was sputtered on a silicon wafer with a 100 nm oxide layer prior to the resist deposition. Desired periodic holes or grating structures were obtained by LIL exposures and subsequently transferred through the Cr layer by RIE with Cl_2 gas. The patterned Cr layer was used as working electrode for the electrodeposition. The Cr layer was recessed in a resist and SiO_2 sandwich, which ensures that the metal deposition occurred only along the exposed edges of Cr layer.

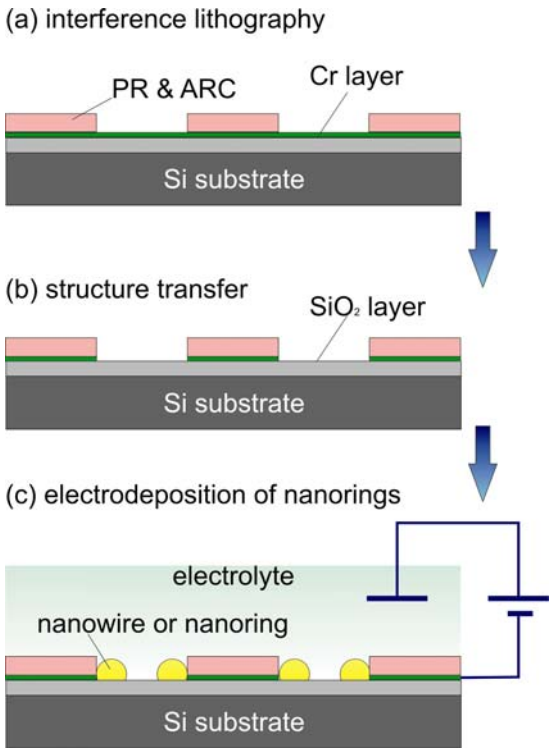

Figure 37: Schematic illustration of electrodeposition of nanoring arrays on sacrificial Cr layer electrode. (a) LIL patterning of the PR and ARC deposited on the substrate; (b) pattern transfer through the buried Cr layer; (c) electrodeposition of metal along the edges of Cr pattern.

Parallel to our work, Penner and his co-workers published a similar method, called lithographically patterned nanowire electrodeposition (LPNE). [72] Nickel was chosen in that case as sacrificial layer for the preparation of a nanoband electrode and the exposed nickel layer was removed locally electrochemically. In our approach, Cr layer has been employed because it is a lithographically compatible material, such as for RIE process, and it will not affect the measurements of magnetic properties of the as-prepared nanoring structures. In comparison to nickel, Cr is much easier to be oxidized, which could block the electrodeposition. Therefore, a HF etching prior to the electrodeposition was performed to remove the native CrO_2 layer on the exposed working electrode.

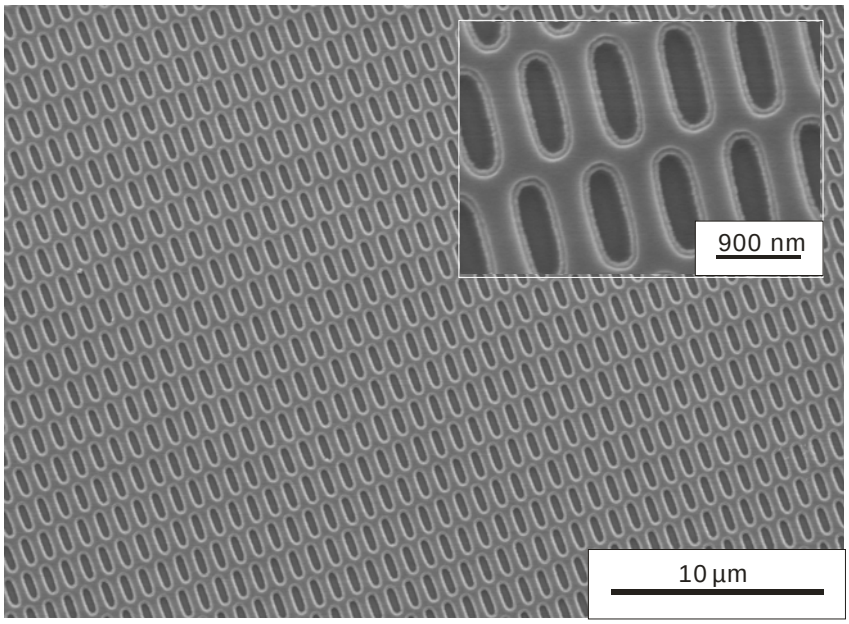

Figure 38: SEM iamge of as-prepared elliptical Ni nanoring array, magnified view is shown as insert.

Figure 38 shows the SEM image of an as-prepared elliptical Ni nanoring array with magnified view as insert. The elliptical rings are hexagonally arranged and have a diameter in the long-axis of 1230 nm and in the short-axis of 400 nm, which gives an aspect ratio of ca. 3.1 (long-axis: short-axis). The center to center distance is about 740 nm and the diameter of the deposited ring-like metal wires is below 60 nm. It is apparent from the SEM image that this approach provides a homogenous deposition of metals along the step edges of resist structures and therefore allows the generation of complex structures, e.g. nanowire arrays. After the deposition of desired materials along the step edges, the photoresist and the sacrificial Cr layer could be selective etched

away by RIE and chemically, respectively. Thus freestanding nanoring or nanowire arrays could be obtained on normal silicon substrates, which will not influence the characterization of the properties of the structures, such as magnetic, electric, optic and thermoelectric properties, etc. Room temperature hysteresis loop measurements of the nanoring arrays shown in Figure 38 were obtained using a SQUID (Superconducting Quantum Interference Device)-Magnetometer. Figure 39 shows the hysteresis loops on applying a magnetic field parallel and perpendicular to the long axis of the elliptical rings, respectively. The long-axis was determined by optical microscopy. On applying a magnetic field parallel to the long-axis, the collective magnetization reversal of the array shows an easy-axis behavior, while applying a field perpendicular to the long-axis displays a hard-axis behavior. The results indicate that the elliptical shape anisotropy dominates the magnetization reversal of this array at room temperature.

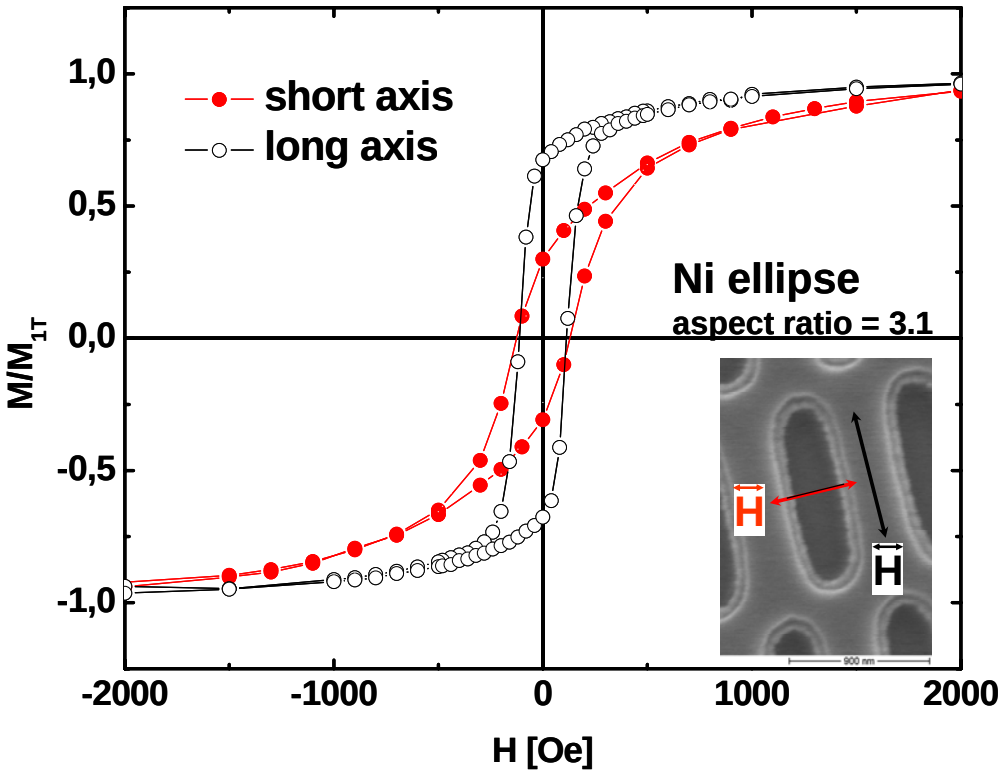

Figure 39: Room temperature hysteresis loop measurements on applying magnetic fields parallel and perpendicular to the long axis of Ni elliptical ring array, respectively.

$Ni_{0.8}Fe_{0.2}$ permalloy nanoring array was also prepared with the same template. Room

temperature hysteresis loops on applying a magnetic field parallel and perpendicular to the long axis of the ellipses have also been measured with a SQUID-Magnetometer. Figure 40 shows the results of measurements of magnetic properties. Both loops display that switching in this ring structures is a complex multistep process rather than a two step process shown in the Ni ring array above. The slanted plateau between transitions and the slope of the transitions suggest that the rings exhibit the vortex and onion state. [46]

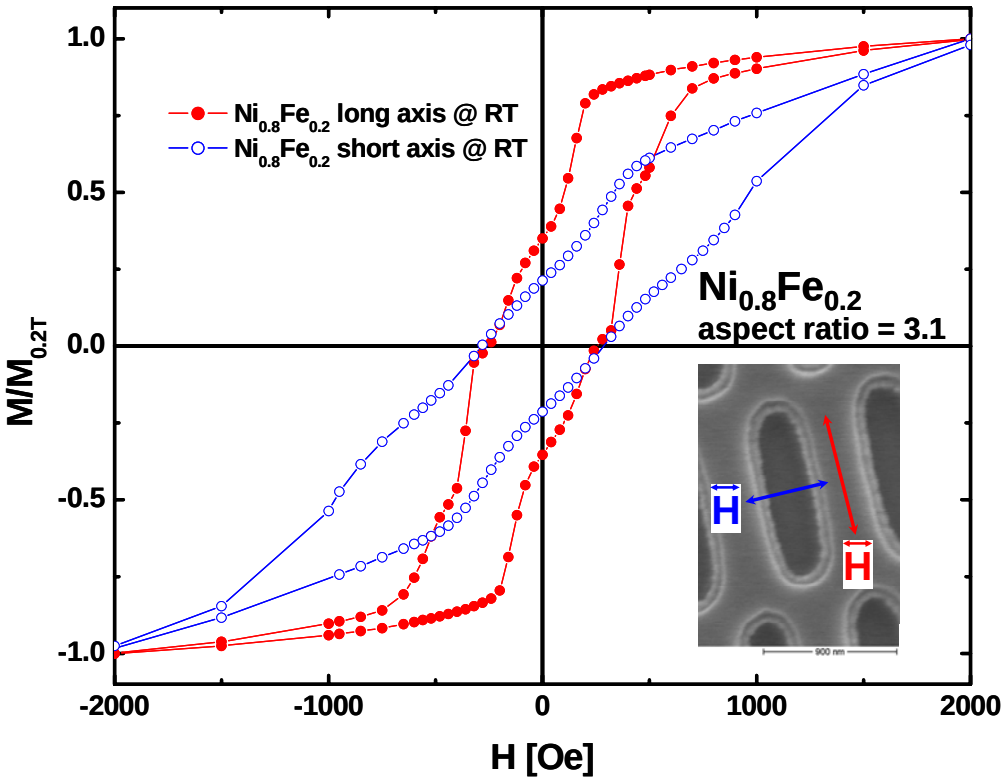

Figure 40: Room temperature hysteresis loop measurements on applying magnetic fields parallel and perpendicular to the long axis of $Ni_{0.8}Fe_{0.2}$ permalloy elliptical ring array, respectively.

Adeyeye *et al*. have reported the spin state evolution and in-plane magnetic anisotropy of elongated $Ni_{0.8}Fe_{0.2}$ nanorings in 2005. [47] They have fabricated permalloy elongated nanorings by using deep UV lithography on a 4x4 mm^2 area and lift-off processes. The room temperature magnetization curve (Figure 41a) of the rings was measured using vibrating sample magnetometer (VSM) and the hysteresis loop of a single ring was simulated (Figure 41b). Both experimental and theoretical results display a number of

transitions in the magnetization states as the applied field is varied from saturation field H_s in one direction to H_s in the other. Compared to their results, our magnetic hysteresis loops (Figure 40) of permalloy elliptical nanoring arrays show similar complexities and magnetic anisotropy. However, our fabrication method provides a better resolution and flexibility.

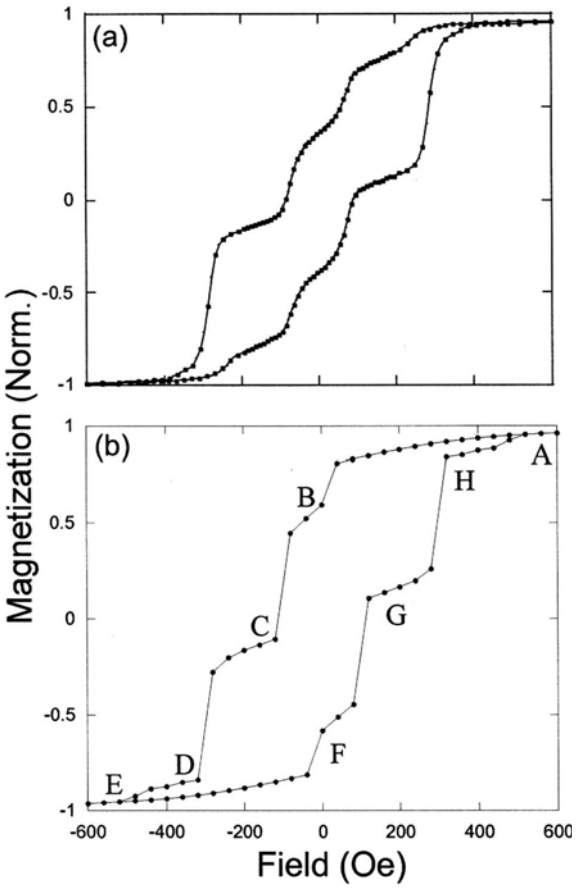

Figure 41: Results from the Ref [47]: (a) Magnetic hysteresis loop of arrays of elongated 30-nm-thick $Ni_{0.8}Fe_{0.2}$ rings when the applied field is along the major axis; (b) simulated hysteresis loop of a single elongated 30-nm-thick $Ni_{0.8}Fe_{0.2}$ ring.

3.2 ATOMIC LAYER DEPOSITION (ALD) OF NANORING ARRAYS

3.2.1 PRINCIPLE OF ALD

Atomic layer deposition (ALD) is a chemical vapour deposition technique for the deposition of materials with extremely precise control over layer thickness down to a fraction of a monolayer. ALD has the capability to coat complex nanostructure surfaces with a conformal material layer of high quality. From a technical point of view, ALD has been defined as a film deposition technique based on the sequential use of self-terminating gas-solid reactions. [73] One ALD reaction cycle is schematically illustrated in Figure 42. A reaction cycle of ALD consists of the following four characteristic steps [73].

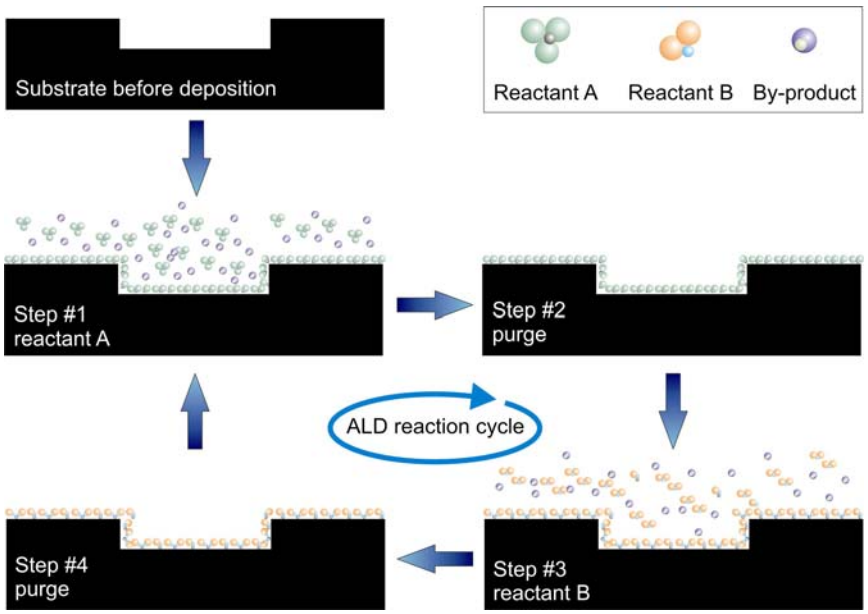

Figure 42: Schematic illustration of one ALD reaction cycle.

- Step #1: A self-terminating reaction of the first reactant (A);
- Step #2: A purge or evacuation step to remove the unreacted reactants and the gaseous reaction by-products;

- Step #3: A self-terminating reaction of the second reactant (B) or another treatment to achieve the surface again for the reaction of reactant A;

- Step #4: A purge or evacuation step.

A certain amount of material is deposited on the surface by each reaction cycle. To grow a material layer, reaction cycles are repeated until the desired thickness of material has been deposited. Because of the surface control, extremely conformal and uniform material coatings are obtained. In this work, TiO_2 and Al_2O_3 deposition have been performed for nanoring (this section) and nanochannel (section 5.3) arrays.

3.2.2 ALD OF NANORING ARRAYS

The fabrication method of nanoring arrays by template based ALD deposition and Ar^+ sputtering is schematically illustrated in Figure 43. The polymer hole array generated by LIL were transferred into the underlying 25 nm thick SiO_2 layer and used as template for the ALD of TiO_2 layer at room temperature (RT). The entire topography of the template was coated with a homogenous TiO_2 layer. Subsequently, a perpendicular Ar^+ bombardment was performed to remove the top- and bottom-parts of the TiO_2 coating and therefore independent TiO_2 nanoring structures were obtained in the polymer holes. Finally the polymers were removed by RIE with O_2 plasma in order to achieve a free-standing TiO_2 nanoring array.

Figure 44 shows the representative SEM micrographs. A template coated with a uniform TiO_2 layer obtained by ALD at RT is presented in Figure 44a. After a perpendicular Ar^+ bombardment, a perfectly square-like arranged circular TiO_2 nanoring array has been achieved. The rings have an inner diameter of 119 nm, a wall thickness of the ring of ~34 nm, and a center-to-center spacing of 370 nm.

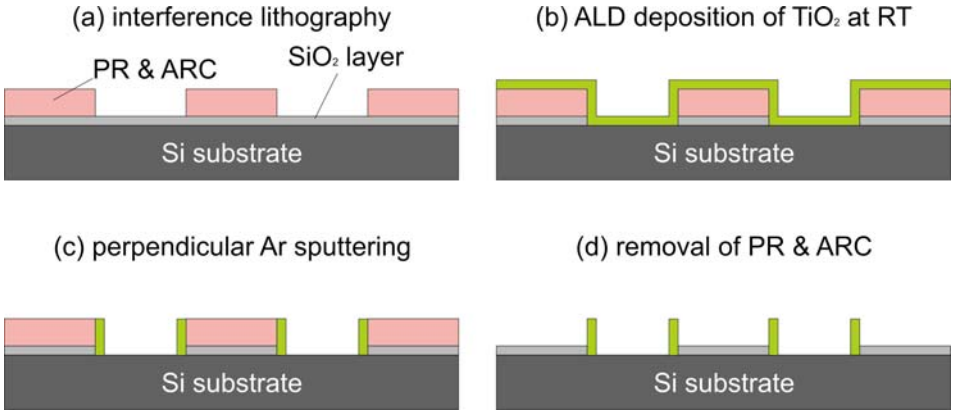

Figure 43: Schematic illustration of fabrication of nanoring arrays by template based ALD of TiO_2 and Ar sputtering. (a) Template with hole array structures was fabricated by means of LIL, and the structures were transferred into the underlying SiO_2 layer by RIE with CHF_3 gas; (b) ALD of TiO_2 layer on the substrate surface at RT; (c) perpendicular Ar^+ sputtering to remove the top- and bottom-parts of the TiO_2 layer; (d) release the separated TiO_2 nanoring arrays from the polymer structures by O_2 plasma RIE.

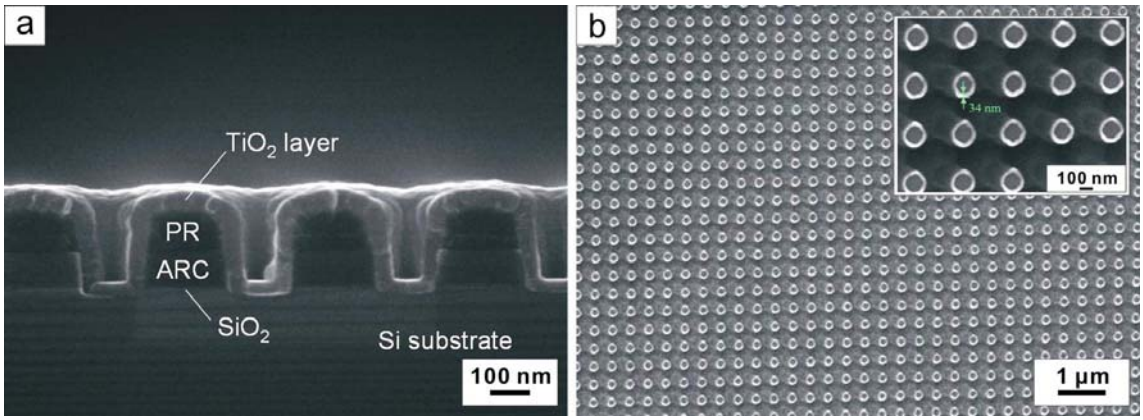

Figure 44: SEM images of (a) cross-section view of a template coated with a uniform TiO_2 layer and (b) top-view of square arranged TiO_2 nanoring array. A magnified view is shown as an insert, the wall thickness of the ring is ~34 nm.

With this method, the diameter, ring-shape and arrangement could be adjusted by the LIL process, which provides a flexible variation of such parameters. The thickness of the wall of the rings could be precisely controlled by varying the number of ALD cycles. However, the Ar^+ bombardment is not suitable for the removal of a very thick layer (>35 nm), otherwise the homogeneity of the surface could not be guaranteed. For a thick ring wall or a multilayered nanoring array, repeating of the process steps from (a) to (c) in Figure 43 is proposed. Due to the conveniences of ALD, a broad range of

materials can be used easily in this method. Even magnetic materials for magnetic ring arrays, which are interesting for applications, could be deposited directly or obtained by reducing oxides such as NiO or Fe_2O_3 into Ni or Fe_3O_4, respectively, in a hydrogen atmosphere. In addition, ring arrays with extremely small thickness, e.g. even several nanometer are feasible.

3.3 SUMMARY

In this chapter, LIL has been employed for the definition of locations and shapes of nanoring arrays. By double exposures, perfectly ordered circular or elliptical structure arrays have been fabricated in photoresist layers on a desired substrate and used as templates. Large-area ordered metallic nanoring arrays have been obtained by electroplating of metals along the step edges of resist structures on the templates. A second generation of substrate has been developed with metallic electrodes. Uniform metal deposition along the step edges of resist structures and, therefore, homogenous nanoring arrays have been obtained. Combination of room temperature ALD of TiO_2 on the template and subsequent Ar^+ bombardment provides another novel approach for the parallel synthesis of nanoring arrays of various functional materials.

4 LIL FOR THE FABRICATION OF IMPRINT STAMPS

In recent years, a considerable interest has developed in using nanoporous anodic aluminium oxide (AAO) as a host or template material for the preparation of two dimensional (2D) arrays of multifunctional nanostructures, which have applications in various scientific and technological fields, [67,74~81] because of its naturally occurring tendency to form self-organized arrays of cylindrical nanopores with triangular symmetry. However, in a typical anodization process, based on self-assembly effects the size of ordered domains is limited to a few micrometers. In template-based materials synthesis, it is desirable to use a template with long-range ordered pores.

In 1997, Masuda and Fukuda have first reported a pretexturing process combining the aluminium anodization method with nanoimprint technology, which allowed the preparation of long-range ordered pore arrangements over a larger area. [82] They have used a SiC imprint mold to produce ordered arrays of concaves on the Al substrate by nanoindentation prior to anodization. Shallow indentations on an Al substrate initiate pore nucleation during anodization and lead to a long-range ordered pore arrangement within the imprinted area (e.g., 4x4 mm). This work has attracted considerable attention within the growing community of research groups using AAO membranes, which is evident from the several hundred citations of this publication within a few years. However, the SiC mold was patterned by e-beam lithography and the processing costs of the imprint stamp can be several thousand US$ for a cm^2 of patterned area.

Alternatively, several nanostructuring techniques have been applied to pattern the aluminium surface by other groups, such as direct writing on the Al surface with EBL or FIB, imprinting with self-assembled nanosphere arrays or optical gratings. Each of those methods shows its own advantages. However, in terms of throughput, reliability, scalability and flexibility, the simple and economic realization of long-range ordered AAO membrane over large area still presents challenges.

In this work, imprint stamps with periodic structures have been developed based on LIL and replication processes. Large-area 2D periodic structure arrays were generated by

LIL as master structures for imprint stamps. Nanoindentations on the Al surfaces were performed prior to the anodization process in order to induce the pore growth at lithographically defined positions. In cooperation with other co-workers in our group and Prof. Ross' group at MIT, two kinds of imprint stamps based on LIL defined structures were developed. The fabrication processes of the Si_3N_4 and Ni stamps are introduced in section 4.1 and 4.2, respectively. The corresponding anodization results are also presented. The advantages of the application of LIL in the guidance of pore growth are summarized in section 4.3.

4.1 Si_3N_4 STAMP REPLICATED FROM INVERSE PYRAMID STRUCTURES

In previous work of our institute, a Si_3N_4 imprint stamp with pyramid tips for imprinting the Al surface to achieve long-range ordered AAO films [83,84] was developed based on conventional optical lithography, RIE, anisotropic KOH etching and wafer bonding techniques. Using pyramid-shape imprint structures, the imprint pressure required for guiding anodization is lower than that of the dot-like master mold fabricated by Masuda *et al.* [82] However, the imprint stamp was patterned in that case by conventional optical lithography, which is limited by resolution (minimum period: 500 nm), cost and scalability.

In this work, instead of conventional optical lithography, LIL was employed for the patterning of the imprint stamp, as shown in Figure 45. Hexagonally arranged periodic structures with lattice constant down to 200 nm were generated on a 4 in. wafer (‹100› orientation) by means of LIL with double exposures. The polymer structures were transferred into the underlying SiO_2 layer by RIE with CHF_3 gas (30 sccm, 5 mTorr, 100 W, 1 min 30 sec for 25 nm) and subsequently removed with O_2 plasma. The substrate with patterned SiO_2 mask was then anisotropically etched in 40 wt.% KOH.IPA (Isopropylalcohol) (100:1) solution to achieve the inverse pyramid structures. A replica of the inverse pyramid structures was obtained by plasma enhanced chemical vapor deposition (PECVD) of Si_3N_4 layer on top of the patterned Si substrate.

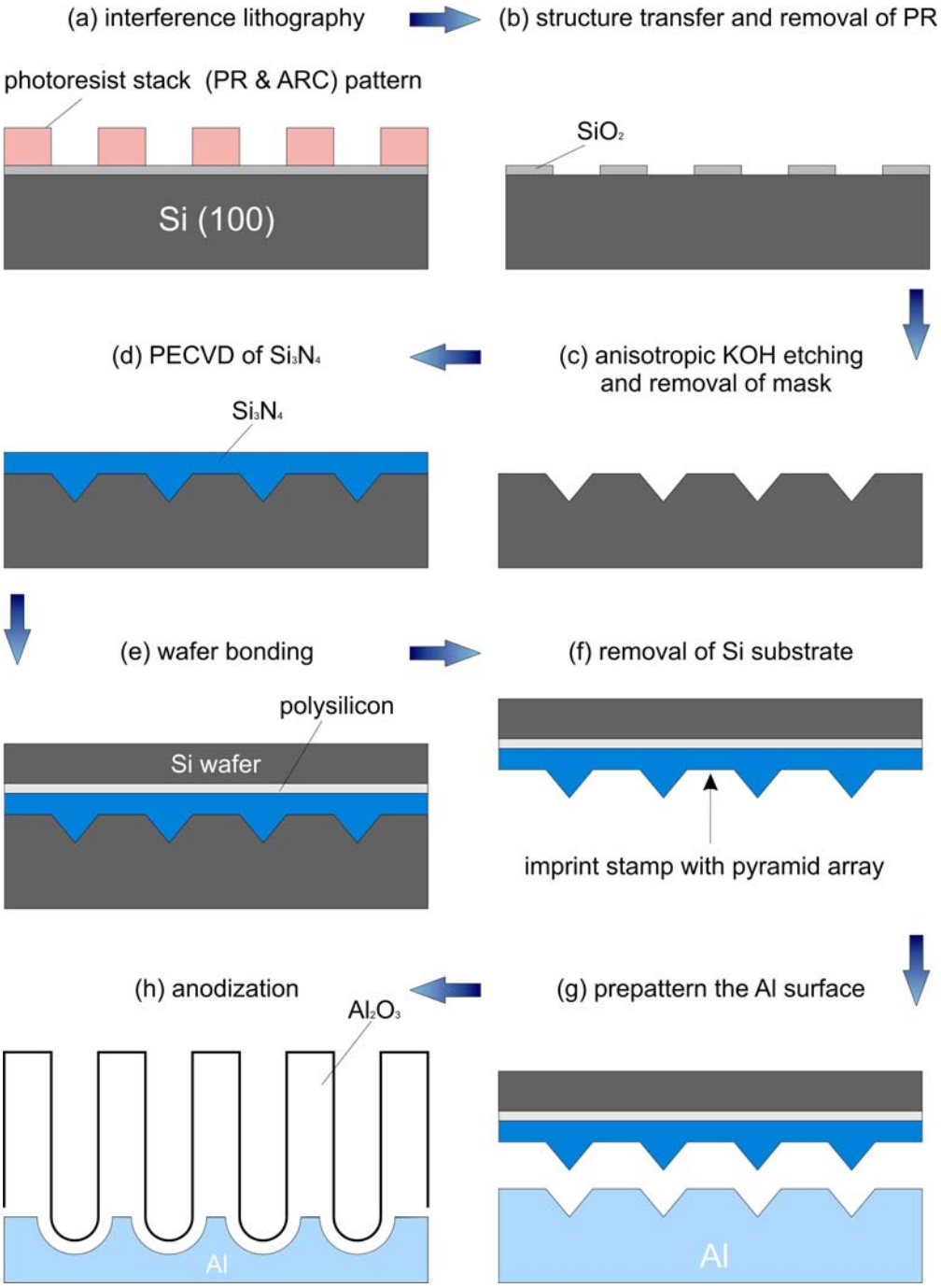

Figure 45: Fabrication Si_3N_4 imprint stamp with pyramid arrays and imprint guided anodization of aluminum. (a) Photoresist pattern with a hexagonally arranged hole array was generated by LIL; (b) The PR pattern was transferred into the underlying SiO_2 layer; (c) Inverse pyramid structure in Si substrate obtained by anisotropic KOH etching; (d) PECVD of Si_3N_4 layer; (e) Wafer bonding; (f) Removal of the patterned Si substrate, imprint stamp was obtained; (g) Prepatterning the electropolished Al surface with the Si_3N_4 stamp by applying 5 kN cm^{-2}; (h) Imprint guided anodization, ideally ordered porous alumina over large area.

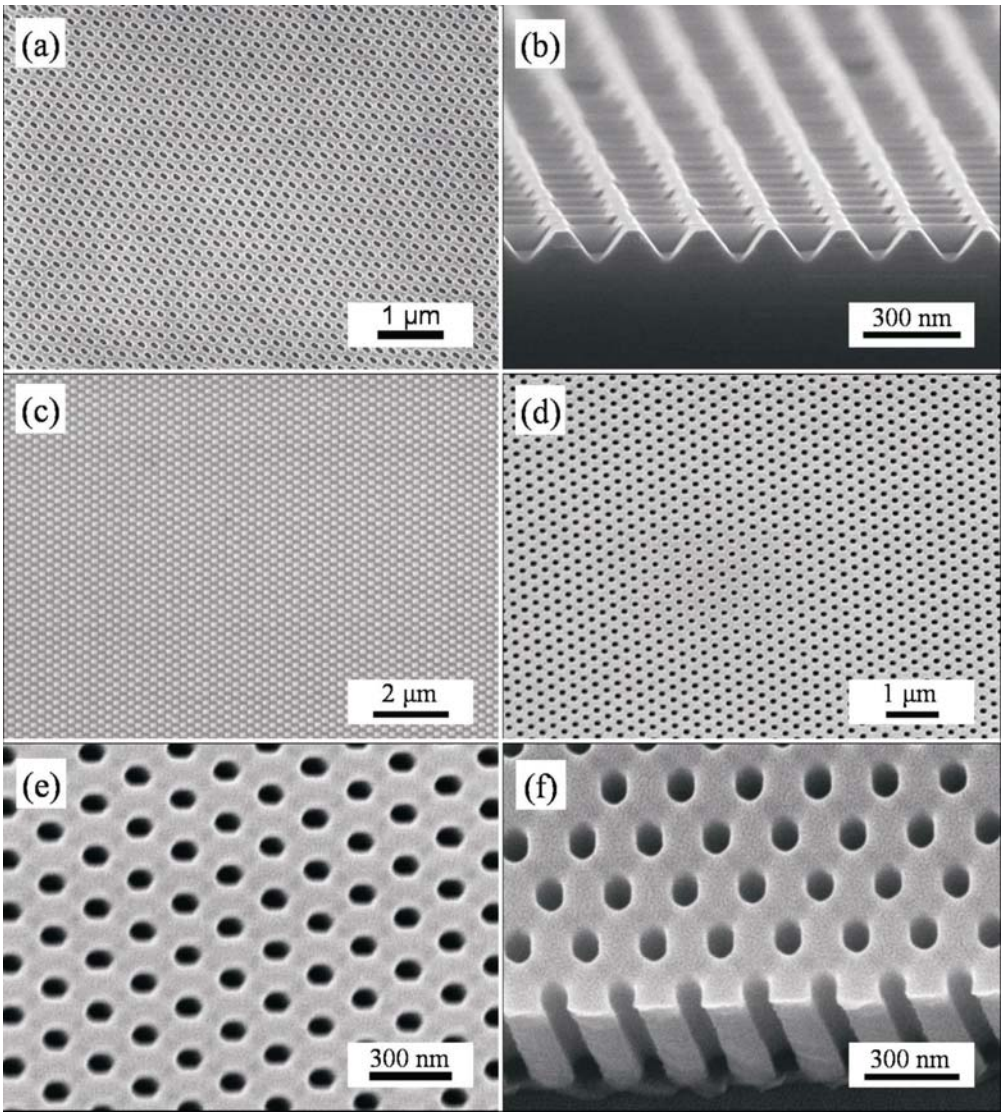

Figure 46: SEM images of (a) LIL generated photoresist pattern; (b) KOH etched inverse pyramid structure; (c) Top-view of the Si_3N_4 imprint mold; (d) Top-view, (e) magnified top-view and (f) oblique-view of ideally ordered porous alumina obtained by imprint guided anodization.

To facilitate the handling, another Si wafer was bonded on the top of the Si_3N_4 layer. [83, 84] Finally, the initial patterned Si substrate was removed by polishing and spin etching. A piece of this imprint stamp (typically 1x1 cm^2) was placed on the electropolished Al chip for nanoindentation with an oil press. By applying 5 kN cm^{-2}, successful pattern transfer was obtained. The prepatterned Al substrate was subsequently anodized in an anodization cell.

Figure 46 shows representative SEM images of the imprint stamp and AAO. LIL-

generated photoresist structure with a hexagonally arranged ellipse array is shown in Figure 46a, the lattice constant is 200 nm. Figure 46b shows an oblique view of anisotropically KOH-etched inverse pyramid array in a Si substrate. A top-view of the replica from the master, the Si_3N_4 imprint mold, is shown in Figure 46c. The imprint guided anodized AAO is shown in Figure 46d (top-view), e with magnified view and f oblique view.

4.2 WAFER SCALE Ni IMPRINT STAMP

More recently, Masuda *et al.* have demonstrated the fabrication of ideally ordered AAO membrane with a sub-50-nm interpore distance by using a metal imprint stamp, which was replicated from a resist pattern prepared by EBL. [85] This process is simple and does not require pattern transfer processes by RIE. However, the resist pattern written by EBL is not reusable and limited by the exposure area. Therefore, the metal mold is expensive. In this work, we have developed two kinds of inexpensive Ni imprint stamps based on LIL and electrochemical deposition (see Figure 47).

4.2.1 Ni IMPRINT STAMP REPLICATED FROM RESIST PATTERN

In method I (Figure 47 a), similar to the method described in ref. [85], the electrodeposited Ni imprimt stamp is replicated from a large-scale periodic photoresist pattern. However, instead of using EBL, the periodic photoresist patterns were fabricated by LIL. A bilayer stack of a negative tone PR (OHKA TSMR-iN027) with a thickness of 180 nm and an ARC (Brewer Science WiDE-8B) with a thickness of 70 nm deposited on the Si substrate was used. After double exposure and development of the resist stack (introduced in section 2.4.2), square- or hexagonal-arranged hole arrays of photoresist were obtained. In order to make the surface of the polymer pattern electrically conductive, a thin Au film with a thickness of several nanometers was then plasma-sputtered onto the resist pattern. This Au layer served as a working electrode in the subsequent electrodeposition of the metal.

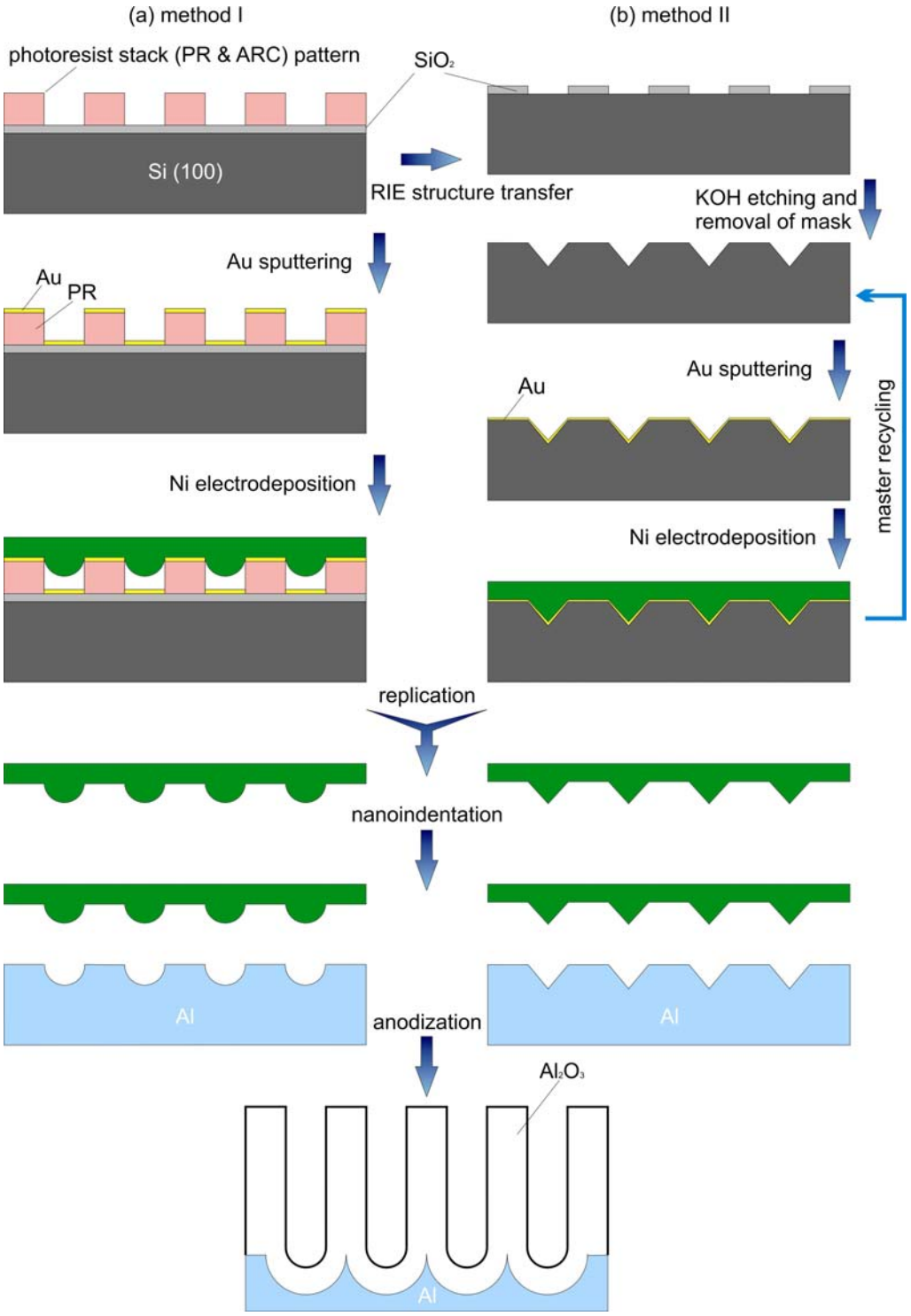

Figure 47: Schematic diagram of the fabrication of ideally ordered anodic alumina using Ni imprint stamp that can be replicated from (a) a photoresist pattern (method I) and (b) a silicon master (method II). The processes consist of two steps: the replication of Ni imprint stamps from a master pattern obtained by LIL or further etching processes, and the subsequent imprint guided anodization for long-range ordered AAO.

Ni was electrodeposited on the resist pattern using a Ni electroplating solution comprising $NiCl_2 \cdot 6H_2O$ ($8.41*10^{-2}$M), Ni $(H_2NSO_3)_2 \cdot 4H_2O$ (1.59M), and H_3BO_3 (0.33M). The typical current density was 7 $mAcm^{-2}$. The thickness of the nickel stamp could be controlled by varying the amount of the total integrated charge involved in the electroplating reaction. After the electroplating, Ni imprint stamps with a thickness of ≈ 5 μm were obtained by peeling the metal films off the resist patterns.

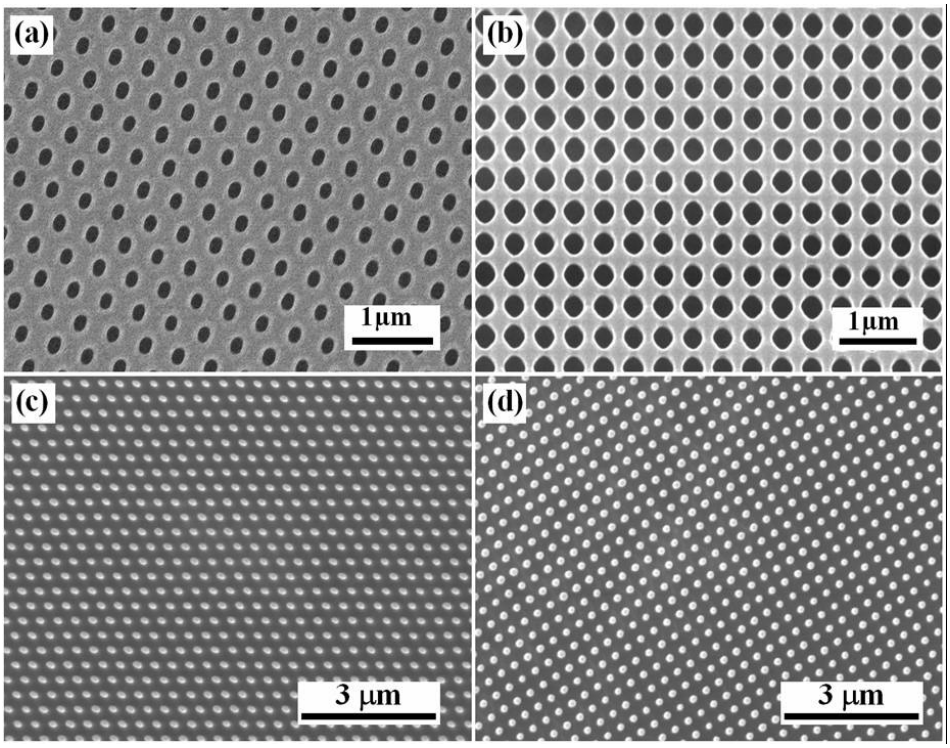

Figure 48: Representative SEM images of photoresist patterns with (a) hexagonal and (b) square arrangements of holes, and the corresponding Ni imprint stamp replicated from them (c) and (d), respectively.

LIL produced arrays of uniform-sized holes in the resist over the entire wafer area (in this case 4 in. in diameter). The symmetry of the lattice and the periodicity of the pattern could be easily controlled by the angle between the two LIL exposures and the incident angle, respectively. The replicated Ni films consist of an array of bumps with elliptical (in the hexagonal array) or circular (in the square array) shapes and rounded tops, which match the geometry of the holes in the resist stack.

4.2.2 Ni IMPRINT STAMP REPLICATED FROM Si MASTERS

After a replication of Ni film from the resist pattern, the structures are mechanically damaged due to the poor mechanical durability of the resist and its weak adhesion to the substrate. The master pattern can not be reused in this case. Pattern transfer by nanoindentation onto Al substrate requires 50 to 2000 times higher pressures in comparison to conventional imprint lithography on polymer layers. [86] Due to the high mechanical stress, damage to the imprint stamp often occurs after several imprints. So it is advantageous to be able to make multiple copies of imprint stamps from a single master. In addition, as introduced in section 4.1, the Si_3N_4 imprint stamp with sharp pyramid tips array allows the pattern transfer on to Al surface with much lower pressure due to its imprint-friendly geometry.

Therefore we have developed an alternative approach, in which a robust Si master with an array of inverse pyramids structure defined by LIL, RIE and anisotropic KOH etching was employed, the same as for the Si_3N_4 stamp (section 4.1). In addition, a surface modification procedure was employed in order to achieve smooth stripping. First, the Si surface after KOH etching was cleaned by immersing the sample in Piranha solution (H_2SO_4/H_2O_2; 3:1) for 30 min with intermediate ultrasonication to remove organic contaminations. Surface modification was achieved by treating the resulting Si with 3-aminopropyltrithoxysilane (3-APTES; 1.0 vol.% in CH_3CH_2OH) at 65 °C. The self-assembled organosilane layer serves as an anti-sticking film [87~89] during the stripping of the Ni film. Instead of complex Si_3N_4 deposition and replication processes, the Ni film was deposited by means of electrochemical deposition and simply stripped subsequently from the master (Figure 47b). The master can be recycled. This approach combines the advantages of the Si_3N_4 stamp and Ni stamp replicated from the resist pattern.

The Ni imprint stamps introduced above show their unique advantages, in comparison with the Si_3N_4 imprint stamps with pyramids tips in section 4.1,:

- They are inexpensive.
- They require fewer process steps.

- They are mechanically very stable and flexible, the curve-like topography of the electropolished Al surface could be matched and therefore a homogenous pattern transfer is enabled.

- They exhibit a lower mechanical hardness and do not form cracks during nanoindentation, thus allowing multiple uses.

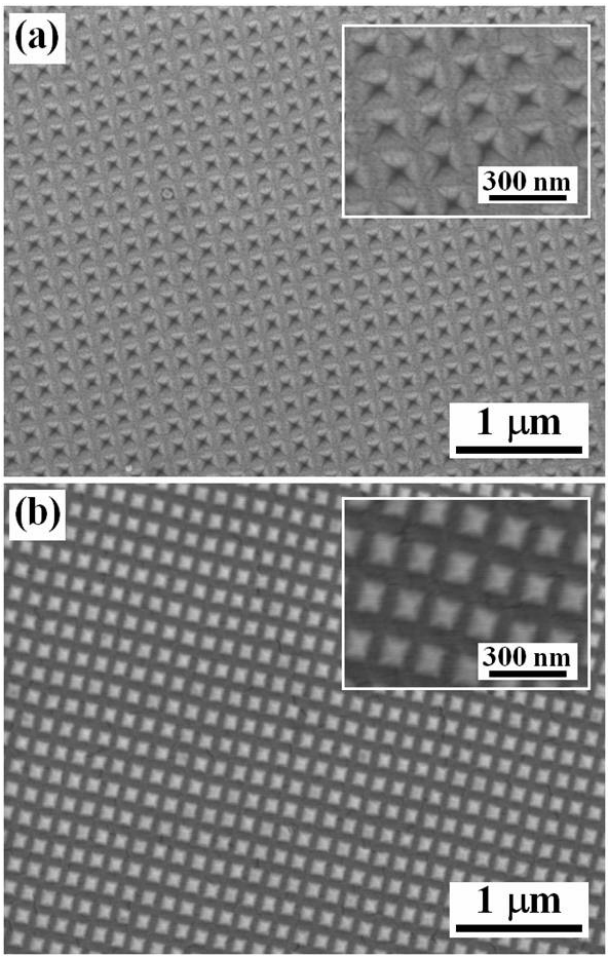

Figure 49: SEM images of (a) a silicon master pattern with an array of inverse pyramid etch tips arranged in a square lattice and (b) a Ni imprint stamp replicated from the silicon master shown in (a). Inserts show the corresponding magnified SEM images.

4.2.3 IMPRINT GUIDED ANODIZATION

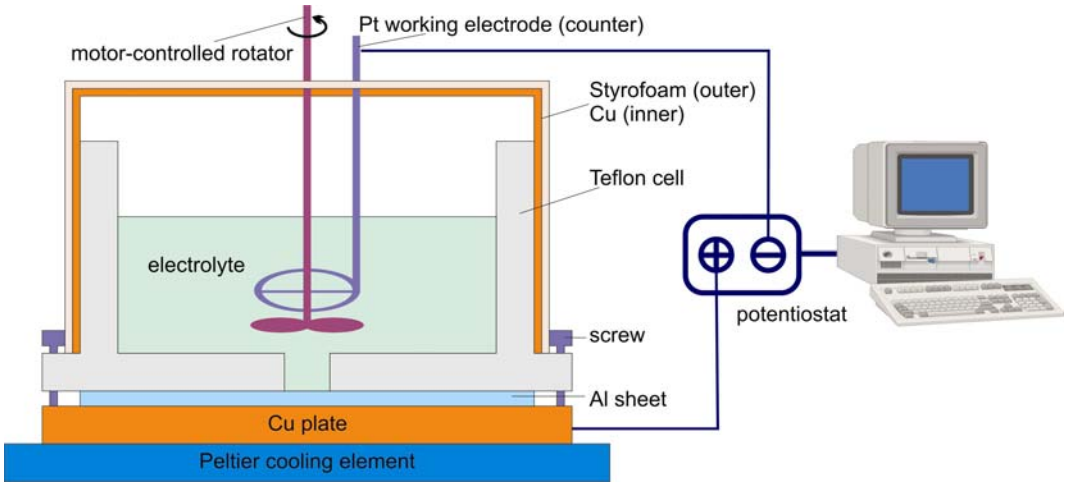

Figure 50: Shematic illustration of an anodization cell.

The replicated Ni films were used as imprint stamps for the prepatterning of electropolished Al substrate. Typically, nanoindentation of the Al was carried out by applying a pressure of about 25 kN cm^{-2} (method I) or 5 to 14 kN cm^{-2} (method II), respectively, for 10 sec using an oil press. The present Ni imprint stamps show a sufficiently high mechanical strength for nanoindentation of Al, and AFM investigations revealed that there was no apparent structural deformation of the surface features of the Ni imprint stamp even after it had been used several times.

After nanoindentation, the Al chip was anodized in an anodization cell, as shown in Figure 50. It consists of a two electrode system, e.g., the platinum (Pt) mesh serving as the counter electrode and the Al sheet serving as the working electrode. The Al sheet is inserted between the electrolyte cell and brass plate and fixed by screws. To stir the electrolytes vigorously, a motor-controlled rotator is used. The anodization parameters are controlled by a computer, using in-house-developed software. The cell is thermally isolated with Styrofoam. For cooling the apparatus, water cooling and Peltier elements are employed.

Each of the shallow concaves created by imprinting serves as an nucleation site for the development of a pore in the early stages of anodization, and results in the eventual growth of a pore channel. The anodization voltage was chosen to satisfy the linear

relationship between interpore distance (here lattice constant of the imprint stamp) and anodization potential (2.5~2.8 nm V^{-1}).

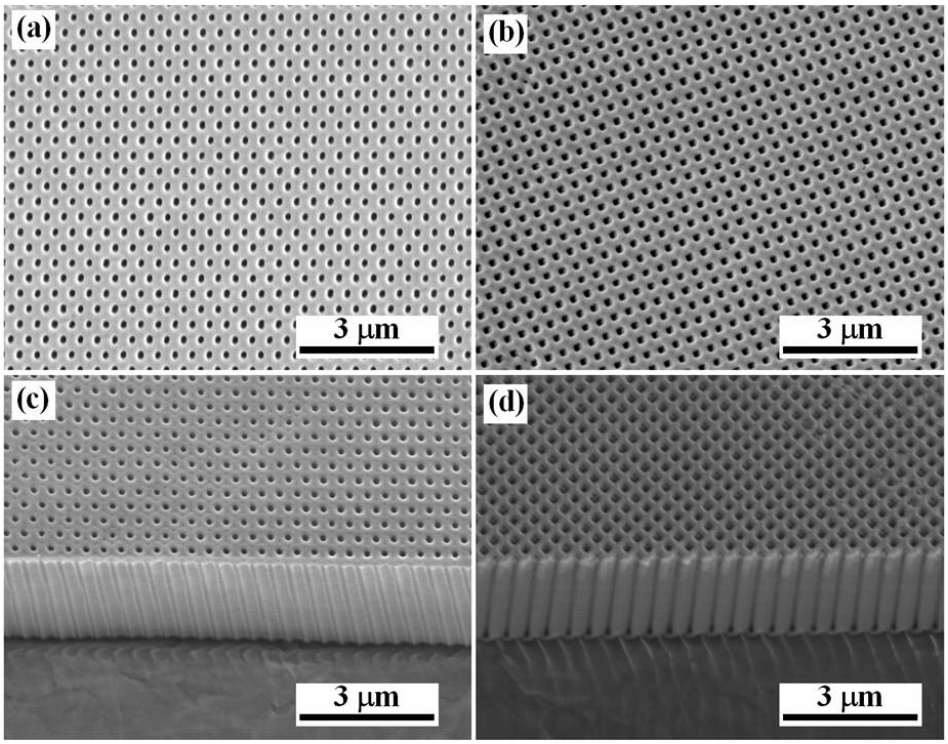

Figure 51: SEM images of long-range ordered anodic porous alumina with (a) hexagonal and (b) square arrangements of pores. (c) and (d) are corresponding oblique-views.

Figure 51 shows representative SEM images of the anodic porous alumina with hexagonal (Figure 51 a) and square (Figure 51 b) pore arrangement, together with an oblique view of the cross-section of the respective samples (Figure 51 c and d), obtained by imprinting the Al surface with the Ni mold prior to anodization (method I). Anodization was conducted under a constant voltage of 156 V in 5 wt% H_3PO_4 (phosphoric acid) at 0.5 °C. Straight oxide nanochannels with uniform-sized pores were obtained.

The samples with a hexagonal pore arrangement maintained a well-ordered pore lattice up to a pore aspect ratio (length/inner diameter) typically over 120, but samples with a square pore lattice maintained long-range order only up to an oxide thickness of about 3 μm, which corresponds to an aspect ratio of 15. In addition, the geometrical shape of the pores depended also on the symmetry of the imprint stamp. The AAO with a hexagonal

arrangement of holes (Figure 51 a) has circular-shaped openings at the pore mouth surface. However, the square arranged holes (Figure 51 b) have rectangular cross-sections.

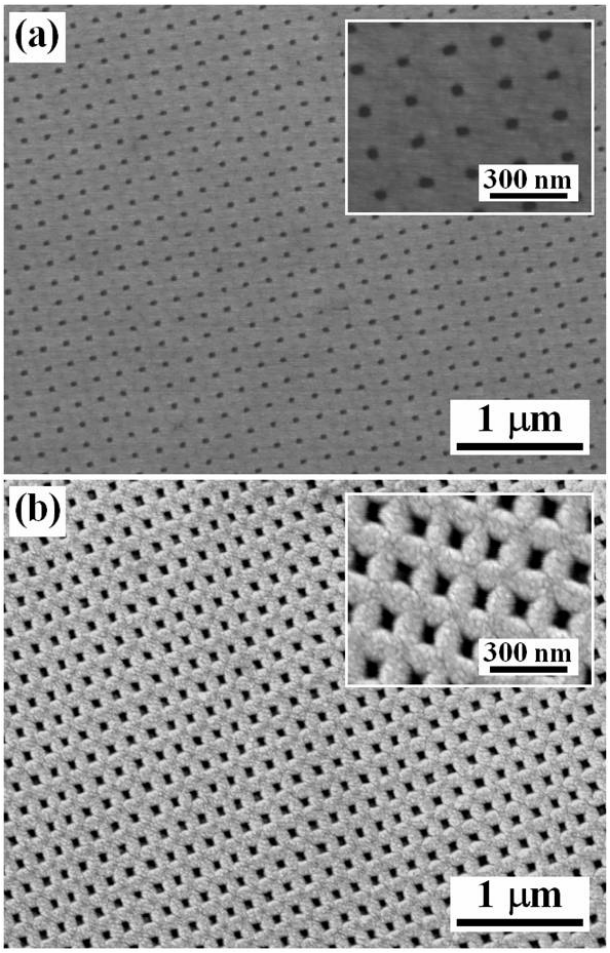

Figure 52: SEM images of anodic porous alumina. The Al surfaces were prepatterned by applying a pressure of (a) 5 kN cm^{-2} and (b) 14 kN cm^{-2} using a Ni imprint stamp shown in Figure 49 b. magnified views of the respective samples are shown as inserts.

Figure 52 shows SEM images of nanoporous AAO prepared by imprinting Al substrate with pyramid imprint structrues by applying 5 kN cm^{-2} (Figure 52 a) and 14 kN cm^{-2} (Figure 52 b). Anodizations were conducted at 84 V in 0.05 M $H_2C_2O_4$ (oxalic acid) at 1 °C. It is clear that a higher pressure applied during nanoindentation process could result in a rectangular pore shape and a larger size of the pore mouths of the AAO.

The Ni imprint stamps have also been employed for the pre-patterning of the aluminium surface prior to a hard anodization (HA) process, which has a much higher growth rate

of the porous oxide film (25~35 times) than for mild anodization (MA) (Figure 53a). A new self-ordering regime has been found in the ranges of D_{int}=200-300 nm with oxalic acid at 120-150 V. Ideally ordered alumina membranes with a high aspect ratio (>1000) of uniform nanopores can be fabricated by HA of pre-patterned aluminium by maintaining the current density at a certain level according to the desired D_{int} at a given anodization voltage. The porosity P in this case is much lower than that obtained by the MA process (P_{HA}~3%, P_{MA}~10%) and therefore a combination of HA and MA allows the fabrication of ideally ordered porous alumina membranes with modulated pore diameters (Figure 53b). The length of each segment can be adjusted by varying the anodization time of the corresponding process.

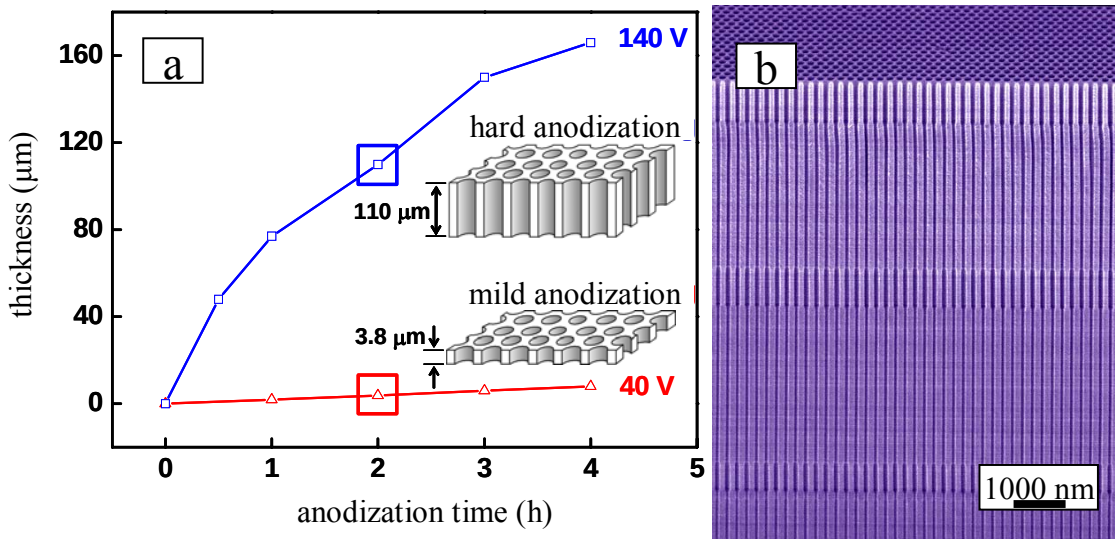

Figure 53: (a) Film thickness as a function of time during HA at 140 V (blue line) and an MA process at 40 V (red line). The different thickness of anodic oxides after 2 h of anodization are highlighted schematically in the inserts; (b) A representative SEM image showing the cross-section view of an ideally ordered AAO membrane with modulated pore diameters.

4.3 SUMMARY

In this chapter, LIL has been introduced for the fabrication of master structures for Si_3N_4 and Ni imprint stamps. It is advantageous that LIL allows parallel wafer-scale fabrication of perfectly arranged 2D periodic nanostructures with a high throughput and flexibility at low cost. Therefore, LIL has been employed for the definition of matrix

structures of imprint masters for the indentation of aluminium surfaces prior to the anodization. Based on the previous works in our institute, instead of the conventional optical lithography, LIL has been introduced into the fabrication of Si_3N_4 stamps with pyramid structures. Wafer-scale Ni imprint stamps have been replicated directly from LIL generated resist structures and Si masters, respectively. The fabrication of large-area perfectly ordered nanoporous anodic aluminium oxide with a square or hexagonal pore arrangement has been demonstrated by using the above mentioned stamps. The smart combination of LIL and imprint guided anodization of aluminium provides a low cost route for the fabrication of porous alumina with lithographically defined pore arrangement on cm^2-scale.

5 HORIZONTAL GRATING, NANOGROOVE AND NANOCHANNEL ARRAYS

The mass fabrication of integrated circuits and optical devices based on silicon and silica has been developed for decades. [90] Compact nanostructures fabricated on Si wafers, such as fin-like structures, nanogroove arrays and nanochannel arrays, show potential applications for nanoelectromechanical systems (NEMs), communication, nanofluidic, nanoelectronic and nanooptic devices. [91~97] For the fabrication of these structures, even though the advanced lithography techniques, such as electron beam lithography (EBL), [98~100] scanning probe lithography (SPL) [101,102] or focus ion beam (FIB) [103], enable the generation of 1-dimensional (1D) line and space structures with a resolution in nanometer range, they are cost- and time-consuming and not suitable for large-scale production.

In this chapter, the fabrication of wafer-scale horizontal nanograting, nanogroove and nanochannel arrays based on LIL defined 1D structures are introduced. The oxidative size-reduction strategy is introduced to extend the available resolution of grating structures generated by LIL (section 5.1). In section 5.2, the non-uniform oxidation of structural silicon or a SOI substrate is described for the fabrication of nanochannel arrays. By using LIL defined polymer structures as sacrificial structures, another approach for obtaining nanochannel templates has been developed (section 5.3).

5.1 NANOGRATING AND NANOGROOVE ARRAYS BASED ON OXIDATION SIZE-REDUCTION STRATEGY

5.1.1 THERMAL OXIDATION OF SILICON

Thermal oxidation of silicon is a standard process step in the IC fabrication industry. During dry oxidation, the silicon wafer reacts with the ambient oxygen, forming a layer of SiO_2 on its surface. A model for the oxide growth has been put forward by Deal and

Grove, which are known as the linear-parabolic-model. [1] It predicts linear oxidation rate initially, followed by a parabolic behaviour for thicker oxides.

$$Si(solid) + O_2(gas) \rightarrow SiO_2(solid)$$ Equation 5.1

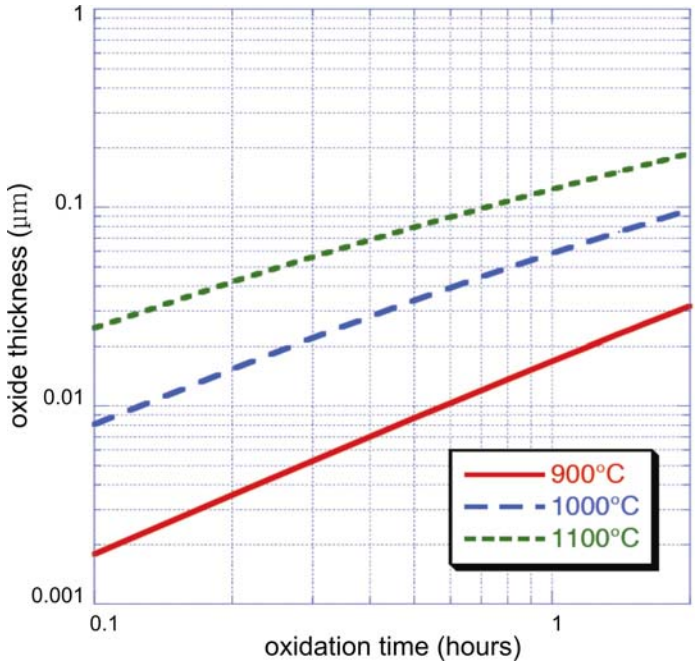

Figure 54: Dry oxidation rate of silicon (100). [1]

The oxidation reactions occur at the Si/SiO_2 interface. Oxygen diffuses through the growing oxide layer and reacts with the silicon surface. Silicon at the interface is consumed as the oxidation takes place. The thickness of the silicon consumed is 44% of the final thickness of the oxide formed. Thermal oxidation is a slow process: for dry oxidation at 900 °C, a ca. 20 nm thick oxide can be produced during 1 h; therefore the thickness of the oxide or of the consumed silicon could be precisely controlled by varying the oxidation time under a fixed oxidation temperature and oxygen pressure. The oxidation rate depends also on the silicon crystal orientation: that of (111) is somewhat higher than of (100) silicon. In addition, highly doped silicon oxidizes faster than normally doped silicon. [1]

5.1.2 SIZE-REDUCTION OF GRATING AND GROOVE ARRAYS

As introduced in chapter 2, LIL allows the fabrication of parallel periodic nanograting

and nanochannel arrays. The duty-cycle can be adjusted by varying the exposure dose. However, due to the limitation of the photoresist contrast, the process latitude for grating line-width control is difficult. For the grating structures, it is very difficult to get a duty-cycle of more than 70% or less than 35%. Thus it is still a challenge to fabricate patterns comprising narrow fin-like structure separated by broad grooves, or narrow grooves separated by broad gratings.

Thermal oxidation and subsequent removal of SiO_2 by HF etching allow the reduction of the lateral size of micro- and nanostructures. [104~110] This process has been considered as a standard approach in silicon technology. In addition, the oxide volume is greater than the volume of the silicon it replaces. Considerably less attention has been paid to the systematic oxidative volume expansion of silicon nanostructures on the exploitation of size-reduction of grooves in grating structures. In this work, the traditional thermal oxidation technique was employed to extend the range of realizable feature sizes and spacings of grating patterns generated by LIL and etching processes on Si wafers.

In this work, as shown in Figure 55a to c, the original silicon grating structures with different periodicities were fabricated by LIL, RIE and KOH etching processes on (110) wafers covered by a 25 nm thick SiO_2 layer. First, photoresist lines and space patterns were defined by LIL. The pattern was transferred through the underlined SiO_2 layer by means of RIE with CHF_3 gas and subsequently removed in O_2 plasma. The SiO_2 pattern was then used as etching mask for an anisotropic KOH etching. In order to improve the infiltration of narrow channel structures during the etching process, isopropanol was added to the solution (KOH: H_2O: isopropanol at a weight ratio of 2:2:1). Shortly before the KOH etching, a short HF etching was implemented to remove the native oxide formed in air. The etching processes were carried out with ultrasonic assistance at room temperature and the etching rate was ~1 nm/sec. By this procedure, an array of aligned grooves with nearly rectangular cross-sections was obtained, since the (110) surface of Si exhibits the highest etching rate. [111~113] The position of the grooves is defined by the developed areas, where the Si is directly exposed to the base, whereas the areas still covered by SiO_2 are not attacked and form the walls between adjacent grooves. Subsequently, the SiO_2 mask was subsequently removed by etching with a 5% aqueous

HF solution at room temperature.

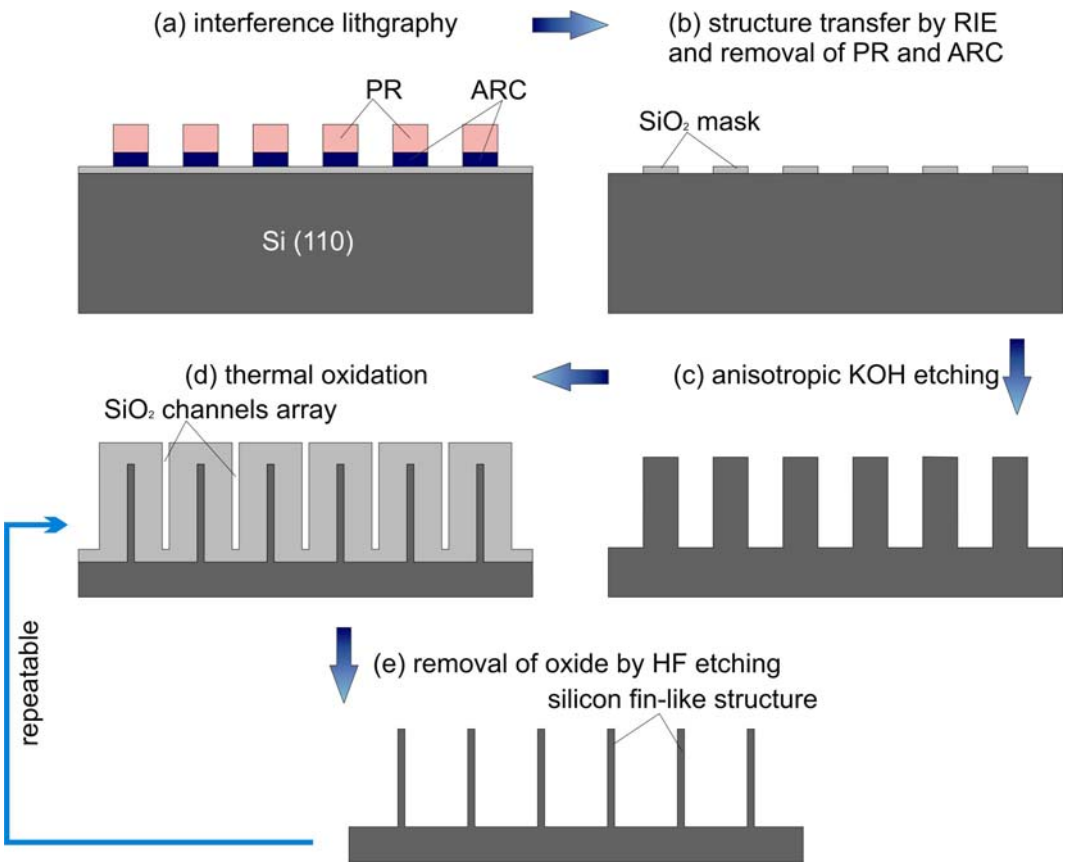

Figure 55: Schematic illustration of the fabrication of nanograting and nanogroove arrays based on LIL and oxidative size-reduction strategy. (a) Photoresist lines and space pattern generated by LIL; (b) Structure transfer by means of RIE with CHF_3 gas and subsequent removal of PR mask in O_2 plasma; (c) Silicon (110) orientation grating structure obtained by anisotropic KOH etching; (d) Thermal oxidation and the size of the grooves was reduced due to the volume expansion. (e) Silicon fin-like structures are obtained by removal of SiO_2 in aqueous HF solution.

Thermal oxidation of the wafers thus treated at temperatures ranging from 900 °C up to 1050 °C in air leads to the growth of an oxide layer on the surfaces of silicon grating structures. In comparison to the volume of consumed silicon during thermal oxidation, the volume of SiO_2 increases by 125%, [114~116] and consequently the width of the grooves decreases significantly (Figure 55d). In addition, the feature size of the fin-shaped silicon core is reduced by the oxidation of silicon. After a subsequent etching step with aqueous HF solution the very narrow fin-like structure array can be released from the SiO_2 shells (Figure 55e). In order to demonstrate the significant size-reduction effect both in gaps and fin-like structures array, two series of samples were prepared

systematically.

Figure 56a shows a SEM image of the top-view of a grating structure prepared by LIL, RIE and KOH etching, corresponding to the schematic cartoon Figure 55c. The grating structures have a period of ~265 nm, a gap width of 130 nm (duty-cycle (DC) = 50.9%) and a depth of ~810 nm. Oxidizing the sample at 950 °C for 170 min and 270 min, respectively, drops the gap width to 90 nm (DC = 66.0%) (Figure 56b) and 35 nm (DC = 86.8%) (Figure 56c and d).

Figure 57 demonstrates the size-reduction of silicon fin-like structures. The original silicon grating has a 640 nm structure width, 1.4 μm period (DC = 45.7%) and is 1.5 μm in depth (Figure 57a). After repeating four times the oxidation (950 °C in air for 120 min) and HF etching processes, the width of the fin-like structures dropped to 140 nm (DC = 10%). Another three times oxidation (900 °C in air for 60 min) and HF etching processes were performed. Silicon structure arrays with an 80 nm (DC = 5.7%) width has been achieved. The width of the structures has been decreased by 87.5%.

Even smaller structure was demonstrated with original silicon grating structures array, which has a width of 140 nm, period of 340 nm (DC = 41.2%) and depth of 810 nm. After repeating three times of the process including an oxidation at 900 °C in air for 120 min following by a chemical etching in 5% HF solution, a sub-30 nm (DC < 8.8%) structure width has been obtained (Figure 58). Figure 59 shows TEM and HRTEM images in cross-section-view of a 60 nm thick silica layer covering a silicon fin-like core, which was prepared by repeating the oxidation and etching processes from an original silicon grating structure in Figure 57a. The upper part of the silicon structures shows crystalline silicon with only ~5 nm in width. The silicon (111) crystal lattice planes are obvious in the HRTEM image (Figure 59b).

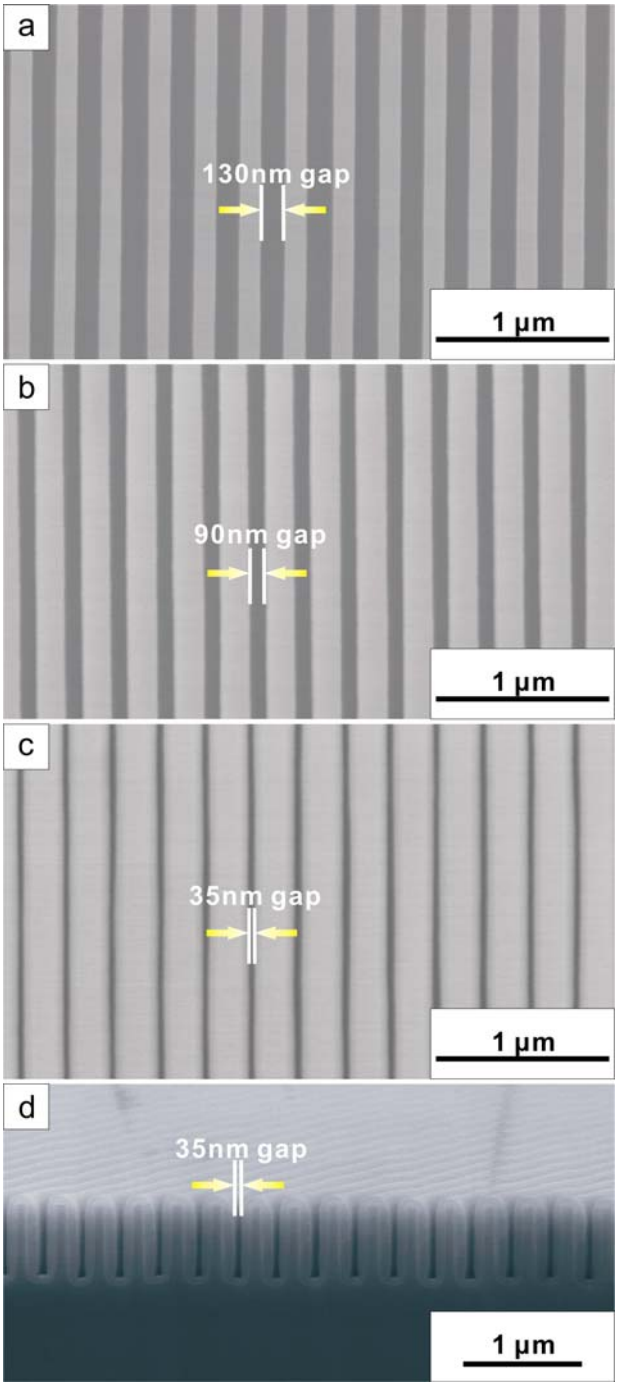

Figure 56: SEM images of (a) original silicon grating structures with 130 nm gap and 265 nm pitch, about 810 nm in depth; the SiO_2 nanogap array with a width of (b) 90 nm and (c) 35 nm, obtained by oxidation of the silicon grating structure in (a) at 950 °C for (b) 170 min and (c) 270 min in air; (d) the cross-section view of the gap structure in (c).

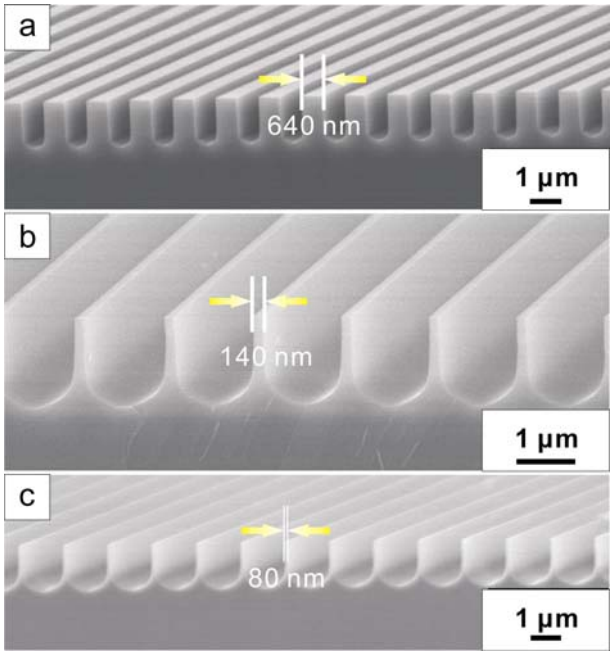

Figure 57: SEM images in an oblique-view of (a) original silicon grating structures; (b) silicon grating structures in (a) after repeating four times of the process including a thermal oxidation following by a chemical etching in 5% HF solution; (c) silicon grating structures in (b) after repeating three times of the process including a thermal oxidation following by a chemical etching in 5% HF solution.

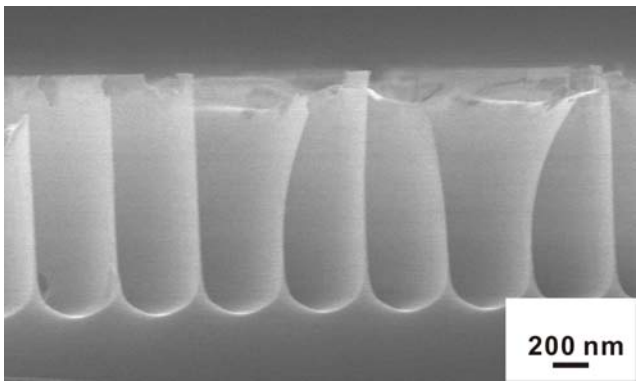

Figure 58: SEM image in an oblique-view of silicon fin-like structure with a sub-30 nm width.

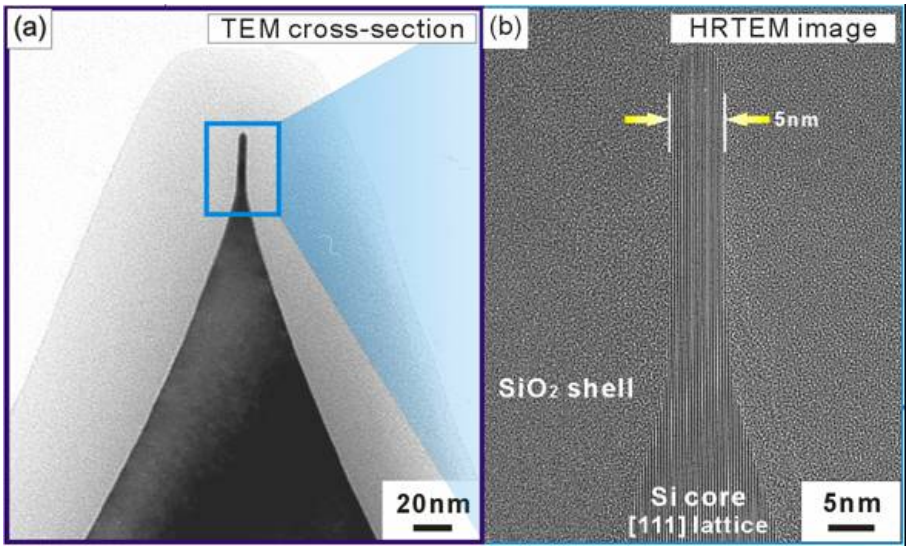

Figure 59: TEM (a) and HRTEM (b) images of silicon fin-like structure with a width of 5 nm at the tip by repeating oxidation and HF etching of the silicon grating structure shown in Figure 57a.

5.2 OXIDATIVE SELF-SEALED NANOCHANNEL ARRAYS

5.2.1 RETARDATION EFFECT AT CORNERS

Besides the narrow nanogroove arrays introduced above, enclosed horizontal nanochannel arrays attract more and more attention recently for various applications in the fields of nanofluidics, nanobiotechnology and analytics. [117~119] Moreover, nanochannels located on Si wafers are potential versatile templates for the fabrication of nanowire or nanotube arrays. They have several unique advantages over AAO templates: for example, nanowires or nanotubes aligned on a planar substrate could be easily electrically contacted. The well-established fabrication procedures for such templates involve the fabrication of nanogroove arrays and additional bonding or deposition steps, which are costly and technologically challenging, in order to convert grooves into sealed channels. [120~124]

As we have demonstrated, based on the thermal oxidative size-reduction strategy, the size of the silicon nanogrooves, which were fabricated by LIL and etching process, can be reduced due to the volume expansion during the oxidation of silicon structures. However, according to the previous literatures of oxidation of structured silicon, the

presence of both convex and concave curvatures on patterned silicon substrates results in a pronounced retardation of the growth of oxide with respect to planar oxidation due to the compressive stress at the corner structures. [111~113,117~124] Therefore, the thickness of the generated SiO_2 layer is significantly smaller at the corners as compared to that of the flat surfaces.

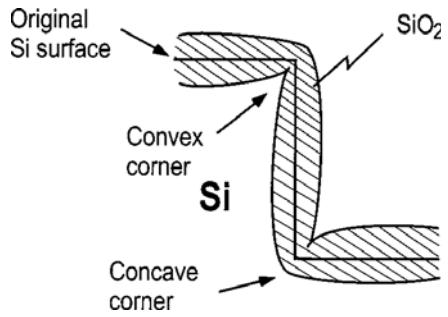

Figure 60: Schematic diagram of silicon thermal oxidation at convex and concave corners. The thickness of the oxide at the convex and concave corners is thinner than that at the flat surface of the silicon (Ref [114] a).

The retardation effect of the SiO_2 growth occurs both under dry and wet oxidation conditions, but it is more pronounced at concave corners than at convex corners. [115] Kao *et al.* attributed the lower growth rate at corners to viscous stress in the oxide layers associated with non-uniform mechanical deformation. [116] On flat surfaces, only the stress component parallel to the Si/SiO_2 exists in the newly formed SiO_2 layer, caused by the expansion in the volume during the oxidation of silicon. However, in curved systems stress perpendicular to the Si/SiO_2 interface also occurs and counteracts with the growth of the oxide layer. It is stretched at convex corners, whereas compressed at concave corners. Since oxidants can more easily diffuse through the stretched layers than through compressed layers, the retardation of the oxide growth appears to be stronger in concave structures. [115] During the investigation of fin-like structures prepared by oxidation of silicon grating structures, this effect has also been observed from TEM investigation. As can be seen in Figure 61, the upper part of the silicon fin-like structure has a width of ~35 nm, whereas the body of it has an only 5 nm silicon core, which clearly demonstrates the corner-retardation effect during the oxidation of silicon structures.

The dependence of the oxidation rates on the curvature dominates the oxidation of silicon nanostructures with sizes below 100 nm. [127,128] However, it is independent of crystal orientations and therefore could be applicable to both single-crystalline and polycrystalline Si substrates. This non-uniform Si oxidation effect at the convex or concave corners have been used, for instance, for fabrication of Si conical sharp tips for the AFM or field emitters, [110] or as mold for Si_3N_4 pyramidal sharp tips for the AFM, [129] respectively.

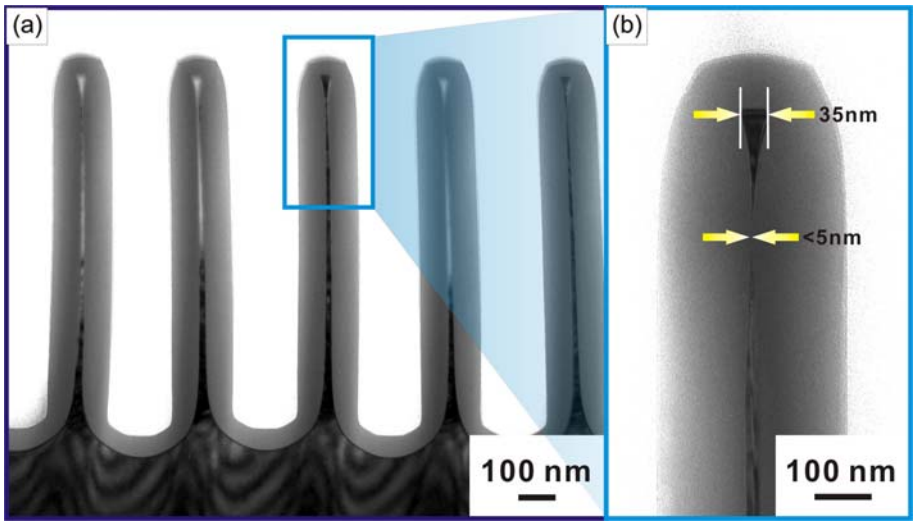

Figure 61: TEM image (a) and zoom view (b) of silicon core with a width of 35 nm at the tip part and <5 nm in the middle part.

We have developed two simple and reliable procedures, which combine the thermal oxidative size-reduction and pattern-dependent oxidative self-sealing strategies, for the large-scale fabrication of horizontal (in-plane) nanochannel arrays on silicon or SOI wafers with high spatial precision and high throughput at a low cost.

5.2.2 SELF-SEALED CHANNELS IN Si (110) WAFER

Figure 62 outlines the procedure for the fabrication of arrays of horizontal nanochannels by oxidative self-sealing of grooves in an (110)-oriented silicon wafer. Similar to the fabrication of silicon grating structures on (110) wafer, introduced in the last section, LIL, RIE and KOH etching processes were carried out step by step (Figure 62a to c). The as-prepared wafers were oxidized in air at temperatures ranging from 950 °C to

1050 °C. At the concave corners at the bottom of the grooves, the growth of the oxide is significantly retarded. Therefore the oxide layer growing from the opposite walls of the grooves will impinge above the bottoms, whereas hollow channels are still present at the bottoms. Since the retardation also occurs at the convex corners at the top of the walls, the oxidized wafers process trenches at their surface, which are parallel to the channels underneath (Figure 62d).

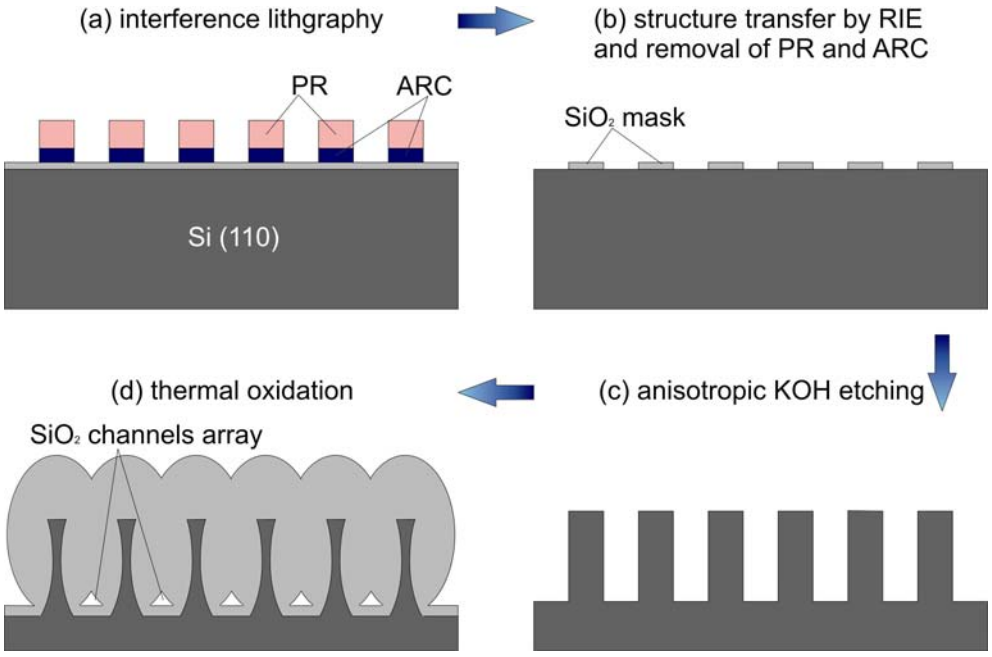

Figure 62: Schematic illustration of the fabrication procedure of aligned, horizontal nanochannel array in (110)-oriented silicon wafer by oxidative self-sealing strategy. (a) PR and ARC are patterned into lines and spaces structures by LIL; (b) Structure transfer through the underlined SiO_2 layer by means of RIE; (c) Anisotropic KOH etching of (110) silicon wafer; (d) Oxidative self-sealing of the silicon nanogrooves into nanochannels.

Figure 63a shows the SEM image of silicon grating structure prepared by the processes described in Figure 62a to c in a cross-section view. Silicon wafer containing grooves with a wall thickness of ~130 nm, a pitch of 260 nm and a depth of 230 nm can be measured from this image. Self-sealing of this structure occurs if the sample is annealed at 1000 °C for 6 hours. To investigate the dimensions of the channels in detail, cross-sectional specimens for transmission electron microscopy (TEM) were prepared. TEM was performed using a JEM 1010 microscope operated at 100 KV. Figure 63b shows a TEM image of a cross-section view of as-prepared arrays of nanochannels. The SiO_2

layer and the silicon substrate appear dark in contrast and light grey, respectively. The regularly arranged, nanochannels horizontally aligned appear as bright spots in the SiO_2 layer. Figure 63c shows a single self-sealed nanochannel with triangular shape in cross-section view. The length of the edges is 26 nm and each of the edges is parallel to the former surface of the wafer.

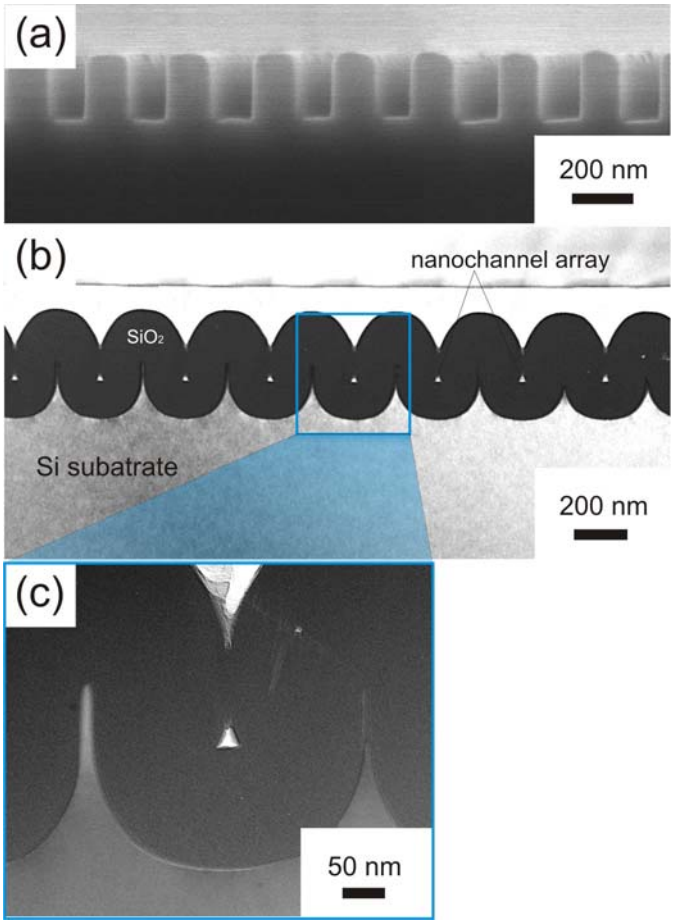

Figure 63: (a) SEM image of silicon grating structures with 260 nm pitch prior to the thermal oxidation in cross-section view; (b) TEM image of cross-section of the thermal oxidative self-sealed SiO_2 nanochannel arrays, and (c) shows the magnified view of TEM image (b).

5.2.3 SELF-SEALED CHANNELS IN SOI WAFER

Oxidative self-sealing is a versatile approach that could be applied to a broad range of different wafer architectures. In this work, we have also tuned this approach for the process of (100)-oriented SOI wafers containing a 250 nm thick SiO_2 interlayer covered by a 500 nm thick Si overlayer. PR and ARC were patterned into lines and space by

LIL. The polymer structures were subsequently transferred through the underlined 50 nm thermal oxide layer by RIE with CHF_3 gas. The silicon layer was selectively etched with CF_4/Ar plasma until the SiO_2 interlayer underneath and the polymer was removed by O_2 plasma etching (Figure 64b). The as-prepared wafer was oxidized in air to seal the grooves in the SOI wafer.

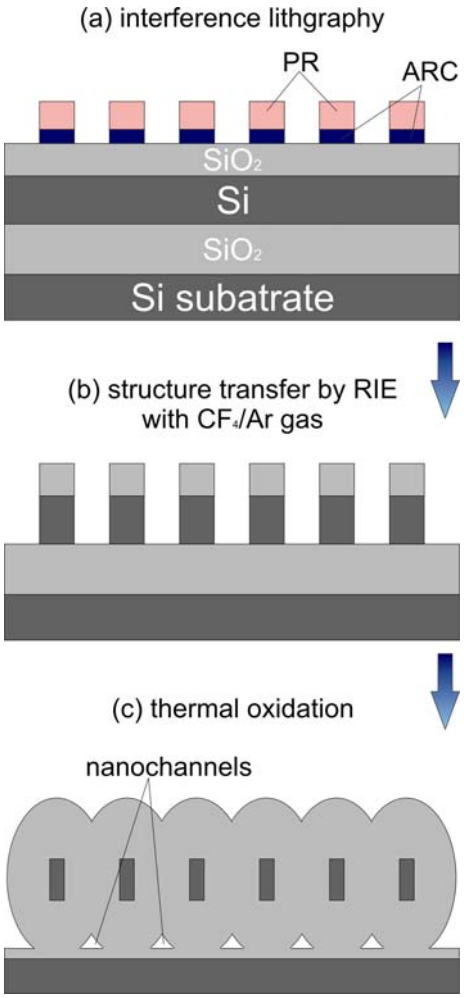

Figure 64: Schematic diagram of the fabrication procedure for horizontally aligned nanochannel arrays on SOI wafers. (a) PR and ARC were patterned into lines and spaces structures by LIL on the SOI substrate; (b) Structure transfer by RIE with CF_4/Ar gases until the SiO_2 interlayer; (c) Thermal oxidative self-sealing of the grooves into nanochannels.

Figure 65a shows a representative SEM image of the as-prepared SOI wafer prior to the oxidative self-sealing. Due to the structure transfer by RIE, the grooves have widths of 180 nm at the top and 120 nm at the bottom. The depth of the grooves is 550 nm and the periodicity is 410 nm. Figure 65b shows a SEM image of a sample kept at 950 °C for 2

hours. The silicon bars (dark areas) are surrounded by SiO_2 shells (light grey areas). The sealing was not complete at this stage, but the retardation effect at concave corners is very apparent. The oxide is thinner at the bottom and thus the diameter of the remaining hollow space is larger than above. The self-sealing of the grooves is complete if the sample was oxidized at 1000 °C for 3 hours (Figure 65c and d). The cross-section of the hollow channels appears as black spots in the SEM images. As evident from the magnified image shown in Figure 65d, they exhibit triangular shape in cross-section, the same as in the case of (110) wafers introduced above. The edges parallel to the initial Si/SiO_2 interface have a length of ~50 nm and the height of the channels is 60 nm.

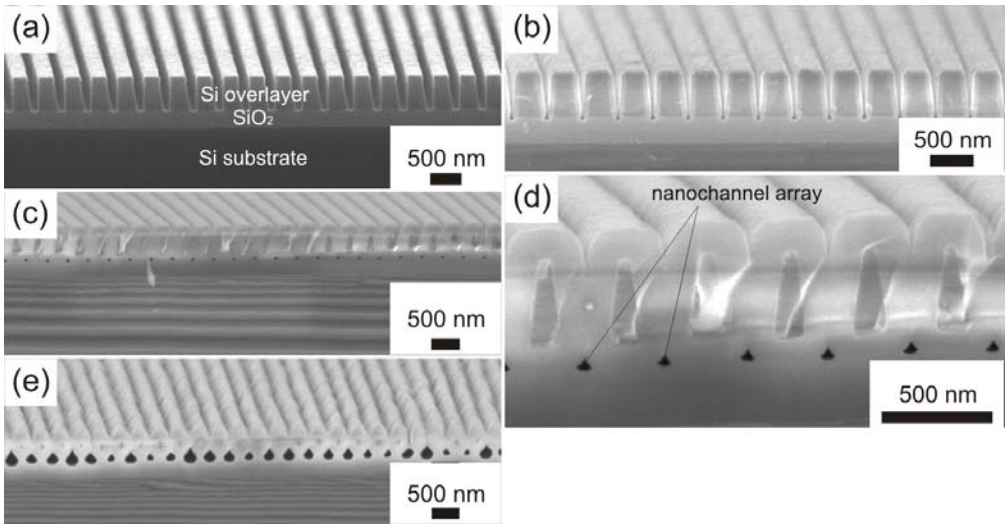

Figure 65: SEM images of (a) nanogroove structures in SOI wafer prior to the oxidation; (b) wafer oxidized at 950 °C for 2 hours, the grooves are not completely sealed; (c) and (d) wafer oxidized at 1050 °C for 3 hours, the grooves are completely sealed, in overview and magnified image, respectively; (e) the channels widened by performing post-oxidative etching and a subsequent second oxidation at 1000 °C for 4 hours.

For the both approaches introduced above, the (110)-orientation or SOI substrate, it is obvious that the locations and the periodicity of the nanochannels could be adjusted by the process conditions of LIL and thermal oxidation. However, they are only suitable for the fabrication of channels with dimensions of sub-50 nm, because the retardation of oxide growth at the concave corners provides only tiny difference from that at the flat surface. A post-oxidative etching with HF solution step allows widening of the channels. As can be seen in Figure 65e, the sample in Figure 65c containing horizontal

nanochannels was etched with a 5 wt-% aqueous HF solution for 3 min at room temperature to remove the SiO_2 formed during the oxidization step. The periodicity of the pattern remained unaltered and the thickness of the silicon walls between the grooves decreased to 130 nm. In addition, due to the isotropic etching of SiO_2 in HF solution, also the SiO_2 interlayer of the SOI wafer was etched and therefore channels were formed directly under the silicon grooves in the SiO_2 layer. We sealed the grooves by oxidizing the wafer again at 1000 °C for 4 hours in air. The resulting horizontal nanochannels exhibit also triangular shape in cross-section. The edge length increased to ~240 nm and the height of the channels to 300 nm.

5.3 SACRIFICIAL RESIST FOR NANOCHANNEL ARRAYS

The two previous approaches seem to be only suitable for the fabrication of channels with profile dimension in the sub-30 nm range and the scalability of the channel dimensions thus is limited. In many cases, films and structures are used intermittently, only to be disposed of in the next process step. However, sacrificial layers enable more complex structural shapes than standard top-down patterning. An alternative method for the fabrication of horizontal hollow nanochannel arrays is the use of a sacrificial material, the so called “place-holder”. There are many examples of sealed channels that have been made with sacrificial materials such as polysilicon, [130] heat-depolymerizable polycarbonate (HDP) [131,132] or polynorbornene (PNB) [121,133]. The basic idea is simple: the sacrificial material is patterned into the desired shape on a surface by conventional lithography techniques, such as optical lithography and EBL; the patterned sacrificial material layer is subsequently covered using a capping layer, which is typically SiO_2, Si_3N_4 or polyimide; the sacrificial material is then removed either chemically or by thermal decomposition.

In this work, the PR and ARC for LIL have been employed as sacrificial polymer for the fabrication of horizontally aligned nanochannel arrays on silicon wafers (Figure 66). Conventional thermal vapour deposition and atomic layer depositon (ALD) techniques have been used to deposit capping layer materials, such as TiO_2, Al_2O_3 and SiO_2. A disadvantage of the chemical removal of sacrificial materials is that it usually requires a lengthy immersion in solvent or another chemical solution, and therefore narrow holes

may be necessary to dissolve the sacrificial materials in a reasonable period of time. To avoid these complications, the sacrificial PR and ARC are removed in this work by means of thermal decomposition.

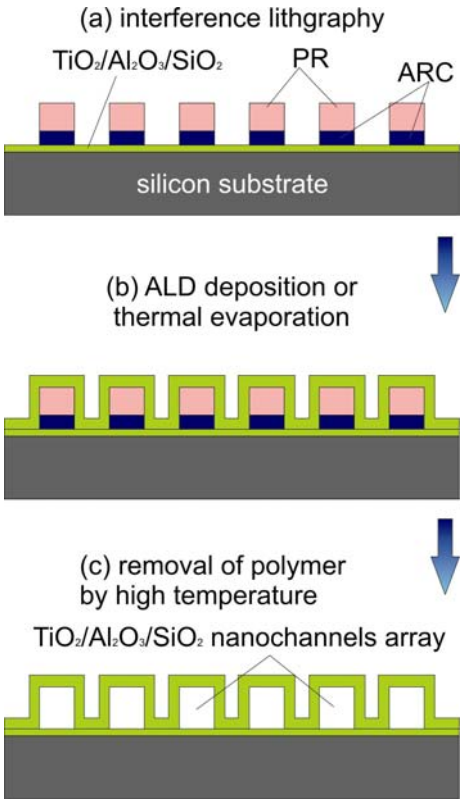

Figure 66: Schematic diagram of the fabrication procedure for horizontal nanochannel arrays on silicon wafer. (a) PR and ARC were patterned by LIL into lines and spaces structure on the substrate surface; (b) Thermal vapor deposition or ALD was employed for the deposition of capping materials; (c) Hollow nanochannel array was obtained by thermal decomposition of PR and ARC at high temperature (T = 800 C°).

First on the silicon wafer surface, a layer of capping material was deposited in order to reduce the possible deformation difference due to the thermal expansion between substrate and capping materials, which might lead to a destruction of the nanochannels during thermal decomposition of the sacrificial PR and ARC. Then PR and ARC were spin-coated on the substrate surface and patterned into lines and spaces structures with desired feature sizes by LIL. Capping materials were deposited by means of various deposition techniques and the sacrificial resist stack (PR and ARC) was subsequently removed at a high temperature (T = 800 C°).

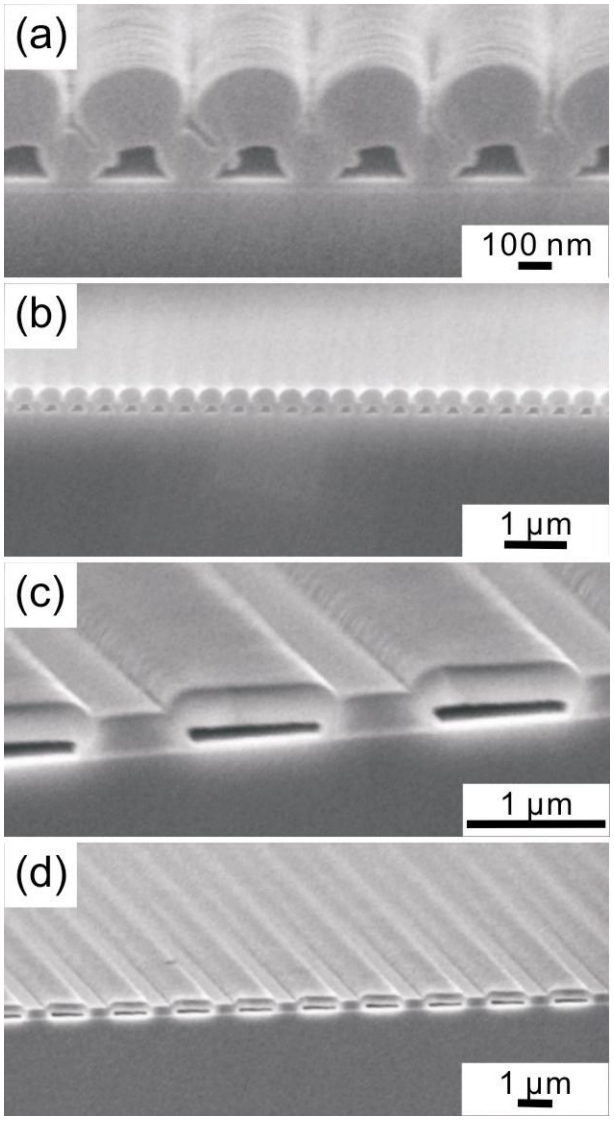

Figure 67: SEM images in oblique-view of (a) and (b) SiO_2 nanochannel array with a period of 370 nm; (c) and (d) SiO_2 nanochannel array with a period of 1250 nm.

Figure 67 shows the SEM images of horizontal SiO_2 nanochannel arrays fabricated by the LIL-controlled sacrificial-resist method. The capping material, SiO_2 was deposited by thermal vapor deposition on the resist structures generated by LIL. The nanochannel array with a channel width of 210 nm, a height of 120 nm and a periodicity of 370 nm can be seen in Figure 67a and b in detailed view and overview, respectively. The initial sacrificial resist structures have the same periodicity and channel width, whereas the height of the PR and ARC structure was 190 nm in total. Figure 67c and d show the

nanochannel array with a 750 nm width, 100 nm in height and a 1250 nm periodicity. Compare to the initial resist structure, the width and the periodicity of the channels were not changed after thermal decomposition, only the height decreased from 190 nm to 100 nm. In addition, an irregular shape of the channel profiles can be observed apparently from the detailed images (a) and (c). According to the investigations of the structures before thermal decomposition, which have the same profiles as that after high temperature treatment, we contribute this irregular profile to the deformation of the polymers during the thermal vapor deposition of SiO_2 due to the too high temperature on the sample position in the chamber.

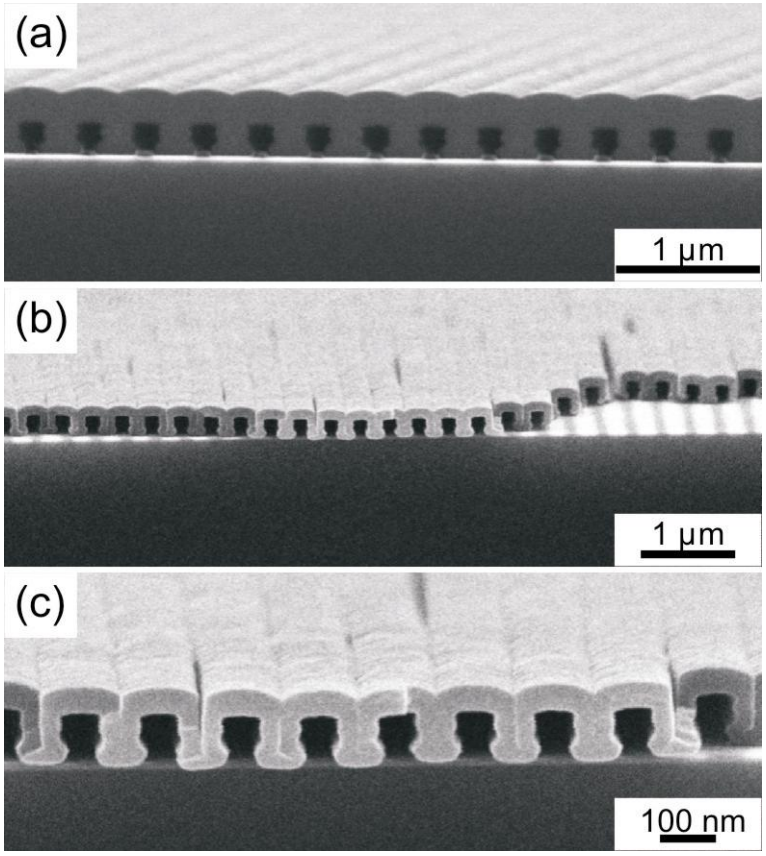

Figure 68: SEM images of (a) photoresist grating structure covered by TiO_2 layer, which was deposited by ALD method at room temperature; (b) and (c) hollow TiO_2 nanochannel arrays after removal of sacrificial resist by high temperature in oblique-views.

As introduced in section 3.2.1, ALD allows the deposition of a homogenous layer of TiO_2, SiO_2 and Al_2O_3 etc. on complex topography at room temperature. This advantage of ALD is beneficial for the deposition of capping layers on the sacrificial resist

structure in our approach. In this work, we produced TiO_2 nanochannel arrays deposited by ALD at room temperature. Figure 68 shows SEM images of a nanochannel array before and after removal of the resist. Form the cross-section views we can observe that the TiO_2 capping layer kept faithfully its profiles after high temperature treatment. We have dipped one side of the sample into distilled water and observed that the water traces went very smoothly up. The capillary action in the channels has demonstrated the quality of the hollow channels across the entire wafer. With this approach, the arrangement of the channels is defined by LIL exposure and the profile of the channels could be controlled by the resist stack design.

5.4 SUMMARY

With single exposure by LIL, the grating structures have been introduced into the fabrication of fin-like, groove and channel structure arrays. The oxidative size-reduction strategy has been employed to extend the available resolution of widths of fin-like structures and grooves, which could compare with those obtained by EBL. The non-uniform oxidation of Si structure at corners allows the fabrication of horizontally sealed hollow nanochannel arrays with a profile diameter less than 30 nm. A different method for the fabrication of nanochannel arrays with larger profile diameter has also been developed based on resist grating structures. The resist grating structure arrays were covered with thermally-stable materials, such as SiO_2 and TiO_2, by thermal evaporation and room temperature ALD, respectively, and subsequently removed by high temperature treatment. In this way, nanochannel arrays defined by LIL with different dimensions have been obtained and can be used as templates for the deposition of novel nanotubes with square-shaped profiles and application in such as MEMs and microfludics.

6 CONCLUSIONS

This dissertation is summarized with a schematic illustration in Figure 69. In Chapter 2, the fundamentals, the experimental setup and exposure results of laser interference lithography (LIL) have been introduced. With Lloyd's-Mirror Interferometer, periodic nanostructures, such as grating, hole and dot arrays, with a resolution of sub-100 nm and period ranging from 200 nm to 1.5 μm have been obtained over 4 inch wafer areas. They were introduced for the first time into different application fields and showed their unique conveniences and advantages.

LIL-generated holes and grating templates have been used for the deposition of nanowire and nanoring arrays. Perfectly ordered metallic nanowire arrays with length across the entire wafer were obtained, which could benefit to the characterization of properties. Lithographically controlled nanoring arrays, even with elliptical shapes, were also achieved and the magnetic properties of Ni and Permalloy elliptical ring arrays were investigated.

The 2D periodic nanostructures with different arrangements and periodicties were employed to define the structures of Si_3N_4 and Ni imprint stamps for the prestructuring of aluminium surface prior to the anodization processes. The flexibility and high throughput of LIL for the fabrication of imprint stamps with periodic structures were thus demonstrated. Long-range ordered porous alumina membranes were obtained with imprint guided anodization process.

The grating structures generated by single exposures were transferred into silicon. The oxidative size-reduction strategy was introduced to decrease the dimensions of grating structures. In this way fin-like structures and nanogroove arrays with a resolution of sub-20 nm, which is comparable with structures written by EBL, and even sealed nanochannel arrays were fabricated in parallel. In combination with atomic layer deposition (ALD) or thermal evaporation of capping materials, the grating structures were also directly used as sacrificial structures for obtaining of horizontal hollow nanochannel arrays with square profiles, which could been employed as novel templates

for the synthesis of nanotube arrays with these profiles.

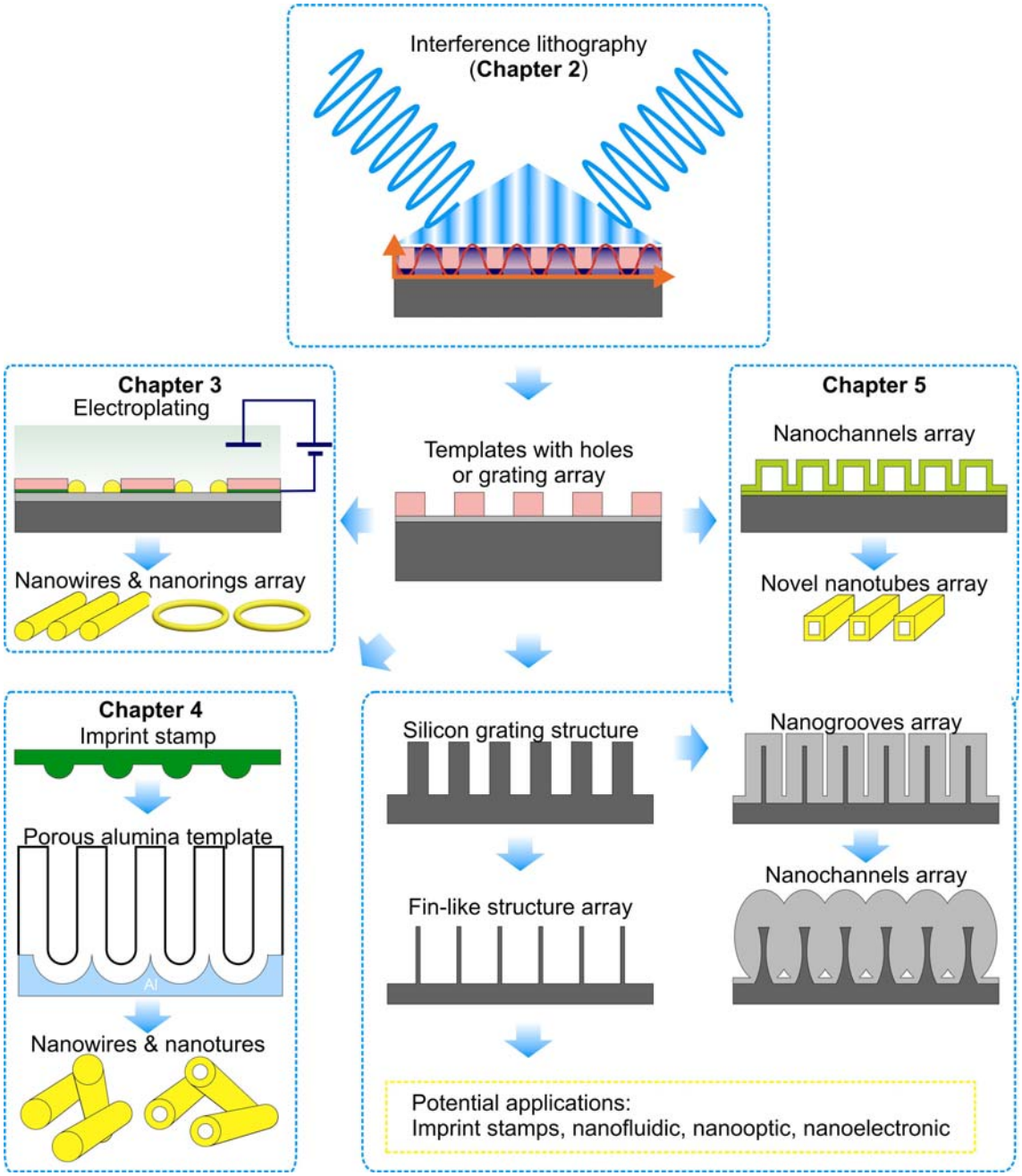

Figure 69: Conclusions of this dissertation: The fabrication of periodic nanostructure by using laser interference lithography and their applications.

7 OUTLOOK

For possible future work, the following research ideas are proposed which are based on this dissertation:

- Lasers with shorter wavelengths will be employed for the LIL, such as a solid state laser (266 nm) or a argon-ion laser (244 nm), which theoretically allows the generation of smaller period of the structures down to 133 nm and 122 nm, respectively.

- A series of samples of elliptical-shaped magnetic nanoring arrays with different aspect ratios can be fabricated and the magnetic properties can be systematically investigated.

- Combination with the smaller period of the structures obtained by the new lasers, imprint stamps with smaller lattice constant can be developed and therefore large-scale perfectly ordered AAO membrane with a shorter D_{int} can be obtained.

- In combination with ALD and/or electrodeposition techniques, the nanochannel structures can be used as templates for the synthesis of planar arranged nanowire and nanotube arrays and their properties can be investigated.

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APPENDIX: SPIN-CURVES OF PR AND ARC

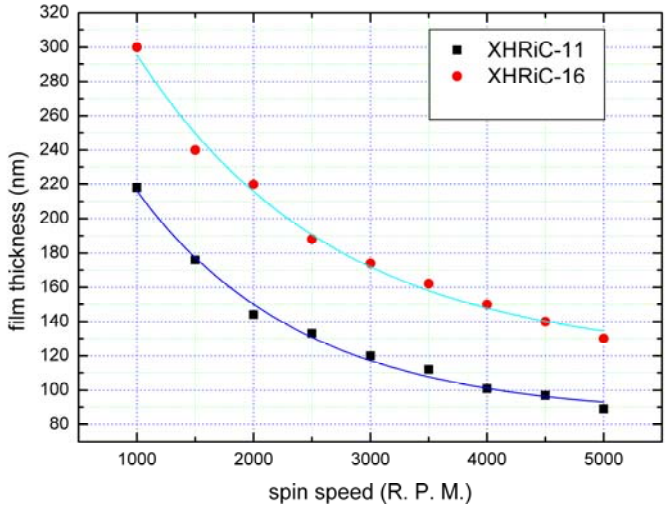

Figure 70: Spin-curve of BS ARC XHRiC.

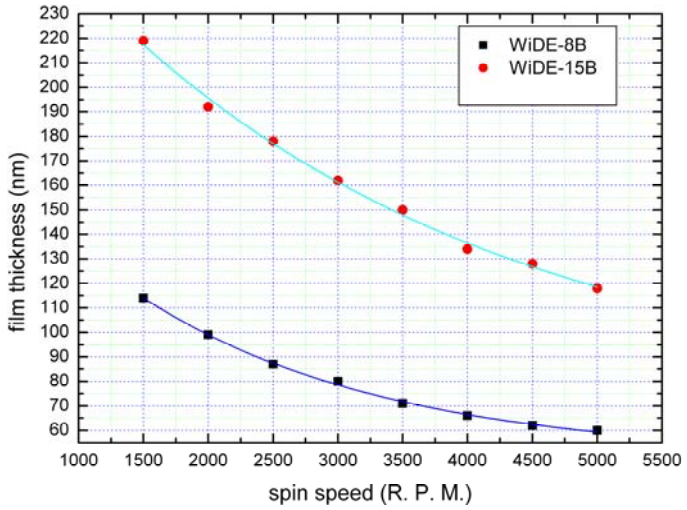

Figure 71: Spin-curve of BS wet-developable ARC WiDE.

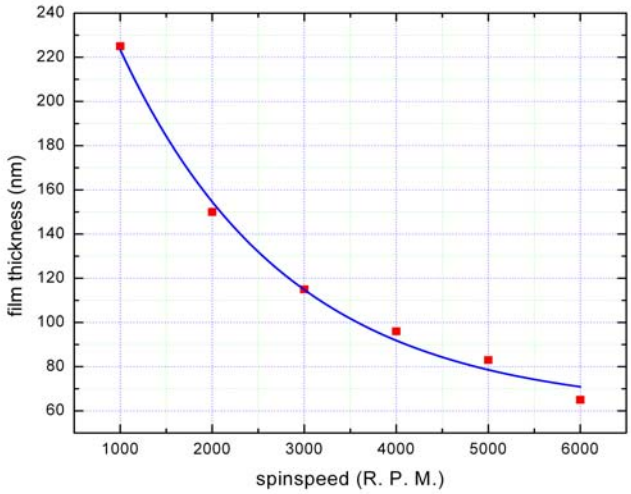

Figure 72: Spin-curve of OHKA positive resist AR-80.

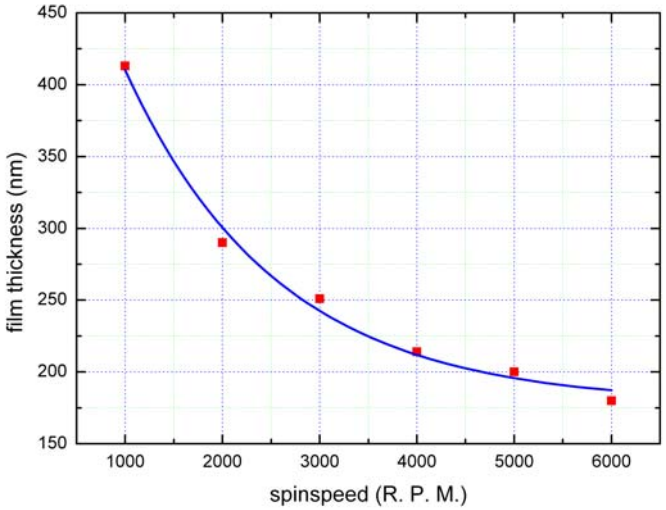

Figure 73: Spin-curve of OHKA negative resist TSMR-iN027.

CURRICULUM VITAE

First Name	Ran
Family Name	Ji
Date (Place) of Birth	Dec. 06, 1977 (Liaoning, China)
Nationality	Chinese

EDUCATION

Mar. 2004 – May. 2007	Max-Planck-Institute of Microstructure Physics Martin-Luther-University Halle Wittenberg, Germany Ph.D. Candidate (Supervisors: Prof. Ulrich Gösele and Prof. Kornelius Nielsch)
Oct. 2001 – Feb. 2004	Rheinisch-Westfälische Technische Hochschule Aachen, Germany M.Sc. in Materials Science Thesis: Developemnt of the process technology for Soft-UV-nanoimprint lithography (Supervisors: Prof. Heinrich Kurz and Dr. Markus Bender)

Sep. 1996 – Jul. 2000	Beijing University of Science and Technology, China
	Bachlor –Eng. in Materials Science

PROFESSIONAL EXPERIENCES

Jun. 2007 – present	NIL Technology ApS, Kongens Lyngby, Denmark
	Production and R&D Engineer
Feb. 2002 – Feb. 2003	Fraunhofer Institute of Laser Technology Aachen
	Research assistant
Sep. 2002 – Feb. 2004	Advanced Microelectronics Center Aachen (AMICA)
	Research assistant

AWARD

Sep. 2005	Third Place in the "Micro- & nano-graph contest" of the 31st international conference "Micro- and nano-Engineering (MNE) 2005" in Vienna, Austria

PUBLICATION LIST

- M. Bender, U. Plachetka, **R. Ji**, A. Fuchs, B. Vratzov, H. Kurz, T. Glinsner, F. Lindner, "High resolution lithography with PDMS mold". *J. Vac. Sci. Technol. B.,* **22** p.3229-3232 (**2004**);
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- X. Chen, R. Zhang, **R. Ji**, R. Scholz, M. Steinhart, K. Nielsch, M. Zacharias, U. Gösele, "Versatile manipulation of Si nanocrystals aligned in silicon dioxide via alternating SiO_x/SiO_2 deposition". In preparation;
- **R. Ji**, M. Knez, K. Nielsch, U. Gösele, "Fabrication of ideally ordered nanoring arrays over wafer-scale area based on laser interference lithography and templated atomic layer deposition". In preparation.

PRESENTATION LIST (SELECTION)

- R. Ji, W. Lee, R. Idris, C. A. Ross, U. Gösele, K. Nielsch, "Fabrication of imprint master based on interference lithography for controlling the growth of porous alumina". 31st International Conference on Micro- and Nano-Engneering (MNE) 2005, Vienna, Austria. 19. -22.09.2005, Talk;
- R. Ji, W. Lee, R. Scholz, U. Gösele, K. Nielsch, "Kill two birds with one stone: Templated fabrication of nanowire and nanoring arrays based on interference lithography and electrochemical deposition". 32nd International Conference on Micro- and Nano-Engneering (MNE) 2006, Barcelona, Spain. 17. -20.09.2006, Poster;
- R. Ji, X. Chen, R. Scholz, U. Gösele, K. Nielsch, "Fabrication of wafer-scale arrays of silicon nanofins and silica nanochannels based on interference lithography and oxidation size-eduction strategy". 32nd International Conference on Micro- and Nano-Engneering (MNE) 2006, Barcelona, Spain. 17. -20.09.2006, Poster;
- R. Ji, M. Knez, T. Xie, A. Frommfeld, P. Werner, U. Gösele, K. Nielsch, "All roads lead to Rome: Two methods for the fabrication of perfectly ordered circular or elliptical nanoring arrays based on interference lithography". 32nd International Conference on Micro- and Nano-Engneering (MNE) 2006, Barcelona, Spain. 17. -20.09.2006, Talk;
- R. Ji, W. Lee, M. Knez, R. Scholz, U. Gösele, K. Nielsch, "Templated fabrication of nanoring arrays based on interference lithography". 2006 MRS Fall Meeting, Boston, USA. 27.11 – 01.12.2006, Talk.
- R. Ji, W. Lee, M. Knez, R. Scholz, U. Gösele, K. Nielsch, "Templated fabrication of nanoring arrays based on laser interference lithography". 33rd International Conference on Micro- and Nano-Engneering (MNE) 2007, Copenhagen, Denmark. 23. -26.09.2007, Talk;

PATENT

- W. Lee, K. Nielsch, U. Gösele, **R. Ji**,
  "A method of manufacturing a self-ordered porous structure of aluminium oxide, a nanoporous article and a nano object".
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Hiermit erkläre ich, dass ich keine anderen als die von mir angegebenen Quellen und Hilfsmittel zur Erstellung meiner Dissertation verwendet habe. Den benutzten Werken wörtlich oder inhaltlich entnommene Stellen sind als solche gekennzeichnet.

Ran Ji

Halle (Saale), den 17.03.2007