Transport properties of $LaAlO_3/SrTiO_3$ nanostructures

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Dedicated to my Nadia

Contents

List of Abbreviations and Symbols

2DEG	Two Dimensional Electron Gas
□	Square area
AFM	Atomic Force Microscope
AlO_x	Alumina (aluminium oxide)
Au	Gold
BHF	Buffered fluoric acid
CCD	Charged-Coupled Device
DAC	Digital-Analog-Converters
e-beam	Electron beam
FET	Filed-Effect-Transistor
ICP	Inductively Coupled Plasma
I_D	Drain current
I_G	Gate current
LAO	$LaAlO_3$
LSMO	$LaSrMnO_3$
MBE	Molecular Beam Epitaxy
μ	Carrier mobility
n_s	Carrier density
PLD	Pulsed Laser Deposition
PO_2	Oxygen partial pressure
Pt	Platinum
R_{ref}	Reference resistor
R_{total}	Total resistance
RHEED	Reflection High Energy Electron Diffraction
RIE	Reactive Ion Etching
RSM	Reciprocal Space Map
SET	Scanning Electron Transistor
SQUID	Superconducting QUantum Interference Device
STO	$SrTiO_3$
T_{C1}	Upper phase transition temperature (105 K)
T_{C2}	Lower phase transition temperature (65 K)
TEM	Transmission Electron Microscopy
Ti	Titanium
T_{min}	Minimum temperature
T_{peak}	Peak temperature
uc	Unit cell
UV	Ultraviolet
W	Effective width
w_d	Depletion width
XRD	X-ray Diffraction

Chapter 1

Introduction

1.1 Motivation

Silicon-based electronics has been serving as a backbone of the modern industry for several decades, and has great influence on our daily lives. To operate the daily life electronics including cellular phone, cars, cameras, kitchen appliances and computers, about 10^{19} microscopic electronic switches are manufactured each year. With the passage of time, devices are becoming smaller, more efficient and cheaper. The constant speed of scaling proposed by Moore's law, that "the size of the device will be half every two years" is now approaching its limit. In order to sustain this scaling down procedure it is necessary to introduce new materials. Moreover, the new materials system should be capable to fulfill the future technological demands like multifunctional, more intelligent, and faster devices [1–3].

Complex oxide is a class of material, which has been extensively studied in the last few decades. Oxide materials incorporate many electronic properties of semiconductors. In addition, other interesting properties like high-temperature superconductivity (in Y-Ba-Cu-O compound) [4], colossal magnetoresistance (in $La_{2/3}Ba_{1/3}MnO_x$) [5], strain-driven ferroelectricity (in strained $SrTiO_3$) [6], interfacial conductivity and ferromagnetism (in $LaAlO_3/SrTiO_3$ heterostructures) [7, 8] and quantum Hall effect (in $ZnO/Mg_xZn_{1-x}O$ heterostructures) [9] have also been reported in the oxide materials. All these intriguing properties made the oxide materials a candidate for future multifunctional oxide electronics in the areas of memories, logic and sensor applications.

In the beginning, due to chemical complexity of oxide materials, the main challenge was the growth of high quality oxides film required for devices. For high-performance devices, it is essential to have a low defect density, because these defects can trap electrons and as a result the performance of the device is reduced [10, 11]. But with the advancement of

modern deposition techniques including pulsed laser deposition (PLD), molecular beam epitaxy (MBE) and in-situ monitoring up to unit cell level with reflection high-energy electron diffraction (RHEED), it became possible to deposit individual atomic layer. These modern deposition techniques brought a boost in the field of oxide electronics.

"The interface is the device", a well known quote used by Herbert Kroemer in his Nobel address [12], is not only true for semiconductor but also equally important for correlated oxides. Amongst other oxide heterostructures, the $LaAlO_3$ (LAO)/$SrTiO_3$ (STO) heterostructures has been intensively studied since last decade. The discovery of two-dimensional electron gases (2DEG) at the interface of two band insulators (LAO and STO) has initiated a huge effort to study this interface in detail [7]. Beside the interface conductivity, other intriguing properties such as induced ferromagnetism [8], superconductivity [13, 14] and thickness dependent electric-field-induced metal-insulator transition [15] have been reported. Due to all these properties, LAO/STO interface became a model system to study the fundamental physics of strongly correlated electronic systems, and also a candidate for technological applications.

Despite such intensive study of the LAO/STO interface, the underlying physics and the origin of interfacial conductivity and magnetism is still debatable. To utilize this interface into a device, nanometer-scaling of the oxide devices have been demonstrated by using conducting Atomic Force Microscope (AFM) probe through the use of phase changes [16]. Field-effect devices have also been demonstrated by back and top-gating using the 2DEG at the LAO/STO interface as drain-source channels [17–20]. However, all the reported techniques for patterning LAO/STO have some limitations and they are also not industry compatible. In order to utilize these interfaces into nanopatterned quantum transport devices, it is crucial to further explore the underlying physics, and also to develop a fully industry compatible, reliable and reproducible patterning technique.

The aim of this work is to develop an industry compatible nanopatterning technique to pattern the LAO/STO interface in Hall bar geometry and then explore the properties of LAO/STO interface in nanostructured sample. Nanostructures are also patterned by using the old patterning technique with some modifications and optimized parameters to check the reliability of newly developed patterning technique. During this work, new and important aspect of the LAO/STO interface such as the effect of structural transition of the STO substrate on the transport properties of the 2DEG at the LAO/STO interface is also explored. The experimental procedure, important parameters and results are discussed herein this thesis work.

1.2 Outline of the thesis

Chapter 2 starts with a brief introduction to the bulk properties of LAO and STO, which are the main building blocks of the LAO/STO interface. Both materials have perovskite crystal structure and in bulk, both are band insulators. The perovskite structure has the chemical formula ABO_3, which can be considered as a stacking of alternating AO and BO_2 layers. When LAO is deposited on single TiO_2 terminated STO substrate, with LaO/TiO_2 stacking 2DEG is formed. The conducting interface between two insulators made this interface a model system to study the fundamental physics of strongly correlated electronic system. The interfacial conductivity is explained by different models, including polar discontinuity at the interface, formation of oxygen vacancies in the STO substrate, and cation intermixing, which are discussed in this chapter.

Chapter 3 deals with the experimental techniques used in this thesis for the fabrication and characterization of the LAO/STO interface. Starting from the preparation of the STO substrate to get single TiO_2 terminated STO substrate, deposition of LAO layer by pulsed laser deposition (PLD) with in-situ monitoring by reflection high-energy electron diffraction (RHEED) up to unit cell level, are explained in this chapter. Structural and stoichiometric quality of the deposited films are characterized by X-ray diffraction (XRD) and transmission electron microscopy (TEM). In the last part of this chapter electronic transport measurement setup that is used during the course of this thesis is explained.

After successful preparation and characterization of LAO/STO heterostructures, the next task was the nanopatterning of the LAO/STO heterostructures. Chapter 4 starts with a brief review of all the patterning techniques which are reported in the literature so far and their possible limitations. In the next part, the newly developed direct patterning technique is presented, which is fully industry compatible. This technique uses e-beam lithography in combination with dry etching to pattern the LAO/STO heterostructures down to 100 nm. The resulting patterned structures are stable at ambient conditions. The process leaves the substrate insulating and preserves the conductivity of the electron gas except for a narrow depletion region. Some nanostructured samples down to 100 nm are also patterned by sequential deposition of LAO layers. The transport properties of both kind of sample patterned by different technique are compared at the end of this chapter.

The effect of phase transition of the STO substrate on the transport properties of the LAO/STO interface is described in Chapter 5. At room temperature, STO has a cubic crystal structure. At low temperature, T=105 K due to the rotation of oxygen octahedra structural transition from cubic to tetragonal takes place, as a result domains are formed within STO. These domain walls move with the application of gate voltage and lead to channeled cur-

rent flow between domains or at the domain walls. The correlation between the interface conductivity and the local structure is explored in this chapter. Transport properties of the patterned LAO/STO interface in nano Hall bars are studied in the region where the structural transitions take place. A huge increase in sheet resistance of the nanostructured sample is observed near the transition temperature, which may be attributed to filamentary current flow due to the structural transition of the STO substrate.

Chapter 6 describes the possibility of using the LAO/STO interface as a field-effect device. There are two common methods of gating namely, top-gating and back-gating. In top-gating, the electrical field is applied from the top and a thin LAO layer is used as gate dielectric, whereas in back-gating the electrical field is applied from back and a thick STO substrate is used as gate dielectric. Back-gating is a global technique, and several hundred of volts are required to achieve a reasonable effect. To resolve these issues, the top-gating technique is used to fabricate the field-effect devices.

In the final Chapter 7, the important results and outcome of the thesis is summarized, and some remaining questions are stated, which can be regarded as an outlook towards the future study.

Chapter 2

An overview of the $LaAlO_3/SrTiO_3$ interface

"The interface is the device", a well known quote used by Herbert Kroemer in his Nobel address [12], is not only true for semiconductor, but also equally important for correlated oxides, which emphasizes that the functionality of many devices originate from the physics at the interface. It is especially true for the $LaAlO_3$ (LAO)/$SrTiO_3$ (STO) system studied in this thesis. It is necessary to know the bulk properties of the constituent materials, before the exploration and identification of the interface effects in the heterostructures.

This chapter deals with the oxides that are used in this work, discussing their structural, electronic and magnetic properties in detail. After a brief introduction about perovskites, the constituent materials of LAO/STO interface are explained. In bulk, both materials are band insulators. Later, the LAO/STO interface is explained, which is found to be metallic. In order to explain the possible origin of the conducting interface, the last part of the chapter discussed different models like polar discontinuity, formation of oxygen vacancies at the STO substrate and cation intermixing.

2.1 Perovskites

A perovskite is a material having the general chemical formula ABX_3, where A stands for a large cation, B for a small cation, and X for an anion that bonds to both A and B. The term "perovskite" originates from the mineral perovskite calcium titanium oxide ($CaTiO_3$), which is named after a Russian mineralogist, Court Lev Aleksevich von Perovski. The mineral was first discovered and named by Gustav Rose in 1839 in Russia. The anion X is usually oxygen or a halogen (in this work X will always be oxygen therefore it is replaced by O

in the general formula). Perovskites are chemically diverse; the diversity depends upon the choice of elements on A or B positions, the stabilization of vacancies and the variation of oxygen stoichiometry [21].

The structure of an ideal cubic perovskite is shown in Figure 2.1a, where B cations are shown at the corner of the cube, A cation in the center and O ions in the middle of the cubic edges. The perovskite structure can be illustrated as a network of corner-sharing BO_6 octahedra as shown in the Figure 2.1b. However, the real perovskite ABO_3 exhibits lattice distortion (octahedra are tilted around its centre), therefore resulting in the transformation of crystal structure like orthorhombic, tetragonal, rhombohedral, hexagonal and monoclinic [22]. These structural phase transitions are often observed as a function of external parameters like pressure or temperature. Perovskite materials exhibit many intriguing properties, such as colossal magnetoresistance, ferroelectricity and superconductivity due to interaction between charge, orbital, spin and external energies [23].

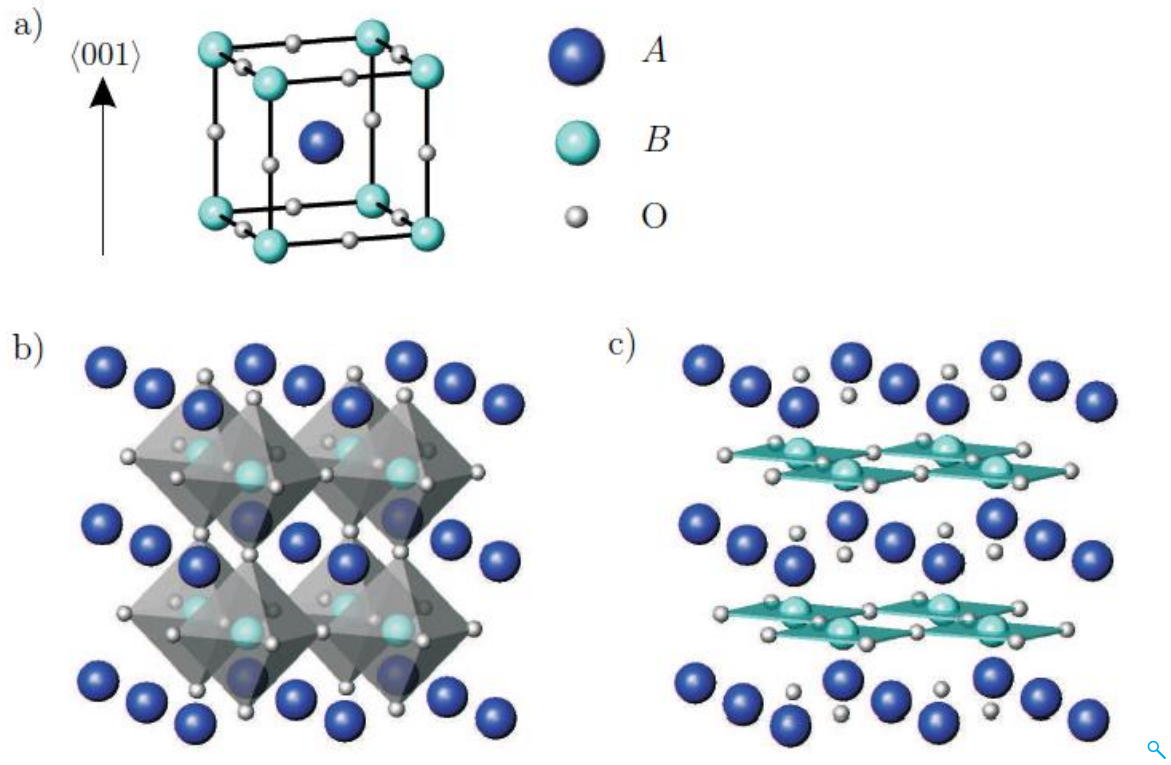

Figure 2.1: Schematic illustration of the perovskite ABO_3 structure. (a) B cation are shown at the corner of the cube, A cation in the center, and O ions in the middle of the cubic edge. (b) Perovskite structure as a network of corner-sharing BO_6 octahedra. (c) The ABO_3 compounds can be seen as a stacking of alternating AO and BO_2 layers [24].

Moreover, along the (001) direction a perovskite can be seen as a stacking of alternating

AO and BO_2 layers as shown in the Figure 2.1c. Later in this chapter, we will use this description of the perovskite structure, to understand the formation of 2DEG at the LAO/STO interface [24].

In this work, STO and LAO have been extensively studied and utilized for interfaces. Both compounds belong to the class of perovskites. In the following sections, these two compounds will be explained in detail.

2.2 $LaAlO_3$: lanthanum aluminate

The LAO, the main building block for the LAO/STO interface is thoroughly investigated in this thesis. In this work, LAO thin film is deposited by pulsed laser deposition technique from a single LAO crystal on STO substrate. In the following subsections, the crystal structure and electronic properties of the LAO will be discussed briefly.

2.2.1 Crystal structure

At high temperature, LAO has cubic peroskite crystal structure with the space group $Pm\bar{3}m$, whereas at low temperature (around ≈ 813 K), the structural transition take place to rhombohedral distorted perovskite with the space group $R\bar{3}c$ [25]. This occurs due to antiphase rotation of the AlO_6 octahedra. At room temperature, the pseudocubic unit cell has a lattice constant of 3.790 Å [26]. Like other perovskites, LAO is also used as a single crystal substrate for epitaxial thin-film growth of many ferroelectric and high-T_c superconductors, due to matching lattice parameter and thermal expansion, chemical compatibility and high crystal quality [27].

2.2.2 Electronic properties

LAO is an electrical insulator with wide band of 5.6 eV [28]. It is high-κ oxide, having dielectric constant of about 24 in the temperature range from room temperature to 4 K. LAO retains high dielectric constant even in the amorphous state. Due to such high dielectric constant, it is used as gate dielectric in Si-based electronic devices [29]. Recently, LAO is also used as a gate dielectric in LAO/STO based field effect devices [18–20, 30].

2.3 $SrTiO_3$: strontium titanate

Strontium titanate, STO is a complex oxide material with perovskite structure. Due to its remarkable array of properties it has been extensively and continuously studied since 1940s. STO is the universal substrate for many oxide materials due to similarities in structure and lattice parameters. For example, high-T_c superconductors [31], colossal magnetoresistance oxides [32] or ferroelectrics are epitaxially grown on $SrTiO_3$ substrate. Moreover, it is chemically inert and does not react with deposited materials. STO is used as a substrate for the formation of LAO/STO interface.

2.3.1 Crystal structure

At room temperature, STO has cubic crystal structure (space group $Pm\bar{3}m$) with a lattice constant of 3.905 Å. The cubic structure consists of a small titanium atom at the center and oxygen atom in each of the six cube walls forming a cage around a titanium atom, and small strontium atoms at the corners of the cube [33]. At low temperature due to the rotation of TiO_6 octahedra, at about 105 K the crystal structure becomes tetragonal and at 65 K the structure becomes orthorhombic and at 10 K possibly rhombohedral [34]. As shown in the Figure 2.1c, the STO crystal lattice can be imaged as a stacking of alternating layers of SrO and TiO_2. Commercially available (001) surface of mechanically polished STO substrate has mixed termination, however, single TiO_2 termination can be achieved by treating the substrate first with water and then with buffered fluoric acid (BHF) followed by annealing in oxygen atmosphere at high temperature. This single TiO_2 terminated, structurally and chemically well-defined STO substrate is perfect starting point for the growth of LAO/STO interface.

2.3.2 Magnetic and dielectric properties

STO is non-magnetic and its magnetic susceptibility is partly diamagnetic and partly (Van Vleck) paramagnetic. Both parts are approximately temperature-independent [35, 36].

STO has exceptional dielectric properties. In its pure and unstressed form, it is an incipient ferroelectric and remains paraelectric down to 0.3 K, although the slight perturbation in the lattice can disturb the delicate state, resulting in ferroelectricity. The perturbation originates from various sources such as epitaxial strain [6] nonstochiometry [37] and doping [38] or even by oxygen isotope substitution [39].

The dielectric constant increases with decreasing temperature. The dielectric constant of STO is 300 at room temperature and increases extensively, up to 25000 in bulk samples [40]

and 4000 in thin films at 4 K [41]. In spite of such high dielectric constant, the material cannot be used as energy storage in high-κ capacitors, because the dielectric constant decreases by application of electric field [36].

Due to high dielectric constants and low microwave losses at cryogenic temperature, STO is an ideal candidate for electrically tunable microwave devices [42]. The value of high dielectric constant also makes STO a suitable candidate as gate dielectric in the field effect devices.

2.3.3 Semi- and superconducting properties

STO has a large, indirect band gap of 3.25 eV. Therefore, it can be regarded either as a band-insulator or a semiconductor. The insulating STO can be transformed into metallic by electron doping. Electron doping is achieved by introducing O vacancies, substituting La for Sr or Nb for Ti [43, 44]. The doped sample with electron carrier concentration 10^{18}-10^{21} carrier/cm^3 showed superconductivity with critical temperature < 300 mK [45, 46]. Moreover, the concentration of oxygen vacancies can be controlled in single crystal as well as in thin films. The glistening oxidized gem (STO crystal) is transformed into dull blue, conductive crystal by removing oxygen atoms from the crystal [47]. In the thin films, the oxygen vacancy concentration profiles of STO with subnanometer abruptness have been prepared and studied [48].

Electrostatic doping by utilizing the electric field-effect is another way to doping stoichiometric STO into conducting and superconducting state [49]. Electric double layer (EDL) gating can enhance sheet carrier densities from zero to 10^{14}/cm^2 in a pristine STO single crystal. A superconducting state also emerged below a critical temperature of 0.4 K due to this field-effect doping.

2.4 Two dimensional electron gas (2DEG) at the interface of two insulators

As described in the above section, the properties of both LAO and STO the building blocks of the LAO/STO heterostructure, are well known. Now the question arises, what will happen if the interface between two different complex oxides is fabricated, either the interface properties would be just the mixture of the bulk materials or the interface will have some unique and novel properties. This section deals with the formation of interface, when two band insulators are combined together. The novel and unique properties found at the LAO/STO

interface are not present in the bulk materials.

In 2004, A. Ohtomo and H. Y. Hwang discovered an electron gas at the interface between the two band insulators LAO and STO, which has initiated a huge effort to study this interface in detail [7]. As mentioned in the Section 2.1, the perovskite ABO_3 can be considered of an alternating stacks of AO and BO_2. They deposited two different stacking of LAO thin film on (001) oriented STO substrates by pulsed laser deposition (PLD). The schematic description of both kind of configurations is shown in the Figure 2.2. In the first configuration, LaO/TiO_2 interface, the LAO was directly grown on TiO_2-terminated STO substrate. However, for second configuration, AlO_2/SrO interface, an additional layer of SrO was deposited before the deposition of LAO. The film were deposited in an oxygen partial pressure p_{O_2} 10^{-6} mbar.

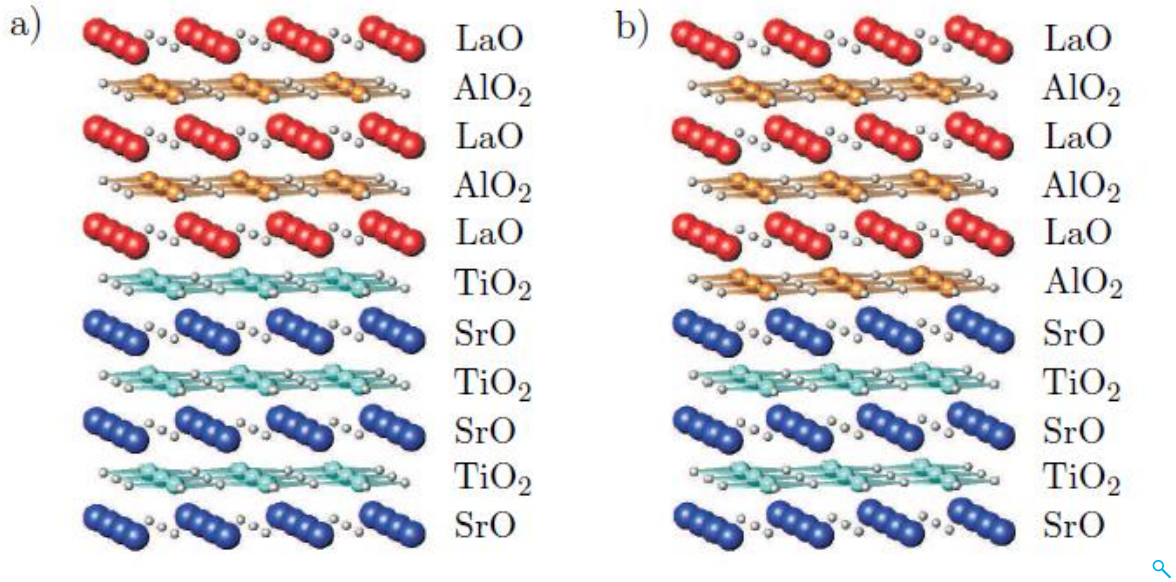

Figure 2.2: Schematic illustration of two different kind of configurations due to atomically abrupt interfaces between $LaAlO_3$ and $SrTiO_3$ in (001)orientation. La (red), Al (orange), Sr (blue), Ti (cyan), O (grey). (a) The films starts with a layer of LaO on the TiO_2 layer of $SrTiO_3$ to form n-type interface. (b) The films starts with a layer of AlO_2 on the last SrO layer of $SrTiO_3$ to form p-type interface [24].

Electronic transport measurements have revealed that one interface LaO/TiO_2 was conducting, whereas, the other AlO_2/SrO was found to be insulating. It is worth to do deep investigation to understand the mechanism of conducting interface. The stacking sequence has great effect on the properties of the interface, and also the interface between two insulators is conducting. To understand the mechanism of conduction, two building blocks LAO and STO are first considered separately. The formal valence states (La^{3+}, Al^{3+}, O^{2-}, Sr^{2+}, Ti^{4+}) differentiate the two interfaces depending on the stacking sequence. STO is composed

of alternating ($(SrO)^0$ and $(TiO_2)^0$) charged neutral layers, whereas, LAO is composed of alternating ($(LaO)^+$ and $(AlO_2)^-$) charged layers. So, the LAO/STO is a special interface where charge neutral and charged layers adjoin.

Later on, it is experimentally observed that there is a critical thickness d≥ 4 uc of LAO layer above which the interface is conducting [15]. However, 3 uc LAO interface is normally insulating, but can be switched by applying the gate voltage. Recently, the relationship between the strain and the electrical properties of the 2DEG at the LAO/STO is investigated that shows an increase in critical thickness with STO compressive strain [50]. Tensile and compressive strain has great influence on the conductivity of quasi-two-dimensional electron gas (q2DEG). Tensile strain eliminates it completely, whereas compressive strain reduces the carrier concentration. To understand the origin of the electrical conductivity, different models have been proposed; polar discontinuity at the interface, formation of oxygen vacancies in the STO substrate during the growth of LAO, and La, Sr intermixing at the interface. In the Section 2.5, these models will be explained.

2.4.1 Other intriguing properties of 2DEG

Besides interface conductivity other interesting properties have been reported such as induced ferromagnetism at the interface between the two non-magnetic insulating perovskites and superconductivity below 200 mK. In 2007, Brinkman et al. [8] have found the hysteresis in the magneto-transport measurements in $LaAlO_3$ and $SrTiO_3$ prepared under certain growth conditions, taking into account that the electronic and magnetic properties of LAO/STO are extremely sensitive to growth conditions. In the same year Reyren et al. [13] reported the superconducting electronic ground state with a transition temperature about 200 mK. This is not usual because superconducting ground state normally dismiss the magnetic ordering.

Later on, several groups have independently reported the existence of ferromagnetism and superconductivity simultaneously at the LAO/STO interface, using different experimental techniques [14, 51, 52]. The interpretation of coexistence of superconductivity and ferromagnetism is explained by presence of two types of carrier at the LAO/STO with different transport characteristics. One type of carriers are highly surface-confined having low mobility, whereas the other type of carriers has high mobility and lie deeper in the substrate. It is proposed that first type of carriers are associated with polar catastrophe mechanism, while the other type of carriers are associated with formation of oxygen vacancies at the LAO/STO interface.

2.5 Different models to explain the 2DEG

To understand the origin of the electrical conductivity and intriguing properties of 2DEG at LAO/STO interface different models have been proposed. In this section, these models will be explained.

2.5.1 Electronic reconstruction and polar catastrophe

Ohtomo et al. has proposed this model to explain the properties of 2DEG at LAO/STO interface [7]. As explained in Section (2.4), STO is composed of alternating $((SrO)^0$ and $(TiO_2)^0)$ charged neutral layers, whereas, LAO is composed of alternating $((LaO)^+$ and $(AlO_2)^-)$ charged layers. The conductive *n*-type interface is achieved by the deposition of LAO on TiO_2-terminated STO, which implies that the next layer is $((LaO)^+$. Similarly the insulating *p*-type interface is achieved by the deposition of LAO on SrO, which implies that the next layer is $(AlO_2)^-)$. In this way, stacking LAO on top of STO would create a so-called "polar discontinuity" [53].

It has been observed experimentally that there is a minimum thickness above which the interface is conducting [15, 54–56]. An electric field E and diverging electrostatic potential $\phi(z)$ arises from the net-charges of $((LaO)^+$ and $(AlO_2)^-)$ sub-layers that increase by increasing the thickness of LAO layer.

To avoid this unstable divergence, an electronic reconstruction can occur, that is the net transfer of half an electron per unit cell from the top surface, resulting in $Ti^{3.5+}$ at the reconstructed interface and consequently the potential no longer diverges. The mechanism of rearranging the electron distribution is illustrated in the Figure 2.3. Typically, one can construct the system from neutral atoms and then transfer half an electron from LAO layer to those above and below. In this way the total structure remains charge neutral.

This induced half an electron at the LaO/TiO_2 interface as shown in the Figure 2.3b, results in n-type conductivity. Due to electronic reconstruction the metallic behavior appears on the interface, which was observed experimentally. The interface with such stacking sequence is termed as n-type interface. Figure 2.3d shows the analogous construction for the AlO_2/SrO interface, here the charge neutrality is maintained by transferring half a hole per unit cell. In principle, here it should be p-type conductivity, however experimentally this interface was found to be insulating [7, 57].

This model provides good explanation of how the electronic reconstruction leads to n-type conductivity at the LAO/STO interface. However, it is difficult to explain with such simple model, why the p-type interface is insulating.

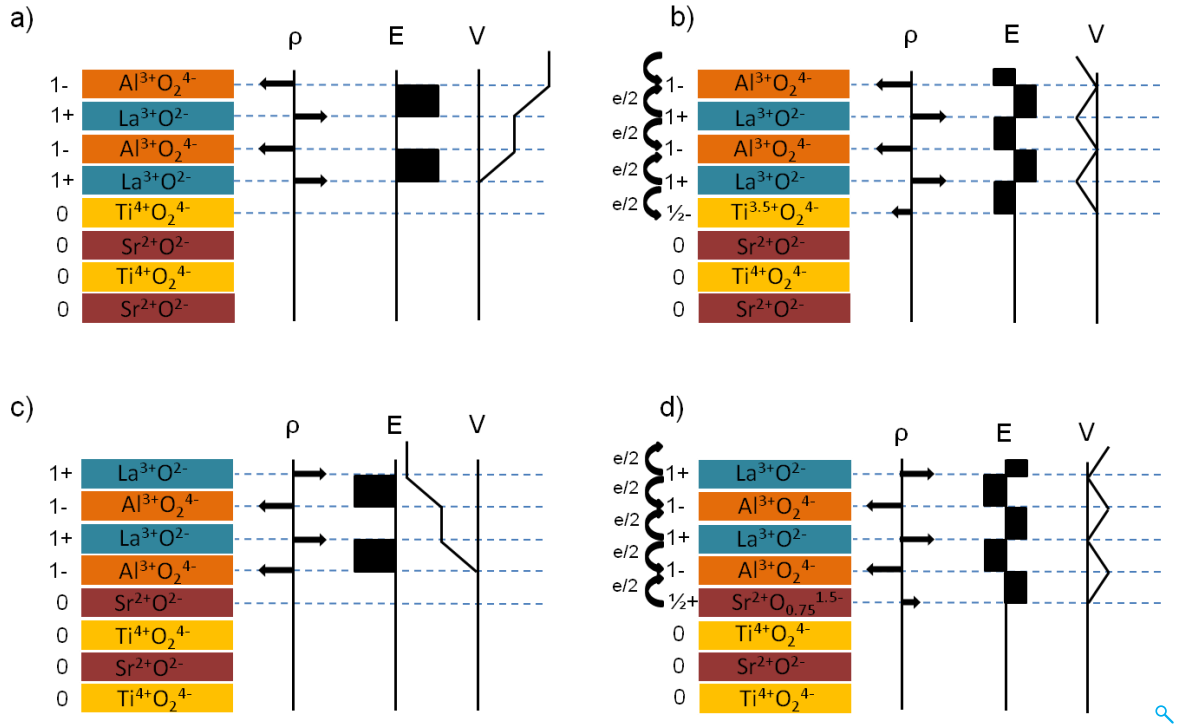

Figure 2.3: Illustration of the polar catastrophe occurring between $LaAlO_3$ and $SrTiO_3$. $SrTiO_3$ has neutral (001) planes, whereas $LaAlO_3$ has charged (001) planes. In the diagram ρ is the net charge of the layers, which leads to the electric field E, that produces the electrical potential V. (a) The n-type interface (TiO_2/LaO stacking) leads to a diverging potential V due to polar discontinuity. (b) If half an electron enters into the last TiO_2 plane the potential stay finite. (c) The potential of p-type interface (SrO/AlO_2 stacking) diverges negatively. (d) Removal of half an electron from the SrO plane in the form of oxygen vacancies can avoid this divergence [53].

2.5.2 Formation of oxygen vacancies

The polar catastrophe model can not explain completely the origin of conducting LAO/STO interface. There should be some other mechanism to explain the properties of 2DEG at LAO/STO interface. Oxygen vacancies are well known intrinsic electron donors in STO that can be deliberately produced by annealing in vacuum or in hydrogen atmosphere at high temperature [58]. High sheet carrier density and mobility values were discovered at the conductive LAO/STO interface. Oxygen vacancies in the bulk STO, which are created during the growth of LAO layers are one of the source of the conductive properties of LAO/STO interface [8, 59, 60]. Oxygen vacancies can be introduced by a conducting AFM tip at 3 uc insulating LAO/STO heterostructure sample. These vacancies contribute electrons to the STO conduction band, as a result conducting regions are created [16].

During the deposition of LAO by PLD, depending on the oxygen back ground pressure, a certain concentration of oxygen vacancies can be achieved, which renders the substrate conductive [8, 59–62]. These oxygen vacancies might be created in two different ways. Oxygen sputtering due to impacting species [63], because different species has different kinetic energy in the laser ablation flux, in the range from few eV up to hundreds of eV. Oxygen affinity of the material is considered other source of oxygen vacancies in the heterostructure. In case of LAO/STO heterostructure, LAO has higher oxygen affinity than STO, as a result STO-oxygen diffuse to LAO film [64]. Both mechanisms support the reduction of STO substrate, as a result it becomes semiconducting or even metallic.

The effect of oxygen pressure during growth on the transport properties of LAO/STO interface was intensively investigated by Brinkman et al [8]. For the sample deposited in the oxygen pressure lower than 10^{-3} mbar, transport properties are mainly governed by reduced substrate. This issue was avoided, either by depositing the LAO film in high oxygen pressure, or through post-deposition annealing to overcome these oxygen vacancies. The post annealing method might not remove all the defects in the structure, especially if the stoichiometry is not correct [65]. Even at high deposition pressure the presence of oxygen vacancies can not be excluded. In this case they are not dominating in the transport properties of LAO/STO interface.

2.5.3 Cation intermixing

Apart from electronic reconstruction, and the formation of defects during the deposition of LAO layer, the other possible mechanism to explain this 2DEG at the LAO/STO might be the chemical reconstruction, i.e. the creation of inter-diffused interface. In case of GaAs (polar in certain direction) grown on (non polar substrates) Si or Ge, such kind of intermixing has already been observed [66]. Liu et al. has also mentioned such kind of effect in $LaNiO_3/LaAlO_3$ superlattices [67].

The driving force for cation mixing is reduction of dipole energy at the interface. Metallic layer of $La_{1-x}Sr_xTiO_3$ is formed at the interface as a result of such intermixing, which could lead to interface conductivity. La is a well-know electron donor in STO, $La_{1-x}Sr_xTiO_3$ is conductive with wide range of x [68, 69]. Willmott et al. [70] has analyzed the LAO/STO structure by coherent Bragg rod analysis. Structural description showed that the LAO-STO interface is not abrupt, but consist of a graded intermixing over 3 unit cells. Moreover, they have noted that La-Sr mixing was evident some 6 Å deeper than that Al-Ti mixing because the ionic radii of La and Sr are twice as large as Al and Ti. Nakagawa et al. [53] using atomic-resolution electron energy loss spectroscopy (EELS), found that the n-type

interface is significantly rougher than the p-type interface. Chen et al. [71] has suggested in the theoretical work that La/Sr intermixing is favorable for the n-type interface, whereas for the p-type it is not, that could contribute to different conductive properties of these interfaces.

Despite extensive work, the origin of these interface properties are not completely understood, because there are more than one mechanism that may play a role in determining the interesting properties. Deposition and process parameters of the sample has great impact on the properties of the sample.

2.6 Summary

In this chapter, the crystal structure, electronic and magnetic properties of bulk LAO and STO were explored. Both LAO and STO are band insulators. At the interface of these two insulators, with a LaO/TiO_2 stacking 2DEG was formed, which has very intriguing properties. Because of these properties, the LAO/STO interface became a model system to study the fundamental physics of strongly correlated electronic systems, and also a candidate for future multifunctional oxide electronics. Different models including polar discontinuity at the interface, formation of oxygen vacancies in the STO substrate and La-Sr intermixing at the interface have been explained in detail, that offer the possible explanation of this conducting interface.

Chapter 3

Fabrication and characterization of the $LaAlO_3/SrTiO_3$ interface

In Chapter 2, bulk properties of the constituent materials and formation of LAO/STO interface along with intriguing properties have been discussed. In this chapter, the experimental methods employed for fabrication and characterization of the LAO/STO interface will be presented, including the deposition of the thin film by pulsed laser deposition (PLD), in-situ monitoring by RHEED, X-ray diffraction and Transmission electron microscopy (TEM). Finally the electronic transport measurement setup and the transport measurement results for unpatterned samples will be presented.

3.1 Sample preparation

The substrates and targets required some preparation before the deposition of high quality thin films. This section deals with the preparation (including cleaning, etching and thermal treatment) of substrates and targets before putting them into the deposition chamber.

3.1.1 Substrates and targets

The $SrTiO_3$ substrates used in this work were bought from CrysTech GmbH, Berlin (Germany). These as-supplied substrates are grown by Verneuil method having single side polished (001) oriented surface. The common size of the substrates used in this work is $10\times5\times0.5$ mm^3. The commercially available polished STO substrate has mixed termination. However, single TiO_2 termination can be achieved by treating the substrate using a well known recipe by Koster et al. [72]. The substrates are first cleaned with acetone and

then ethanol and isopropanol in ultrasonic bath for 10 min each, and at the end dried with nitrogen. In the second step, the substrates are put in DI water in ultrasonic bath for 30 min. The water hydrolyzes SrO unit cell planes which are dissolved by buffered hydrofluoric acid (BHF) by putting the sample for 30 sec in the acid. The terminated substrates are annealed in oxygen environment (with flow rate 150 L/h) at 950 °C for 2 hours to get straight terrace edges. This generates very clean, smooth and chemically well defined surface, suitable for layer by layer growth.

Prior to deposition, the stoichiometric $LaAlO_3$ single crystal target is polished with fine sandpaper, rinsed with acetone and isopropanol, and then dried with nitrogen. The target is mounted on a rotating multi-target holder, where five targets can be mounted and then transferred to the deposition chamber. As a final cleaning step before the actual film deposition, pre-ablation is performed for 2 minutes using the same parameters which are used later for film deposition, while keeping the shutter closed.

3.2 Pulsed laser deposition (PLD)

3.2.1 Principle and advantages of PLD

Pulsed laser deposition (PLD) is one of the most popular and advance technique to deposit epitaxial multi-component oxide thin films with very low defect density. The key advantages of PLD are that many materials can be ablated, growth rate is well controlled, relatively simple, and flexible technique for the deposition of high-quality films.

Using a laser to ablate the material for multicomponent system was under investigation as early as 1962 when Breech and Cross [73], used ruby laser to vaporize and excite atoms from the solid surface. Smith and Turner [74] used the similar laser to deposit thin film. The technique remained dormant for approximately the next twenty year until when in 1987 Dijkamp and Venkatesan [75] fabricated $YBa_2Cu_3O_7$ (YBCO), a high temperature superconductor thin film by pulsed laser deposition technique. Since then, pulsed laser deposition has been employed for the preparation of epitaxial thin film of a wide variety of materials including superconductors, metals, ferroelectrics, ferromagnetics and dielectrics.

In PLD, a high fluence pulsed photon beam is directed into a high-vacuum chamber and focused on the target material, resulting in ablation of material as shown in the Figure 3.1. The absorption depth of the photon at the surface depends on the wavelength of the laser beam. Gas excimer lasers are most widely used for the PLD which emit in the UV range like KrF (248 nm) and XeCl (308 nm). The wavelength between 200-400 nm restricts the penetration depth to the thin surface of the target material. This range is suitable in order

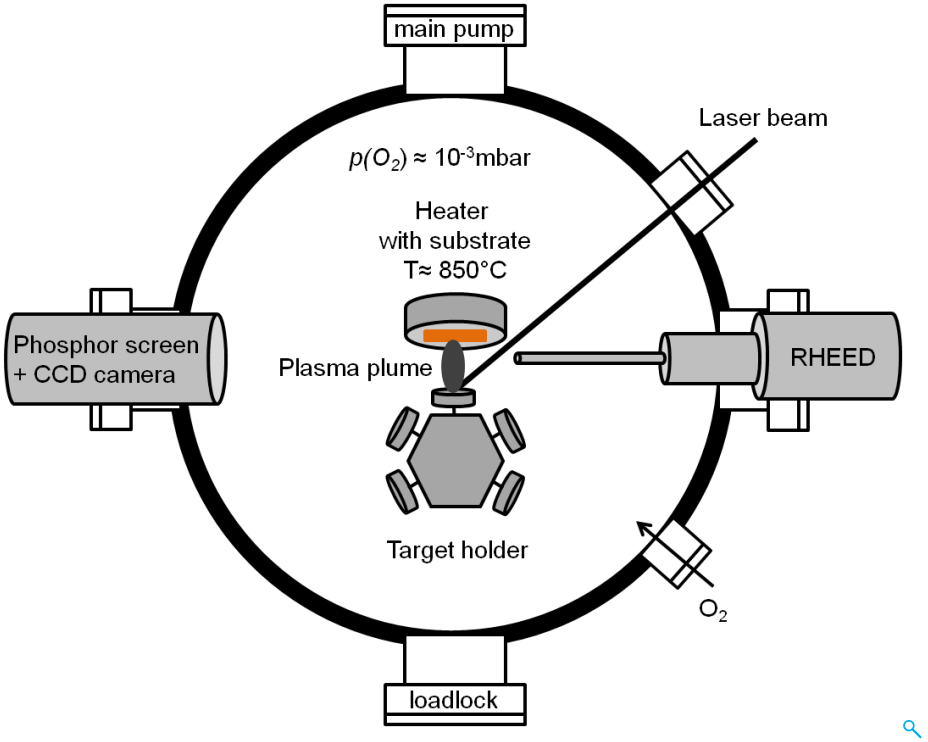

Figure 3.1: Schematic illustration of pulsed laser deposition (PLD) principle.

to avoid the boiling of the surface. The ablated material expands from the target surface due to high pressure and form the plasma plume, which is highly forward directed. During expansion, the internal thermal energy is converted into kinetic energy of the ablated particles. The heated substrate is positioned at the end of the plasma plume. The sufficiently high temperature of the substrate ensures the high film crystallinity. The ablated material is condensed on the substrate, involving the thin film nucleation and growth processes [76–79]. By adjusting the right deposition parameters, like energy density on the target, background gas pressure, substrate temperature, target-to-substrate distance and laser pulse frequency, a stoichiometric and high quality crystalline thin film are deposited by this technique.

3.2.2 Experimental procedure and parameters

In this work, thin film fabrication has been carried out in the system shown in Figure. 3.2 equipped with a KrF Excimer Laser (λ =248 nm). The homogeneous part of the laser beam profile is obtained by using an aperture. The deposition high vacuum chamber (base pressure $\approx 10^{-9}$ mbar) is connected to a load lock, so the substrates and targets can be mounted and exchanged without breaking the vacuum of the deposition chamber.

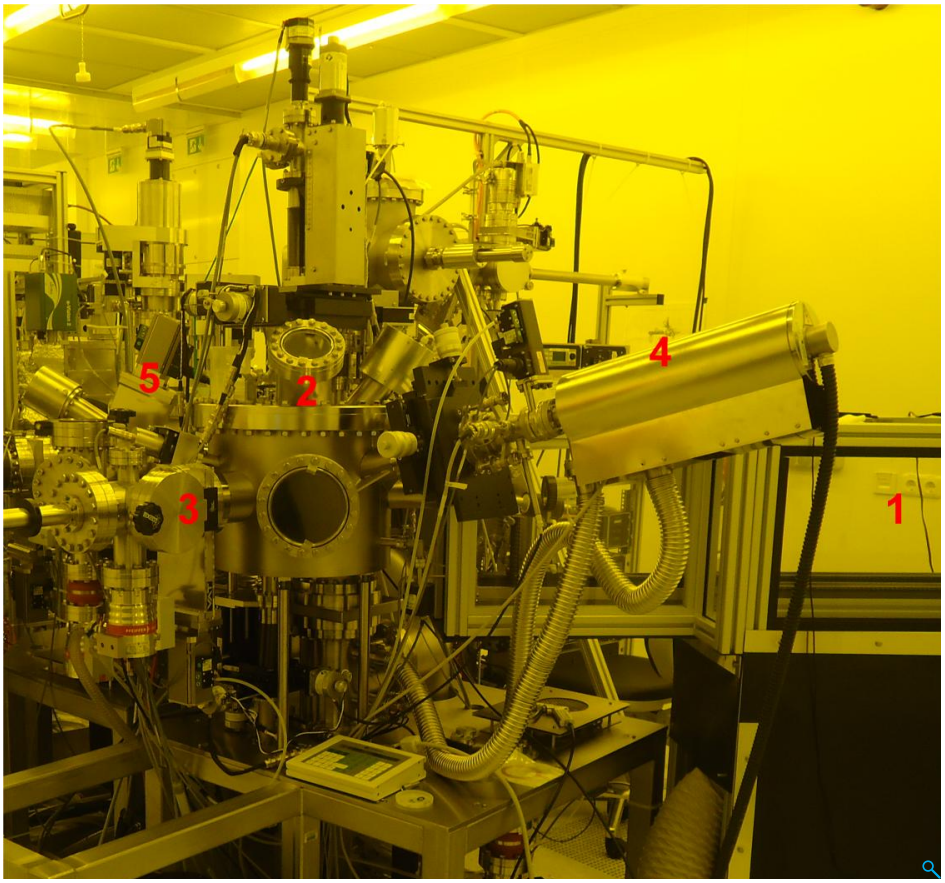

Figure 3.2: The PLD setup used in this work. **(1)** KrF Excimer Laser (λ =248 nm). **(2)** Main deposition chamber. **(3)** Loadlock. **(4)** RHEED system. **(5)** CCD camera.

The thin layers of LAO are grown from a single crystal LAO target on TiO_2-terminated STO (001) substrates. The substrate is glued to a heater by silver paint (for drying, put the heater on thermal plate having temperature 300 °C for 30 min) to assure good thermal contact. To monitor the layer thickness up to unit cell level in-situ reflection high-energy electron diffraction (RHEED) is used during the growth. After transferring the heater into the deposition chamber, the temperature is ramped up slowly up to 200 °C, then RHEED signals are aligned and then again ramped up to deposition temperature i.e 850 °C. Oxygen is used as a background gas, initially we have deposited samples at different pressure (i.e. 10^{-3} mbar and 10^{-5} mbar). X-ray diffraction(XRD) and transmission electron microscopy(TEM) measurements revealed that high quality films are obtained at a deposition pressure of 10^{-3} mbar. Later on we have used optimized parameter, 10^{-3} mbar during deposition. Laser fluence and pulse frequency are kept at 2 J/cm^2 and 2 Hz, respectively, during the deposition. The beam energy is controlled with a variable attenuator or with the laser voltage, yielding a

fluence at the target of 2 J/cm^2. The distance between the target and substrate is 4 cm during deposition. Before actual deposition, the target is pre-ablated for 2 min at 2 Hz to remove any possible surface contamination. After deposition, the samples are slowly cooled down to room temperature while the oxygen pressure is maintained.

3.2.3 Role of background oxygen pressure

In pulsed laser deposition, background gas is used for the following purposes; it is used as reactive species (e.g., molecular oxygen for oxides) to attenuate and thermalise the plume, and also to maintain balance between differently charged species in the plume. Interaction of ablated species with the background gas often produces molecular species in the ablation plume. These species facilitate multication phase formation. In addition to that, it is also used to characterize the kinetic energies and deposition rate of the ablated species [76, 80].

For the growth of oxides, it is necessary to have oxidizing environment to get the desired crystal phase. In case of LAO/STO interface, the background oxygen pressure has special importance because oxygen vacancies are considered one of the source of doping. Oxygen vacancies are formed in the bulk STO substrate during the growth of LAO films [60,81]. The role of oxygen vacancies is dominant in interface conductivity for the sample grown under low oxygen pressure.

Different research groups have used different values of oxygen partial pressure during the growth of LAO thin film and reported diverse values of carrier concentration and mobility at the interface. The sample grown at low PO_2 ($\leq 10^{-5}$ mbar) has carrier density $\approx 10^{17}$ cm^{-2} and mobility $\approx 10^4$ cm^{2}V^{-1}s^{-1} at low temperature. The large value of carrier density is attributed to oxygen vacancies. On the other hand, the sample grown at high PO_2 ($\geq 10^{-4}$ mbar) has reduced carrier density $\approx 10^{14}$ cm^{-2} as well as mobility $\approx 10^3$ cm^{2}V^{-1}s^{-1} at low temperature [7, 8, 15, 16, 82–84]. In this work, thin films (6 uc) are grown under oxygen pressure 10^{-3} mbar in order to limit the possible doping by oxygen vacancies.

3.3 Film growth

In the PLD technique, the laser pulse ablates the material from the target surface. The ablated material contain atoms, ions and molecules, that reach the substrate surface. Many individual processes such as adsorption, desorption, diffusion and nucleation occur and finally the particles are incorporated into the film. The schematic of the growth process is shown in the Figure 3.3. The structure of substrate, energy of the impinging atoms, deposition rate and surface mobility control the above mentioned processes.

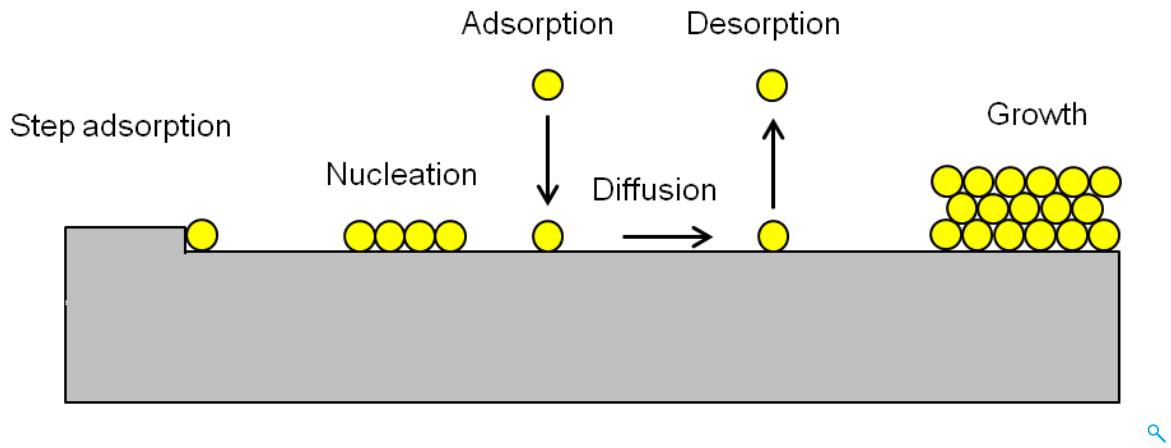

Figure 3.3: Schematic diagram of the processes during nucleation and growth.

In the beginning of the deposition process, the impinging particles are either elastically reflected or captured on the substrate by transferring their kinetic energy to the surface molecules. In the next step, small clusters or islands, distributed more or less homogeneously on the substrate surface are formed. These islands grow in size and merge together which is called the coalescence step. Coalescence continues until a connected network with unfilled channels is developed. With further deposition, these channels are filled in and leaving isolated voids behind. In the last step, these isolated voids are also filled in completely, as a result a continuous film is formed, as shown in the Figure 3.4 [85].

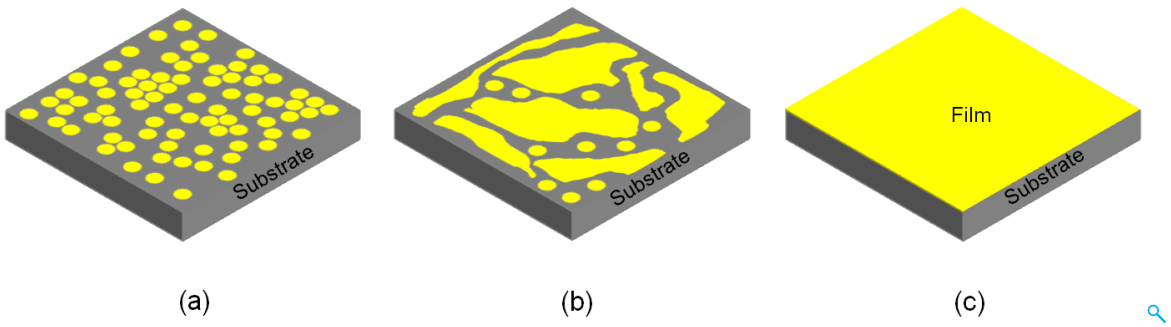

Figure 3.4: Schematic illustration of film formation. (a) Formation of small clusters or islands on the substrate. (b) Coalescence of small clusters. (c) Continuous film formation.

Depending on the free energy of the film surface, substrate surface and film-substrate interface, the growth modes can be classified into four types [86–89]. When the total free energy of the film surface and the interface is lower than the free energy of the substrate sur-

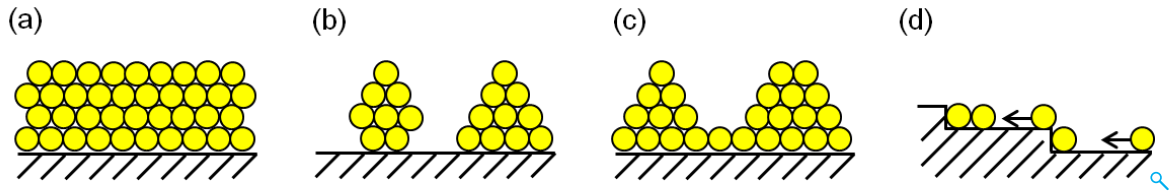

Figure 3.5: Schematic diagrams of different film growth modes. (a) Layer-by-layer or Frank-Van der Merwe mode. (b) Island or Volmer-Weber mode. (c) Layer plus island or Stranski-Krastanov mode. (d) Step-flow growth mode.

face, significant wetting will appear, as a result layer-by-layer growth occurs, which is also known as Frank-Van der Merwe (see Figure 3.5 a). This mode occurs during the deposition of semiconductor, and in complex oxide thin films. On the other hand, when the bonding between the film and substrate is weak, three dimensional islands are formed (see Figure 3.5 b). This growth mode is also known as Volmer-Weber growth. The Stranski-Krastanov growth mode is an intermediate mode between the island and layer growth mode. This growth mode occurs, when the film and substrate has lattice mismatch. The initial film growth is heavily strained due to lattice mismatch. The transition to island growth mode is favorable as a relaxation mechanism due to film-substrate lattice mismatch (see Figure 3.5 c). The fourth growth mode is known as step-flow growth (see Figure 3.5 d), where the film preserves step-terrace structures on the substrate. Atomic steps on the substrate, high temperature and high deposition rate are the main factors that are responsible for the step-flow growth.

3.4 Reflection high energy electron diffraction (RHEED)

Reflection high energy electron diffraction (RHEED) is a versatile technique, used to monitor the film growth in the deposition chamber with atomic level precision. The main advantages are that it is highly surface sensitive and compatible to use in-situ during the crystal growth. Electrons are diffracted by surface atoms and give the information about the periodic arrangement of the surface atoms [90–92]. Our PLD chamber is equipped with RHEED, and it is always used during the growth of LAO on STO substrate.

A typical RHEED measuring system consists of three components; an electron gun, a phosphor screen and an image-processing software and hardware [91]. Figure. 3.6 shows a schematic view of the RHEED geometry. A high energy electron beam (30 kV acceleration voltage) is incident on a sample at a grazing angle in the range of 0.5°–3°. The electrons are scattered from the sample surface, as a result a characteristic diffraction pattern is ob-

tained on the phosphor screen. Charge-coupled device (CCD) camera is used to analyze the RHEED pattern with necessary time resolution. Usually oxides are deposited in the PLD with high background oxygen pressure. To enable RHEED in such high pressure, a differential pumping unit and an extension tube is used [93]. The differential pumping unit allows to maintain a vacuum of better than 5×10^{-6} mbar in the electron source for safe operation and long lifetime of the cathode. An extension tube, which separates the electron source from the deposition chamber, is kept below 10^{-3} mbar. Using this two-stage pumping system, the pressure in the deposition chamber can be increased up to 0.5 mbar, while maintaining the vacuum of the electron source. The extension tube allows the electrons to enter the deposition chamber near the substrate. In his way, scattering loss of the electron is minimized.

In kinematical scattering theory, intensity maxima in the reflection are produced when the wave vectors of the incident and diffracted beam differ by a reciprocal lattice vector **G**.

$$\mathbf{k}_S - \mathbf{k}_0 = \mathbf{G} \tag{3.1}$$

Where $\mathbf{k}_S$ and $\mathbf{k}_0$ are the wave vectors of the diffracted and incident beam. A useful geometrical representation for this condition is provided by the Ewald sphere construction. The reciprocal lattice of a two-dimensional surface consists of infinitely thin rods, perpendicular to the surface. In this construction, the tip of the incident wave vector is attached to a reciprocal lattice rod, and the sphere is drawn around the origin of $\mathbf{k}_0$ with radius $|\mathbf{k}_0|$. Every intersection of the Ewald sphere to the reciprocal rod corresponds to one reflection. The wavelength of the energetic electron is very small ($\lambda \approx 7\text{x}10^{-12}$ m). The Ewald sphere has very large radius ($\approx$900 nm^{-1}) compared to the typical reciprocal lattice vectors ($\approx$16 nm^{-1}), as a result only few reflections lying on the circle are seen on the screen.

During the deposition of oxides, RHEED oscillation are observed in layer-by-layer growth mode, as shown in the Figure 3.6 (b). In the Figure 3.6 (b), the peak intensity of the (00) spot is plotted as a function of the time. In this mode, one layer is essentially completed before material is added to the following layer. The intensity of the specular spot changes during the growth of the crystal, that allows determination of the growth rate and accurately control the thickness up to mono-layer level. As depicted in the Figure 3.6 (b), the intensity fluctuations of the RHEED oscillation originate from the variation in surface morphology during 2D (layer-by-layer) growth [94–96].

In the beginning, the sudden drop of the intensity is most probably due to increase in roughness upon deposition of LAO, because initially we only have perfect surface. During the deposition, the intensity drops as the roughness increases due to the formation of small nucleation centers on the smooth substrate. The intensity increases again after the comple-

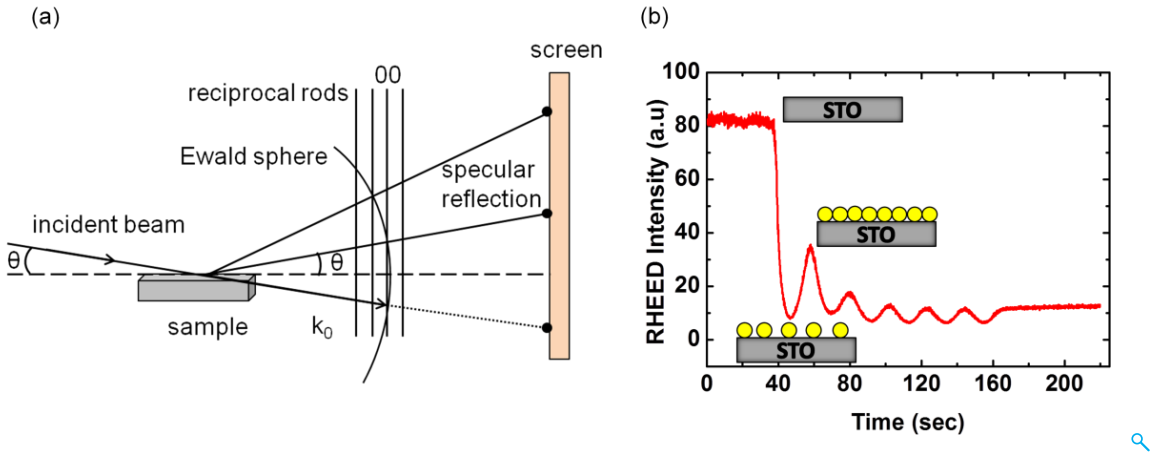

Figure 3.6: Schematic diagrams of RHEED geometry and RHEED oscillation. (a) Intensity maxima in the reflection occur in the direction defined by the intersections of the Ewald sphere with the reciprocal lattice rods. (b) RHEED oscillation during the growth of 6 uc of LAO on the TiO_2-terminated STO substrate and schematic presentation of film formation.

tion of mono-layer, because now the surface of the substrate become smooth again. Here the period of the oscillation corresponds to the growth of one mono-layer. The intensity decreases again upon formation of a new layer (rough surface). In this way, the thickness of the film is determined by counting the number of RHEED oscillations.

3.5 X-ray diffraction

X-ray diffraction (XRD) technique was used to determine the epitaxial relationship between the substrate and the film. In this work, high-resolution X-ray diffraction (HRXRD), Bruker D8 diffractometer equipped with a Cu X-ray tube, Göbel mirror, 4-bounce Ge (220) asymmetric monochromator and a Vantec-detector was used. With this configuration, the monochromatic Cu $K\alpha_1$ ($\lambda = 1.54054$ Å) x-rays were obtained.

Normally, θ-2θ scan is performed to observe the film as well as substrate reflections and to determine the lattice parameters of thin film and substrate. A detailed XRD analysis of an epitaxial film can be done by reciprocal space map (RSM). It is a data collection strategy in which a loop scan is performed. In the beginning, the specimen is set at a particular angle and then a 2θ scan is performed (in our case 2θ scan is performed by one dimensional (Vantec) detector). The specimen position is then incremented and another 2θ scan is performed. In this way, data is collected in 2-dimensional grid in reciprocal space. Figure 3.7, shows the basic features of RSMs of epitaxial thin films. Usually by reciprocal space map (RSM),

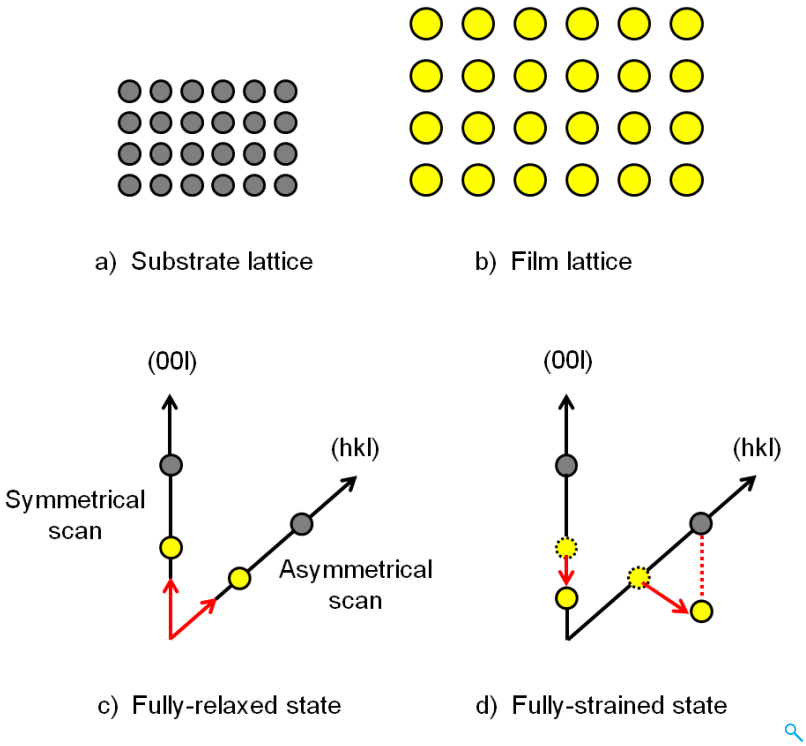

Figure 3.7: Basic features in reciprocal space map (RSM) for symmetrical and asymmetrical scan for epitaxial films [97].

the data is collected in a range around an asymmetric crystal reflection as shown in the Figure 3.7(c and d). Asymmetric reflection has a partial out-of-plane and in-plane direction component. For example, in case of (001) STO substrates, the area around the 103 or 113 reflection is usually studied. This method allows to check quickly (visually) whether the in-plane lattice parameter of a film is the same as that of the substrate. For asymmetric scan it is also possible to transform reciprocal space coordinate q_x, q_z into real space coordinate d_x, d_z [98, 99].

Figure 3.8 shows the reciprocal space map around asymmetric +103 Bragg reflections of different $LaAlO_3$ films grown on the $SrTiO_3$ substrate. It shows that all LAO films are fully strained, that is the in-plane lattice parameters are same as that of $SrTiO_3$ substrate (3.905 Å) whereas, the out-of-plane lattice parameters of films (3.75 Å) are smaller than the bulk values. Figure 3.8(a) shows the RSM for bare substrate, where we can only see the substrate peak. In Figure 3.8(b and c) film peaks are also visible. For 5 uc LAO layer the film peak is not pronounced, whereas, for 10 uc LAO layer it is more pronounced. The epitaxial growth of films is confirmed by RSM.

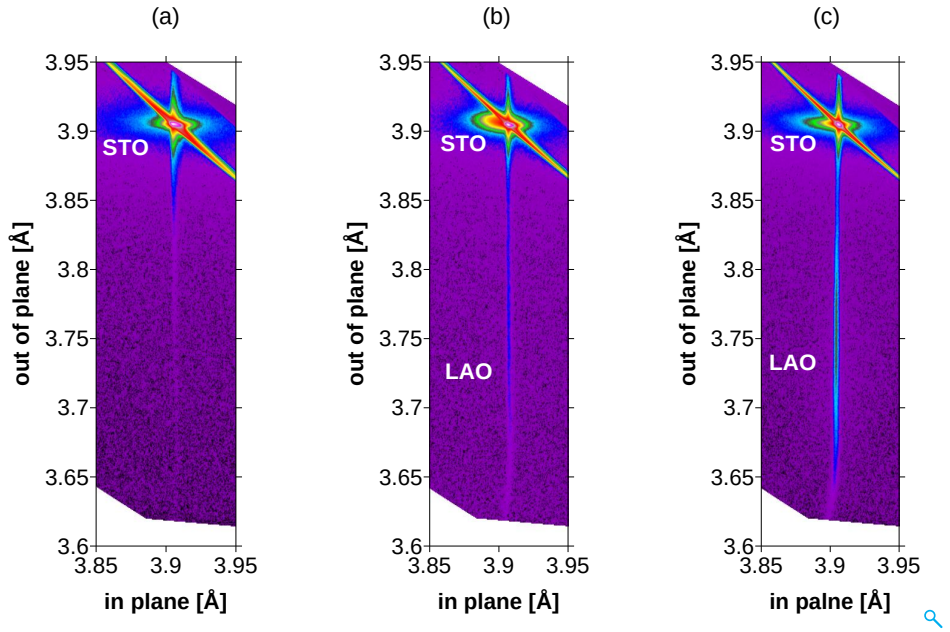

Figure 3.8: Reciprocal space map around asymmetric (103) Bragg reflection. (a) Bare STO substrate. (b) 5 uc of LAO on STO substrate. (c) 10 uc of LAO on STO substrate.

3.6 Transmission electron microscopy (TEM)

To gain more information about the crystal structure and stoichiometry of the LAO layer, especially when deposited at different deposition pressure, two samples were investigated by transmission electron microscopy (TEM) by Hakan Deniz and Dietrich Hesse at Max Planck Institute for Microstructure Physics Halle (Germany).

Two LAO thin films with different growth parameters were grown by pulsed laser deposition (PLD) on STO substrates. The sample labeled as MM9 was grown at the background oxygen pressure of 2×10^{-5} mbar, whereas the sample labeled as MM11 was grown at 1×10^{-3} mbar. Both samples were grown at the same substrate temperature (850 °C). To investigate the LAO thin films and the interface between LAO and STO, electron microscopy samples for cross-section view were prepared by conventional mechanical polishing procedures. Cross-section samples were observed using JEOL-4010 TEM at 400 kV for high-resolution imaging, and TITAN at 300 kV for S/TEM imaging and chemical analysis.

Figure 3.9 shows high-resolution TEM images of LAO/STO cross-section view from the sample MM9. Contrary to the expected growth of 5 unit cells of LAO, we observe two different thin films with different morphologies on the top of STO substrate. The underfocused image of Figure 3.9(a) shows the additional layer with lighter contrast on top of the LAO layer. The high-resolution image of Figure 3.9(b) has 4 unit cells of LAO film clearly

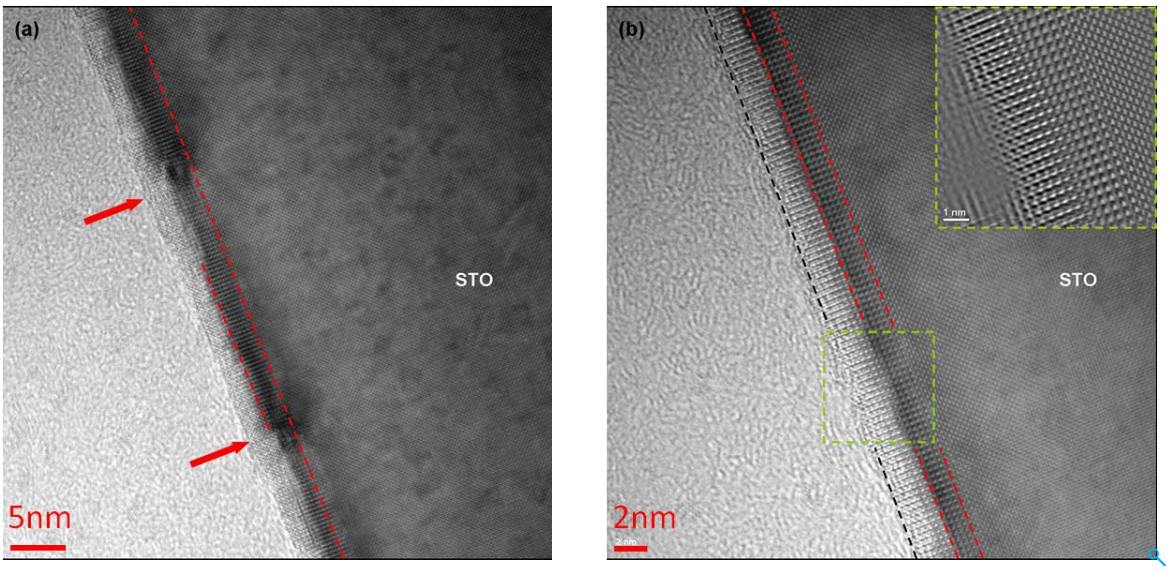

Figure 3.9: (a) Slightly under-focused TEM image of the LAO film on STO (MM9). Two dashed red lines outline the boundaries of the LAO film. An additional film is visible on top of the LAO film. Red arrows point to the defects that start at the interface between LAO and STO. (b) High-resolution image showing the secondary phase on top of the LAO film. The inset shows a filtered image from the region of interest colored in green.

visible, giving 3.85 Å for the in-plane lattice constant. The out-of-plane lattice constant of LAO varies between 3.80 Å and 3.90 Å, depending on the part of the images where the measurement is performed. There are occasional defects (as pointed at in Figure 3.9(a) by red arrows) originating at the LAO/STO interface that lead to a local tilt of lattice planes all through the grown film thickness.

Figure 3.10 shows HRTEM images for the sample MM11. In this case, there is no (or almost no) pronounced secondary phase observed on top of the LAO film, unlike the sample MM9. It also appears that the interface between LAO and STO is free from those defects seen in the MM9. The lattice constants for in-plane and out-of-plane directions are here 3.852 Å and 3.766 Å, respectively.

Sample MM9 was further investigated in the TITAN microscope using scanning TEM and energy dispersive X-ray (EDX) spectroscopy. Figure 3.11 shows a high-resolution STEM image together with X-ray intensities of Al-K and La-K lines obtained from the EDX line scan. Bright contrast in the STEM image corresponds to the pure LAO layer. The region which is marked between two violet colored lines is the unknown secondary phase that has rich Al content and poor La content compared to the LAO film. The high magnification high-angle annular dark field (HAADF) STEM image of Figure 3.12 shows the atomic structure

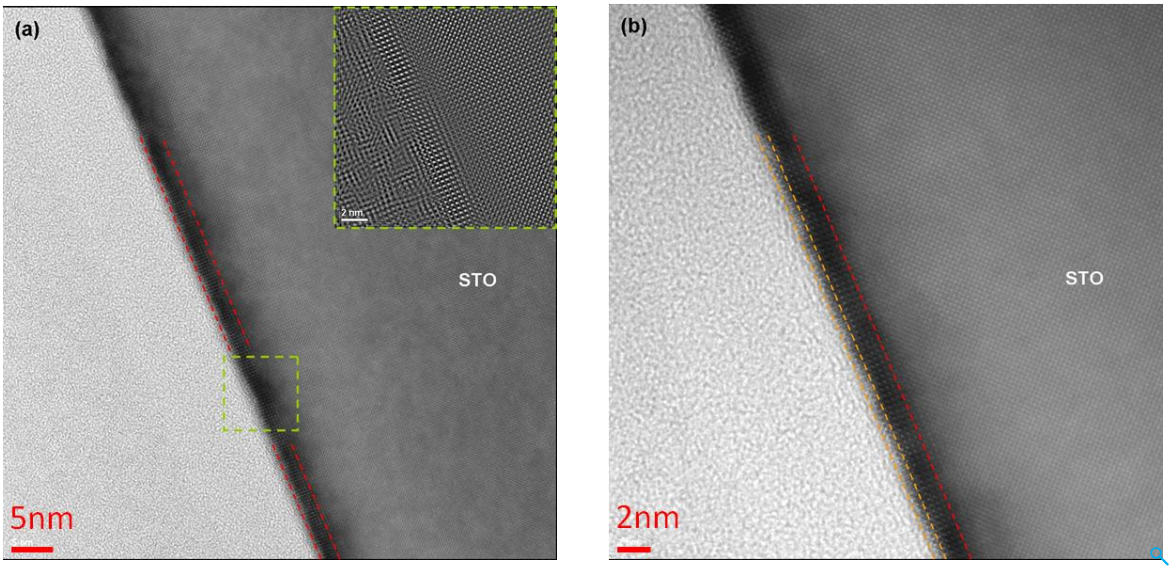

Figure 3.10: (a) High-resolution image of the LAO film from the sample MM11. Two dashed red lines outline the LAO film again. The inset shows a filtered image from the region of interest. (b) Another image of the same sample. Two orange lines indicate the boundaries of the secondary phase. In this case, it is less pronounced than in the previous sample.

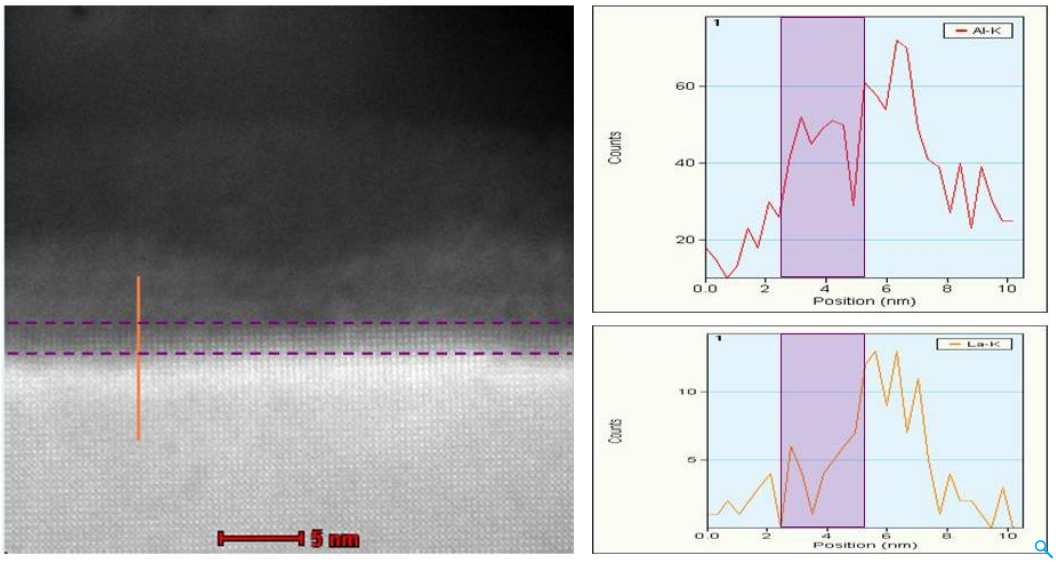

Figure 3.11: Scanning TEM image of MM9 (left). The bright layer corresponds to the pure LAO film. The vertical orange line in the image shows where the EDX line spectrum was acquired. On the right, Al-K and La-K X-ray intensities are shown as a function of position along the line from the left image (Spectrum started at the top of the line). Violet shaded areas in the X-ray line profiles correspond to the region of the film on top of the LAO film. They show that the secondary phase is rich in Aluminum content, but poor in Lanthanum.

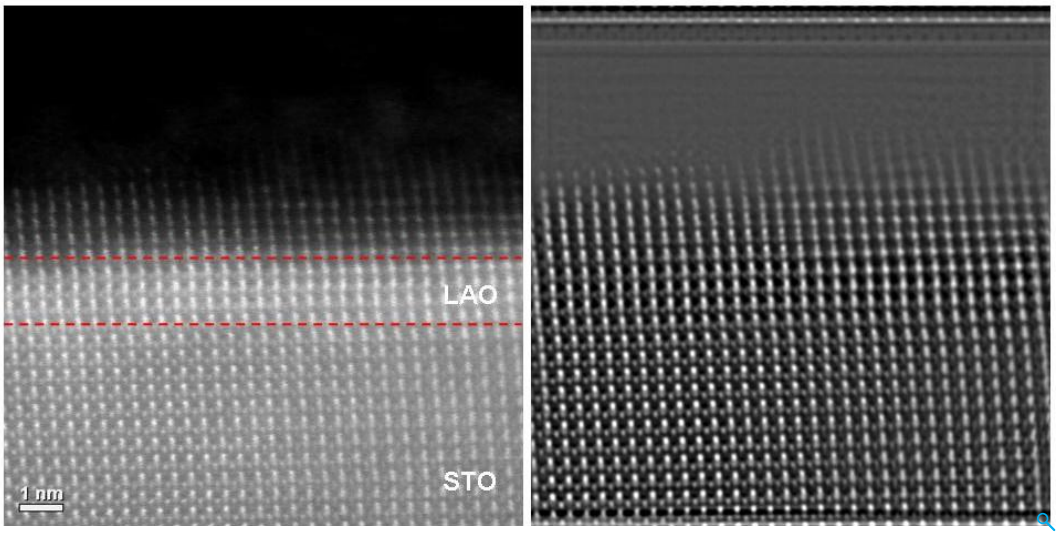

Figure 3.12: HAADF STEM image of LAO film from MM9 (left). The bright contrast in the image shows where the LAO layer is located (between the two red lines). The filtered image on the right shows the absence of La atoms in the unit cell in the secondary phase.

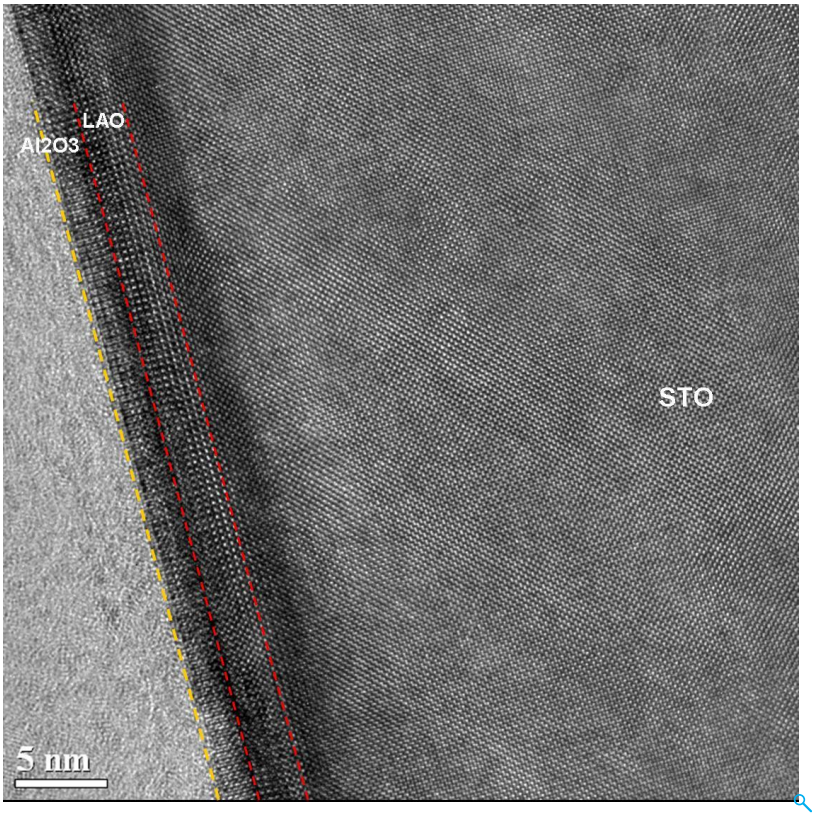

Figure 3.13: High-resolution TITAN TEM image of MM9 showing the LAO film on top of STO substrate and the Al-rich film (Al_2O_3) on top of the LAO film clearly.

of the LAO film and the STO substrate and confirms the epitaxial growth of the LAO film on top. However, the filtered image on the right shows that the intensity contribution of the atoms at the center of the unit cell (La atoms at the body center of the unit cell) decreases as we move from the bottom of the LAO film to the top of the secondary phase. This also confirms the results of the X-ray analysis. Figure 3.13 is another high-resolution image of the sample MM9 taken at the TITAN TEM, showing clearly two distinct films grown on top of STO. Crude Fast Fourier Transform (FFT) analysis indicates that the Al-rich phase has epitaxial growth mode with respect to the LAO film. The thickness of the Al-rich phase measured from the image is 2.018 nm approximately.

These measurements show that both samples MM9 and MM11 have epitaxial growth of LAO on the STO substrate. The sample MM9 has an additional secondary phase on top of LAO layer, which has rich Al content and poor La content (may be due to low background pressure the non-stoichiometric transfer of target material) compared to LAO layer. By considering these results, later all the LAO film used in this thesis were grown by using oxygen pressure of 1×10^{-3} mbar.

3.7 Electronic transport measurements

In this section, the experimental setup used for the measurement of electronic transport properties is presented. Besides the structural properties, electronic transport properties (like conductivity, electron density and mobility) also give the necessary information about the quality of thin film and its applicability in the future device. All the transport measurements are done in the Hall-bar geometry. The detailed procedure for patterning of the nano Hall-bars is explained in the Chapter 4.

After patterning the Hall-bars the samples are glued with low temperature varnish in the chip carrier as shown in the Figure 3.14(a), which are designed to fit into the various experimental setups in the labs. In the beginning, the preliminary characterization, including the I/V curve are done at room temperature at probe station. This characterization is done as a test to check the shorted devices. After this preliminary test, the gold pads of the chip carrier are connected to the Hall-bars via wire bonds. Aluminum wedge-bonding is used to bond the samples on the chip carrier. After bonding the sample, the electronic transport measurements are carried out in a ^{4}He bath cryostat in the temperature range of 4.2 – 300 K. Temperature dependent transport measurements are done during cool-down as well as during warm-up to identify the possible hysteresis.

Our electronic transport measurements setup comprises of Oxford cryostat, temperature

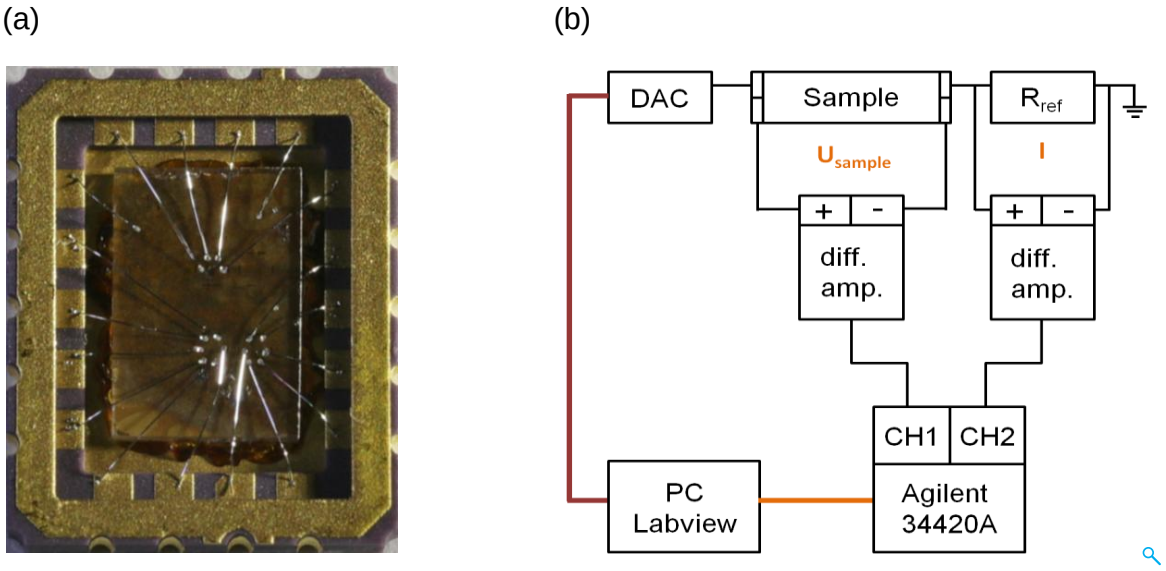

Figure 3.14: (a) Photo of sample mounted on a chip carrier and contacted by wire bonds. (b) Schematic diagram of the measurement circuit including peripheral components (PC, digital-analog-converter (DAC), Reference resistor (R_{ref}), differential amplifiers (diff. amp.), Agilent voltmeter). This configuration is used to measure the sample resistance in the Hall-bar geometry.

controller and nano-voltmeter (Agilent 34420A). Figure 3.14(b) shows the schematic measurement circuit diagram of temperature dependent transport measurement. The peripheral components like the computer is also included in the schematic, which is used to control the measurement setup by suitable program (Labview virtual instruments). The output bias voltage is provided by digital-analog-converters (DAC, self-built external equipment or input/output-controllers installed to the computer) that can be addressed by the program. As depicted on the left side in the Figure 3.14(b) the analog voltage is applied to the measurement circuit. As the fundamental component of transport studies is the determination of the sample resistance. This can be achieved by connecting a reference resistor R_{ref} in series to the sample, and grounded the other contact of the R_{ref}. Using differential amplifiers (diff. amp.) voltage drops across the sample and the R_{ref} can be measured. The voltage drop across R_{ref} is then used to calculate current (I) using Ohms Law. In this way, two voltages have to be measured. As mentioned above, a highly sensitive and precise two-channel-voltmeter (Agilent 34420A), which is capable of measuring voltages in the nV-range is used for this job. The out put channel of the voltmeter is connected to the measurement program as depicted in the Figure 3.14(b). The maximum bias voltage can be used in the range of ±10 V due to limits of the DAC (±2 V for the differential amplifiers).

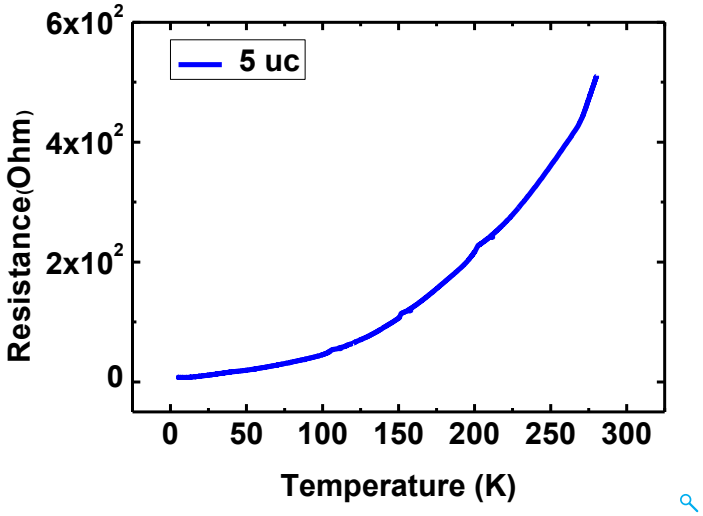

Figure 3.15: Temperature dependent resistance of 5 uc LAO/STO heterostructure.

At the start of this thesis, we have studied un-patterned LAO/STO interfaces, i.e. LAO film and also the electron gas extended over the complete sample area. We have grown different samples under same growth conditions, but by varying the film thickness. Some of the samples have thickness less than the critical thickness (i.e. 3 uc) and the others have thickness more than the critical thickness (i.e. 5 uc). For the electronic transport measurements, these un-patterned samples are contacted by using van-der-Pauw method. The electronic transport measurements are carried out in a ^{4}He bath cryostat.

Electronic transport measurements showed that for 5 uc sample the interface between TiO_2-terminated STO and LAO has conducting electron gas, whereas the 3 uc is found to be insulating. The R(T) curve of 5 uc sample is shown in the Figure 3.15. Conducting interface is observed with a typical drop in resistance of two order of magnitude from 280 K to 4.2 K. These measurements revealed that the electronic properties of the samples are in accordance with polar discontinuity model proposed by Ohtomo and Hwang in the very first publication about LAO/STO interface [7].

For unpatterned LAO/STO interface, it is not possible to do Hall measurements. However, during the course of this thesis we have developed a reliable and reproducible patterning technique (see Chapter 4), which is capable of patterning LAO/STO interface down to nanometer scale. With this technique we have patterned big Hall bars (having dimension in micrometer range) and also nano Hall bars (having dimension in 100 nm range) to study the transport properties of LAO/STO in detail.

3.8 Summary

In this chapter, the experimental techniques employed in this thesis for the preparation and characterization of LAO/STO heterostructures are explained.

A well known pulsed laser deposition (PLD) technique is used for the deposition of thin LAO layers on the TiO_2-terminated STO substrate. The thin films (6 uc) are grown at 850 °C under oxygen pressure 10^{-3} mbar in order to limit the possible doping by oxygen vacancies. The layer-by-layer growth of LAO is monitored by RHEED. The number of RHEED oscillations correspond to the number of LAO layers grown on the STO substrate. Reciprocal space map (RSM) around asymmetric +103 Bragg reflections is done to check the epitaxial relation between film and substrate. All LAO films are fully strained, the in plane lattice parameters are same as that of $SrTiO_3$ substrate (3.905 Å). Transmission electron microscopy (TEM) measurements revealed the effect of background oxygen pressure on the crystal structure and stoichiometry of the LAO layer, when deposited at different deposition pressures.

At the end, the electronic measurement setup is presented, which is used to study the conducting two dimensional electron gas (2DEG) at the interface of two insulators. The electronic setup comprises of Oxford cryostat, nano-voltmeter (Agilent 34420A) and temperature controller. In the beginning, the transport properties of the un-patterned LAO/STO interfaces having 3 uc and 5 uc LAO film was studied. The 5 uc sample was conducting whereas, 3 uc sample was found to be insulating. The results are in accordance to polar discontinuity model.

Chapter 4

Nanopatterning of $LaAlO_3/SrTiO_3$ interface

Silicon-based electronics have been the backbone of the industry for several decades [3]. The hallmark of semiconductors as technological materials is due to wide range tunable electrical conductivity, possibility of device scaling down to nanometer range and easy formation of insulating layers (SiO_2) for field-effect devices [16, 100]. Oxide materials incorporate many electronic properties of semiconductors [1], moreover, other interesting properties like interfacial superconductivity [13], strain-driven ferroelectricity [6], interfacial ferromagnetism [8] and colossal magnetoresistance [5] have also been reported in the oxide materials. These emergent phenomena made the oxide materials a promising candidate for future multifunctional oxide electronics [18, 19].

As explained in Chapter 2, the LAO/STO interface has a vast array of unique properties. A reliable and reproducible patterning technique is essential to use the material in nanopatterned quantum transport devices or employ it in state-of-the-art field effect based nanoelectronics. The technique should ideally be compatible to industrial processing and at the same time conserve the properties of the material independent from the lateral pattern size. The simple and straightforward way is to physically remove the LAO film by chemical or dry etching or by using a lift-off process. Common dry etching techniques like Ar ion milling are only of limited use for LAO/STO structures, because exposure to the ion beam creates a highly conducting layer on the $SrTiO_3$ substrate surface at room temperature as well as at cryogenic temperatures [101–103]. This highly conducting layer complicates any transport experiment in the patterned structures and makes device application virtually impossible.

Until now, different research groups have used different indirect patterning techniques to pattern the LAO/STO interface. The term indirect-pattering technique is used because no

physical patterning is done by using these techniques. No real physical nanopatterning of large area LAO/STO interface has been reported so far. These indirect patterning techniques are also not compatible with industrial process. Here, we have developed a direct and fully industrial compatible patterning technique to pattern the LAO/STO interface down to the nanometer scale [104]. In this chapter, all the steps followed to develop this direct-pattering technique will be explained in detail.

4.1 Indirect patterning techniques described in literature

In this section, all the patterning techniques which are reported in the literature so far will be described. In these techniques, either amorphous LAO [105] or AlO_x hard mask [17] or the conducting AFM tip [16, 106] was used to pattern the interface. In the following subsections, these techniques will be explained one by one.

4.1.1 Using amorphous LAO mask

The conducting quasi-two-dimensional electron gas generated at the LAO/STO interface has been patterned successfully by using particular thickness dependence of the interface conductivity, which sets in when the thickness of the LAO layer exceeds 4 unit cells (uc) only. By using this approach, the interface is patterned without exposing the edges of the conducting channels to the environment or chemicals [105].

In this technique, first 2 uc of epitaxial LAO were grown by pulsed laser deposition on a TiO_2 terminated (001) STO substrate. The films were deposited from stoichiometric, single crystalline targets in an oxygen atmosphere of 2×10^{-5} mbar at 770 °C and then cooled down to room temperature in 400 mbars of O_2 pressure. During the cooling process an additional annealing step was done for 1 h at 600 °C. Subsequently, UV-lithography was done and amorphous LAO was deposited at room temperature which was then patterned by lift off. Further deposition of LAO under suitable growth conditions led to a continuation of epitaxial growth limited to those places where the epitaxial LAO surface was still open while in places covered by amorphous material crystalline growth was inhibited as shown in the Figure 4.1. In this way, patterning of a q2-DEG in sub-micron resolution was achieved. The smallest conducting structures accomplished were ≈200 nm in width. Electrical measurements revealed that the patterned structures were conducting and the amorphous area between the structures was insulating. The sheet resistance of the unpatterned sample with 6 uc of LAO and the patterned sample with a width of 1.5 μm was comparable. However, the measured

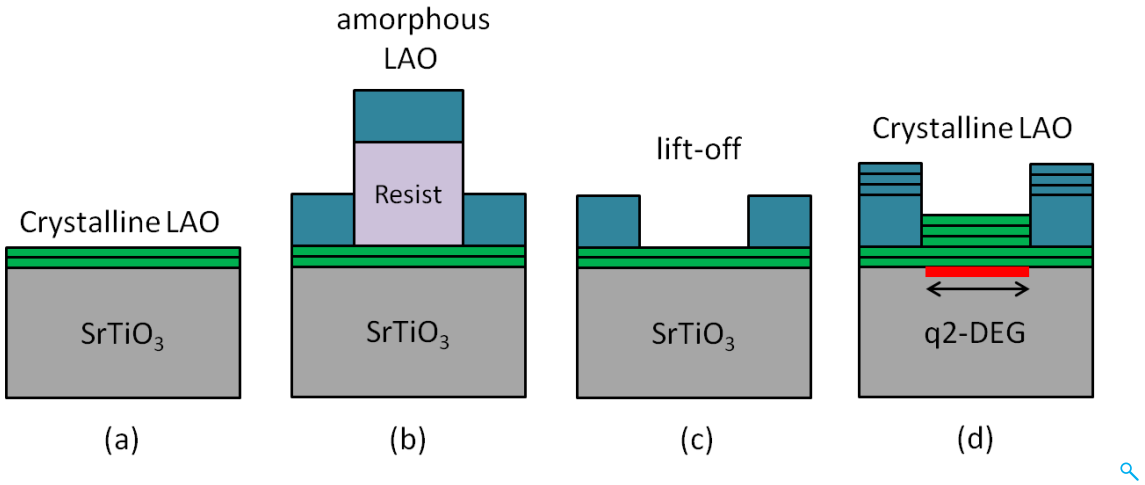

Figure 4.1: Illustration of the patterning procedure. (a) First 2 uc of crystalline LAO were deposited on TiO_2 terminated (001) STO substrate at high temperature. (b) UV-lithography was done and then 10 nm of amorphous LAO were grown at room temperature. (c) Lift off was done. (d) Again 3 uc of LAO were deposited at high temperature, 2DEG was formed where only crystalline growth took place.

small values of electron mobilities at 4.2 K, as well as at 300 K was attributed to the electron scattering at the edges of the patterned structures.

4.1.2 AlO_x based hard mask

In the hard mask approach, Banjerjee et al. [107] used an AlO_x based hard mask and epitaxial lift-off to pattern the LAO/STO interface. Temperature dependent magnetotransport studies have revealed the conservation of high-quality interface properties in the patterned structures.

The fabrication process has used the following steps: first $\approx$ 30 nm layer of amorphous aluminum oxide was deposited on TiO_2 terminated (001) STO substrate by PLD using a single crystalline AlO_x target. During the deposition, the oxygen pressure of 0.15 mbar was used and the substrate was held at room temperature. In the next step, the Hall-bar structures were patterned using UV-lithography, a developer solution (OPD 4262) was used to develop the sample, it also reacted with exposed aluminum oxide and formed the water-soluble alkali-metal aluminates. As a result, the STO substrate was covered with amorphous aluminum oxide with structured openings. The LAO film was deposited by PLD on these pre-patterned substrates at 800 °C in 10^{-3} mbar of O_2 pressure. The sample was cooled down in the deposition atmosphere without any annealing step. In the final step, the lift-off was done using 4M aqueous NaOH solution, as a result, well-defined and stable structures

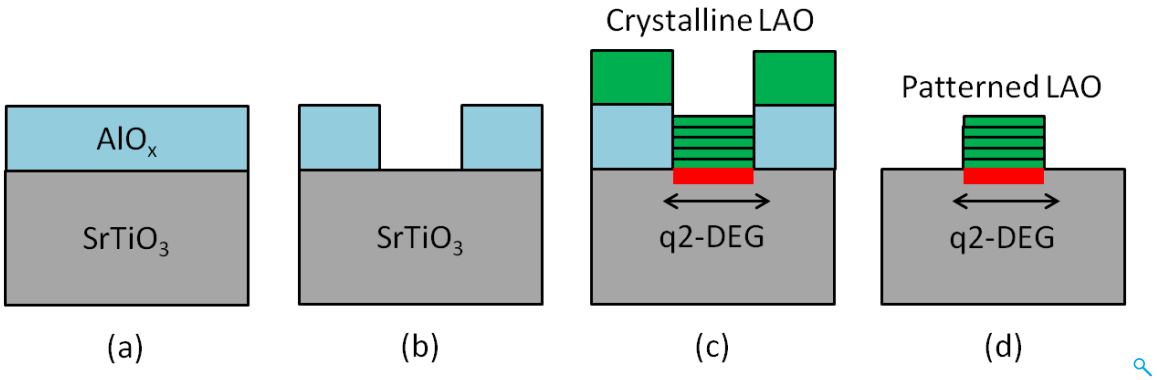

Figure 4.2: Cross sectional view of the sample during patterning. (a) First AlO_x was deposited on TiO_2 terminated (001) STO substrate at room temperature. (b) UV-lithography was done to pattern Hall-bars and then developed the sample. (c) Crystalline LAO was deposited on the pre-patterned sample by PLD. (d) Lift-off of AlO_x layer with LAO on top.

were achieved as shown in Figure 4.2. Transport properties of unpatterned LAO thin films and patterned Hall-bar structures have revealed very similar results for a 10 uc LAO layer.

4.1.3 AFM probe

Conducting Atomic Force Microscope (AFM) probe was used to create and erase conducting nanoscale structures at the LAO/STO interface. In this approach, the conduction was induced by AFM tip at 3 uc insulating LAO/STO heterostructure sample. The positively charged AFM tip introduced oxygen vacancies at the LAO surface, which contributed electrons to the STO conduction band. As a result, conducting regions were created [16].

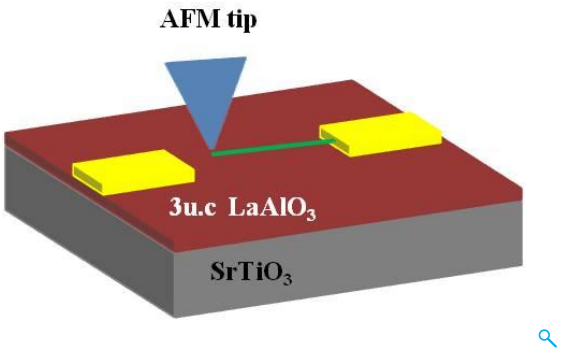

Figure 4.3: Schematic diagram to illustrate the experimental set-up for writing and erasing the conducting nano wire by AFM tip. A voltage-biased tip generated an electrical field that caused a metallic q2-DEG form locally at the route of the scanning tip.

To utilize this technique, first 3 uc of LAO were deposited on TiO_2 terminated (001) STO substrate by PLD. The substrate temperature was kept at 770 °C and the oxygen pressure at 6×10^{-5} mbar during the deposition. After deposition, the sample was cooled down in 400 mbar of O_2 with a 1h oxidation step at 600 °C. A positive biased (V_{tip} = +3 V) conducting AFM tip was used as a writing tool as shown in Figure 4.3. The AFM tip was scanned over the surface of the sample, starting from one conducting electrode to the other. Normally, the conductance between the electrodes was very low, but as the AFM tip reached the second electrode, a pronounced and abrupt increase was observed, that demonstrated the creation of a metallic wire between the electrodes with lateral size of $\delta x \approx 2$ nm. To check the reversibility of the process, the wire was cut with a reverse voltage (V_{tip} = -3 V) by scanning the AFM tip perpendicular over the wire. A sharp drop in conductance occurred when the tip crossed the wire.

Quantum size effect could be demonstrated by using these nanostructures, however, the disadvantage of this technique is that the structures are not stable over time at ambient conditions. Moreover, it is difficult to pattern large area devices or even integrated circuits by using this techniques.

4.1.4 Low energy Ar-ion beam irradiation

Recently, low energy Ar-ion beam irradiation was used to pattern the quasi-two-dimensional electron gas (q2DEG) at the LAO/STO interface with the combination of optical and electron beam lithography and subsequent ion beam irradiation [108].

Prior to the sample patterning, the LAO films (from 4 to 10 uc) were grown on TiO_2 terminated (001) STO substrate by PLD from a single crystal LAO target. During deposition, the substrate temperature was kept at 800 °C and oxygen pressure at 10^{-4} mbar. After deposition, the sample was annealed for 1 h at 600 °C and 500 mbar of pure oxygen. In the next step, the patterning of the LAO/STO interface was performed using photo and e-beam lithography and low-energy Ar-ion. The process relies on the fact that the decrease in interface conductivity under ion radiation due to lattice damage is faster than the increase of the substrate conductivity, leaving only a small process window for pattern fabrication. Therefore, by careful adjusting the irradiation dose, the interface can be made insulating and avoid unwanted electron doping due to oxygen vacancies. Lateral dimensions of 50 nm were achieved by using this patterning technique, and the structures exhibited good electrical transport properties down to low temperature and long stability. However, a notable unexplained increase in resistivity was observed for smaller structures.

4.1.5 Limitations of indirect patterning techniques

The above mentioned indirect nanopatterning techniques have some limitations. The techniques in which pre-patterned substrate surfaces and hard masks were used for the epitaxial growth of LAO could have residues of the hard mask material on the final devices, and also the surface was exposed to lithography and solvents before the deposition of the LAO thin film. The technique in which AFM tip was used for patterning has disadvantages, that the structures are not stable over time at ambient conditions and it is difficult to pattern large area devices or even integrated circuits by using this technique. For the low energy Ar-ion beam irradiation technique, an unexplained increase in resistivity was observed for smaller structures. All these may affect the electronic properties of the interface electron gas.

4.2 Direct nanopatterning of LAO/STO interface

No real physical nanopatterning of large area LAO/STO has been reported in literature so far. We have found that under certain conditions, chlorine-based reactive ion etching can be used to pattern LAO/STO interfaces while preserving the insulating properties of the substrate surface [104].

4.2.1 Deposition of LAO/STO interface

We use LAO layers (6 uc) grown by pulsed laser deposition (PLD) from a single crystal LAO target on TiO_2-terminated STO (001) substrates [72, 109]. Oxygen is used as a background gas at a pressure of 10^{-3} mbar during deposition. During deposition, the substrate temperature is 850 °C and Laser fluence and pulse frequency are kept at 2 J/cm^2 and 2 Hz, respectively. To monitor the layer thickness up to unit cell level, in-situ reflection high-energy electron diffraction (RHEED) is used during the growth [93]. After deposition, the samples are slowly cooled down to room temperature while the oxygen pressure is maintained.

4.2.2 E-beam lithography and Reactive ion etching (RIE)

“For the patterning, a thin film of novolack based image reversal resist is deposited by spin coating (see Figure 4.5, top). We have used AR-U4060 photoresist, which is capable of generating positive or negative tone images depending upon process parameters. For a negative process some optional steps have to be done including post baking and flood exposure. Here, we have used it for a negative process. This resist is also suitable for high resolution

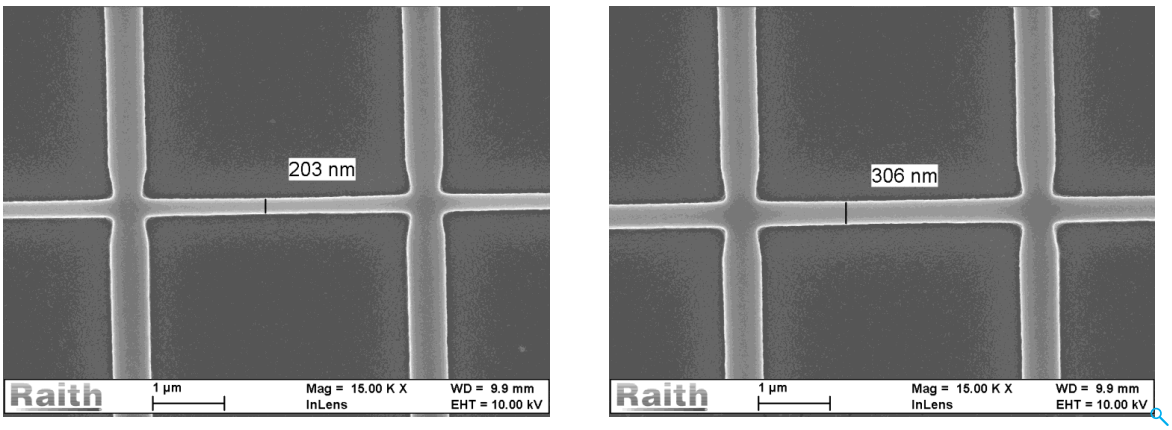

Figure 4.4: Scanning electron micrograph of part of (left) a 200 nm and (right) a 300 nm wide Hall bar with approx. 500 nm wide contact leads at the top and bottom.

optical lithography, allowing for direct transfer of the process to industrial lithography tools. Subsequently, the sample is exposed by electron beam (e-beam) lithography.

The exposed pattern consists of Hall bars with different respective nominal widths between 100 and 500 nm including large area bond pads. The sample is developed using photolithographic developer solution (AR-300-26, we have used the developer in dilution of 1:4). After development, reactive ion etching is performed in an inductively coupled plasma reactive ion etching system (ICP-RIE, Oxford Plasmalab 100) using a BCl_3-based etching process. The optimum results were obtained with a gas (BCl_3) flow of 30 sccm and a RF power of $230\,W$ while $1200\,W$ ICP was applied. The chamber pressure was held rather low (6 mTorr) to enlarge the mean free path length of the ions. Using these etching parameters, we obtained an etch rate of 13 ± 3 nm/min. We chose a process time of 19 sec for complete removal of the LAO layer. After etching, the resist is removed using N-Ethylpyrrolidone at 60 °C for 3 hours. The resulting patterned structures are stable at ambient conditions. The Hall bars are bonded using Al wire for electrical transport measurements. The bonds are placed directly on the LAO without additional metallization. Figure 4.4 shows a 200 nm and a 300 nm wide Hall bar, whereas Figure 4.5 (bottom) shows a 100 nm wide bar with approx. 500 nm wide contact leads. The line edge roughness achieved after etching is well below 10 nm" [104].

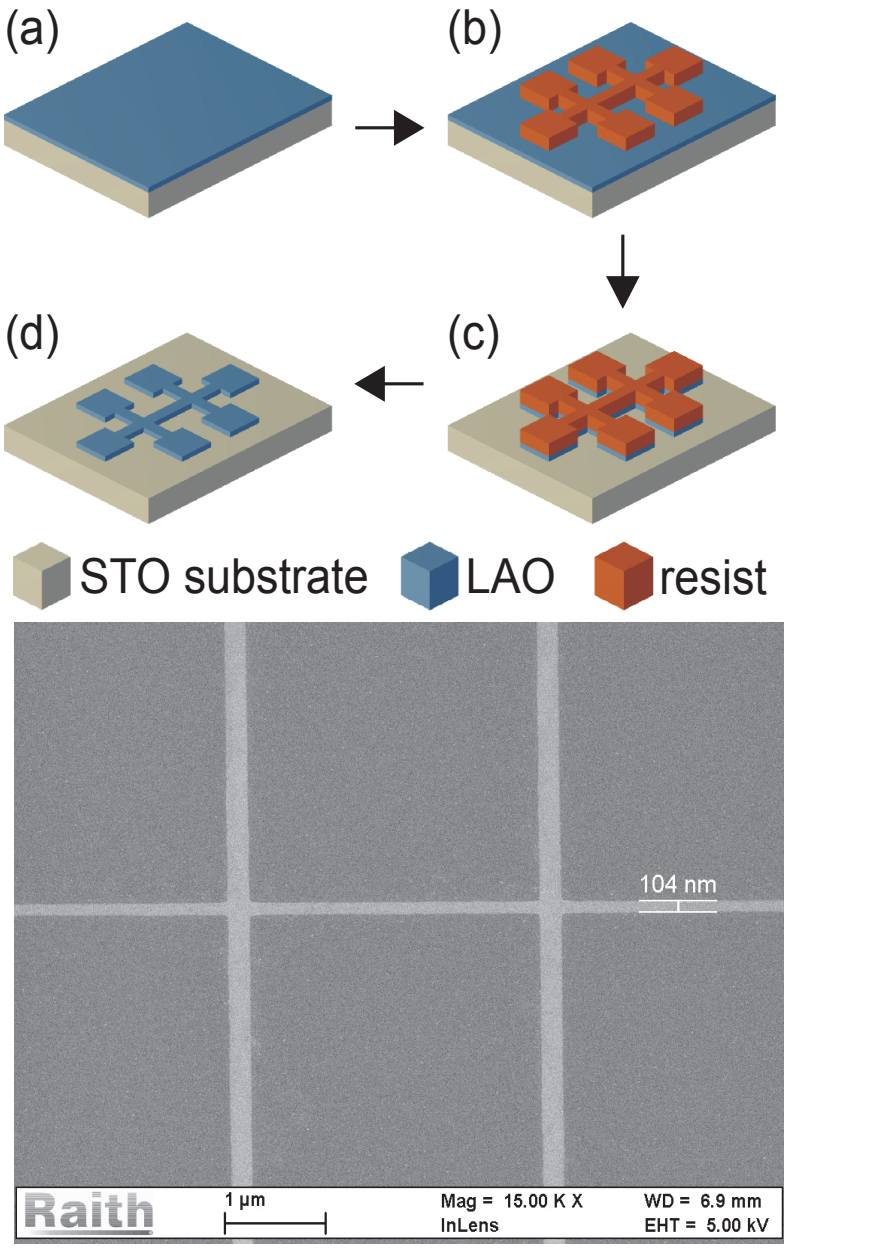

Figure 4.5: Top: Schematic diagram showing the process used to pattern the q2DEG down to the nanometer scale. (a) The LAO film is deposited on the TiO_2-terminated STO substrate. (b) Resist is deposited and patterned by e-beam lithography. (c) Dry etching is performed down to the STO substrate. (d) After removal of the resist, the patterned LAO structure remains on the STO. Bottom: Scanning electron micrograph of part of a 100 nm wide Hall bar with approx. 500 nm wide contact leads at the top and bottom. Published in Ref. [104]

4.3 Transport properties of nanopatterned LAO/STO interface

"Electrical transport measurements were carried out in a ^{4}He bath cryostat in the temperature range of 4.2 – 300 K. We are using DC measurements with a voltage drop over the sample of approximately $5-7\,mV$. The voltage drop over the sample and the reference resistor as well as the Hall voltage are measured using high impedance difference amplifiers and an Agilent 34420A nanovoltmeter. The area between the structures is insulating at room temperature as well as at low temperature. All fabricated Hall bars show metallic behavior down to 4.2 K (see Figure 4.6). The small increase in resistance at low temperature is not a special property of the nanosized Hall bars, but also often observed in large area transport structures [8, 107, 110, 111]. Figure 4.7 shows the resistance as a function of the Hall bars inverse nominal width at four different temperatures, ranging from room temperature to 4.2 K. Although plots show almost straight lines as expected for constant conductivity, there is a notable increase in sheet resistance with decreasing dimension of the structures.

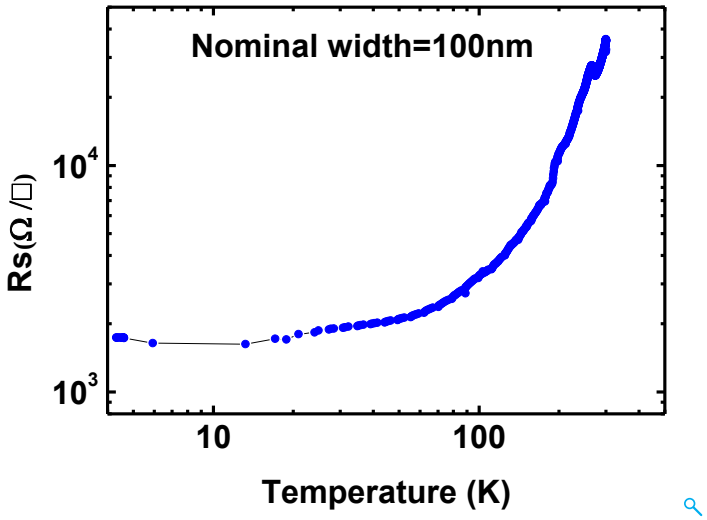

Figure 4.6: Temperature dependent sheet resistance of the q2DEG in Hall bar geometry with a nominal width of 100 nm. Published in Ref. [104]

This effect can be seen more precisely when the sheet resistance is plotted as a function of width (see Figure 4.9). For a perfect etching process, the sheet resistance should be constant and independent from the width of the Hall bars. In our results, however, comparing the temperature dependent resistivity for large area sample and micro Hall bars of different widths yields the following: The sheet resistance for large area samples is approximately

$12\,k\Omega/\square$ at room temperature, $7.5\,k\Omega/\square$ at 200 K, $1.5\,k\Omega/\square$ at 100 K and $0.25\,k\Omega/\square$ at 4.2 K. In the nanopatterned samples, we observed a slight increase in sheet resistance with decreasing width for all temperatures. However, this increase is much weaker than the one observed by Aurino et al. [108]. In order to understand the origin of the effect, we analyzed the dependence of the resistance on the width of the structures in more detail" [104].

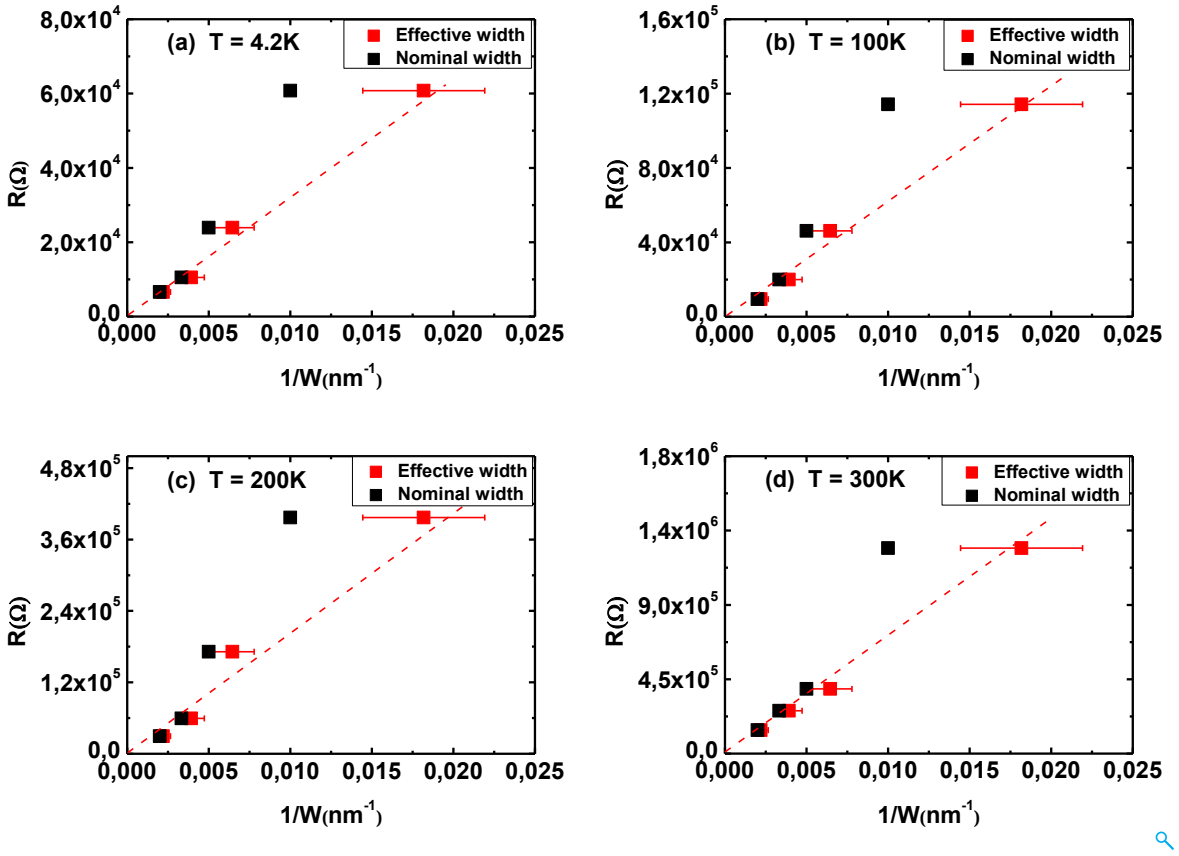

Figure 4.7: Resistance of the q2DEG in Hall bar geometry plotted as a function of the inverse effective (red) and nominal (black) width of the Hall bars. (a) Measured at 4.2 K, (b) measured at 100 K, (c) measured at 200 K, (d) measured at 300 K. Published in Ref. [104]

4.4 Sidewall depletion in nanostructures

An increase in resistivity throughout the whole nanopatterned samples does not fit the experimental results, but sidewall damage can explain the observations. Here the term "damage" is used in a broad aspect, which refers to any effect of the etching process that impairs the electrical properties of the material. Plasma etching-induced sidewall damage is already

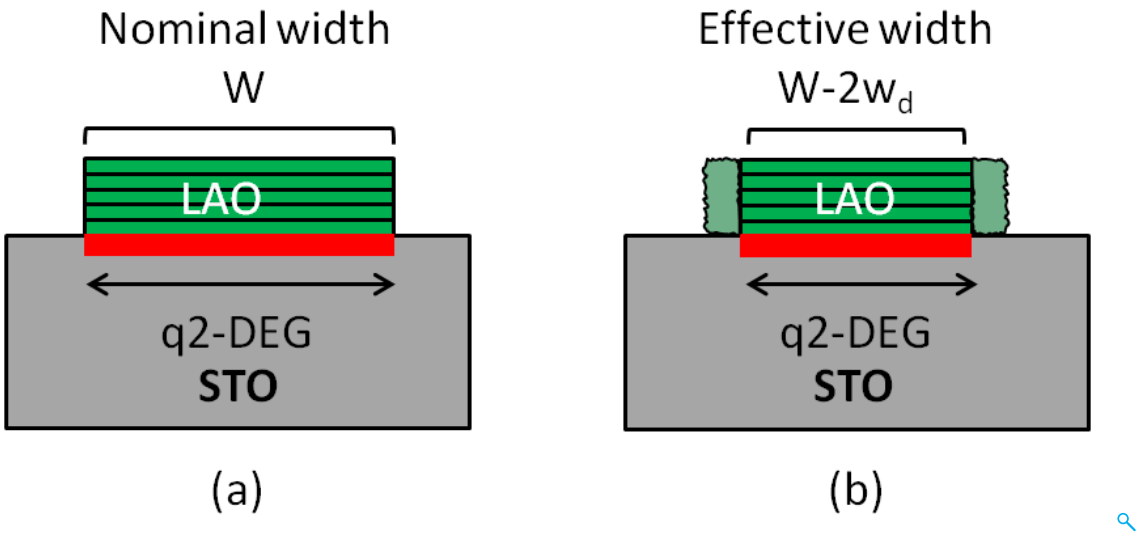

Figure 4.8: Illustration of the sidewall depletion. (a) Nominal width (W) of the structures, (b) Effective width of the structures (W-$2w_d$) is obtained by subtracting the depletion region (w_d).

reported in III-V (GaAs) and IV (Si/SiGe) semiconductor heterostructures [112–116]. Actually, during the plasma etching process, various species including electrons, positive and negative ions, neutral species, atoms and radicals etc. interact with sidewalls and cause damage. Sidewall damage depends on the ion bombardment energy and etching time. The higher the ion bombardment energy the larger the sidewall depletion width [114, 117]. During the plasma etching process the charges may be introduced and trapped on the sidewall surfaces that may also attribute to sidewall depletion width through electrostatic forces, and consequently affect the mobility of the device [118–120]. The sidewall depletion width can be derived from conductance measurement of etched wires with different widths [121]. Plasma etching-induced sidewall damage is subtle that leads to change in stoichiometry and creation of different traps and dislocation loops, consequently, one observes enhanced depletion, increased leakage and higher contact resistance [117].

"As described in the above paragraph, during the etching process, the sidewalls are exposed to the etchant and the material is damaged to a certain extent, mainly depending on the etching time. As etching time is constant for all structures, the depth of damage in the crystal is also identical for all Hall bars. This damage can result in a depletion region with constant width for all structures in which the conductivity is reduced. This reduction, however, should also depend on temperature.

For correct analysis, we have to divide the Hall bar along its width into two different

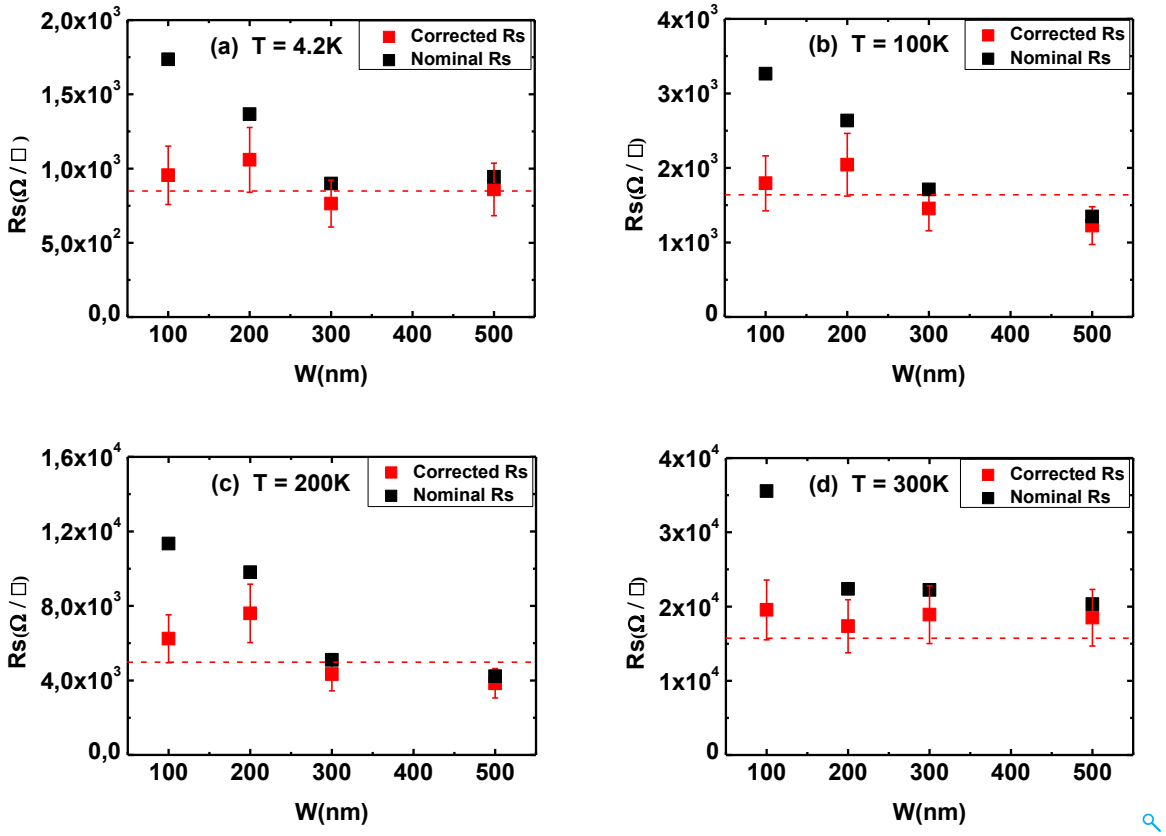

Figure 4.9: Sheet resistance of the q2DEG in Hall bar geometry plotted as a function of width. When the effective width is used, the sheet resistance is constant within the error bars. (a) Measured at 4.2 K, (b) measured at 100 K, (c) measured at 200 K, (d) measured at 300 K. Published in Ref. [104]

regions as shown in the Figure 4.8. A central region with an effective width (W-$2w_d$), where w_d is the depletion width, exhibits the sheet resistance of large area structures and a depletion region along the edges which has a higher but also temperature dependent resistance. It is however, a reasonable approximation to assume that the width of the depletion region does not depend on the temperature as it only depends on the presence of the defects.

The total resistance of the Hall bar can thus be calculated using the formula

$$\frac{1}{R_{total}} = \frac{W-2w_d}{\rho_1(T)L} + \frac{2w_d}{\rho_2(T)L} \tag{4.1}$$

where $\rho_1(T)$ and $\rho_2(T)$ are the sheet resistances for the Hall bar and the depletion region, respectively, W and L are the width and the length of the hall bar, respectively, and w_d is the depletion width. An adequate fitting procedure can be used to obtain the respective values for $\rho_1(T)$, $\rho_2(T)$ and w_d. It should be noted that $\rho_1(T)$ must correspond to the sheet resistance

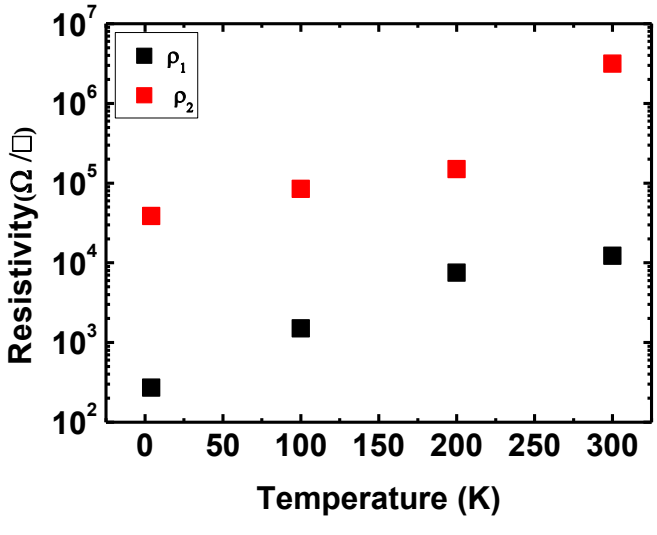

Figure 4.10: Resistivity ρ_1 of the center of the structure (black) and ρ_2 of the depletion region as function of temperature. Published in Ref. [104]

measured for large area structures. The fitting is performed for each temperature separately, nevertheless if the model is valid, the values obtained for w_d obtained must be identical for each temperature. Figure 4.10 shows the resistivity $\rho_1(T)$ of the center of the structure and $\rho_2(T)$ of the depletion region plotted over temperature.

The assumption of a temperature dependent $\rho_2(T)$ is based on the fact that defects introduced by the etching can result in traps whose occupation depends on the energy level and thus on the temperature. Based on this analysis we get a best fit for a sidewall depletion of approximately 20 ± 3 nm on each side of the structure for all temperatures evaluated. Figure 4.9 shows the sheet resistance plotted over the nominal width, once calculated using the nominal width and once calculated using the effective width. Obviously, the value which is obtained using the effective width is constant within the error bars of approximately 20% at all temperatures confirming the validity of our model" [104].

Hall measurements were used to calculate the carrier density (n_s) and carrier mobility (μ) in the nanostructure samples. The temperature dependent carrier density and carrier mobility are shown in the Figure 4.11 and 4.12 respectively. The carrier density (n_s) is calculated by using the relation $n_s = -1/R_H e$. Hall measurements show that at all temperatures the carrier density is in the range, $n_s \approx 10^{13}$ cm^{-2} for all structures, which is in good agreement with the literature values [15, 105, 122]. All samples exhibited thermally activated carriers. The carrier density increases fast up to 100 K, then it becomes approximately constant, as shown in the Figure 4.11.

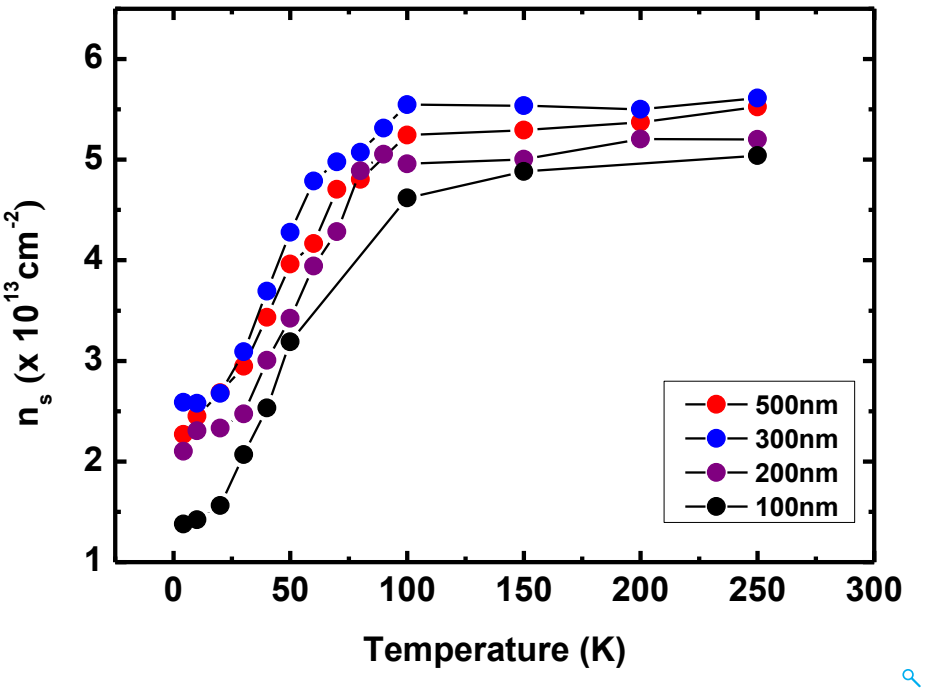

Figure 4.11: Temperature dependent carrier density n_s of the nano Hall bars.

Figure 4.12 (a) shows the carrier mobility calculated by using the nominal width of the structures. All the structures have shown same trend at all temperatures, except the 100 nm structure, which has low mobility at higher temperature. We have to recalculate the carrier mobility by considering the depletion region of the structures, because for smaller structures it has great impact on the carrier mobility. Figure 4.12 (b) shows the carrier mobility calculated by using the effective width of the structures with an error bars of approximately 20% at all temperatures. After the recalculation, we still do not have single value of mobility for all structures at the particular temperature. The highest values of mobilities are in the range of ≈ 500 cm^{2}V^{-1}s^{-1} and ≈ 5 cm^{2}V^{-1}s^{-1} at 4.2 K and 300 K, respectively. These values are smaller than the values reported in the literature at low temperature [7, 60, 122]. We may attribute these differences to the sidewall depletion. As the conductivity of the depletion region is lower than the central region, obviously it would effect the mobility of the structure. Other possible reason could be the electron scattering at the edges of the nanostructures.

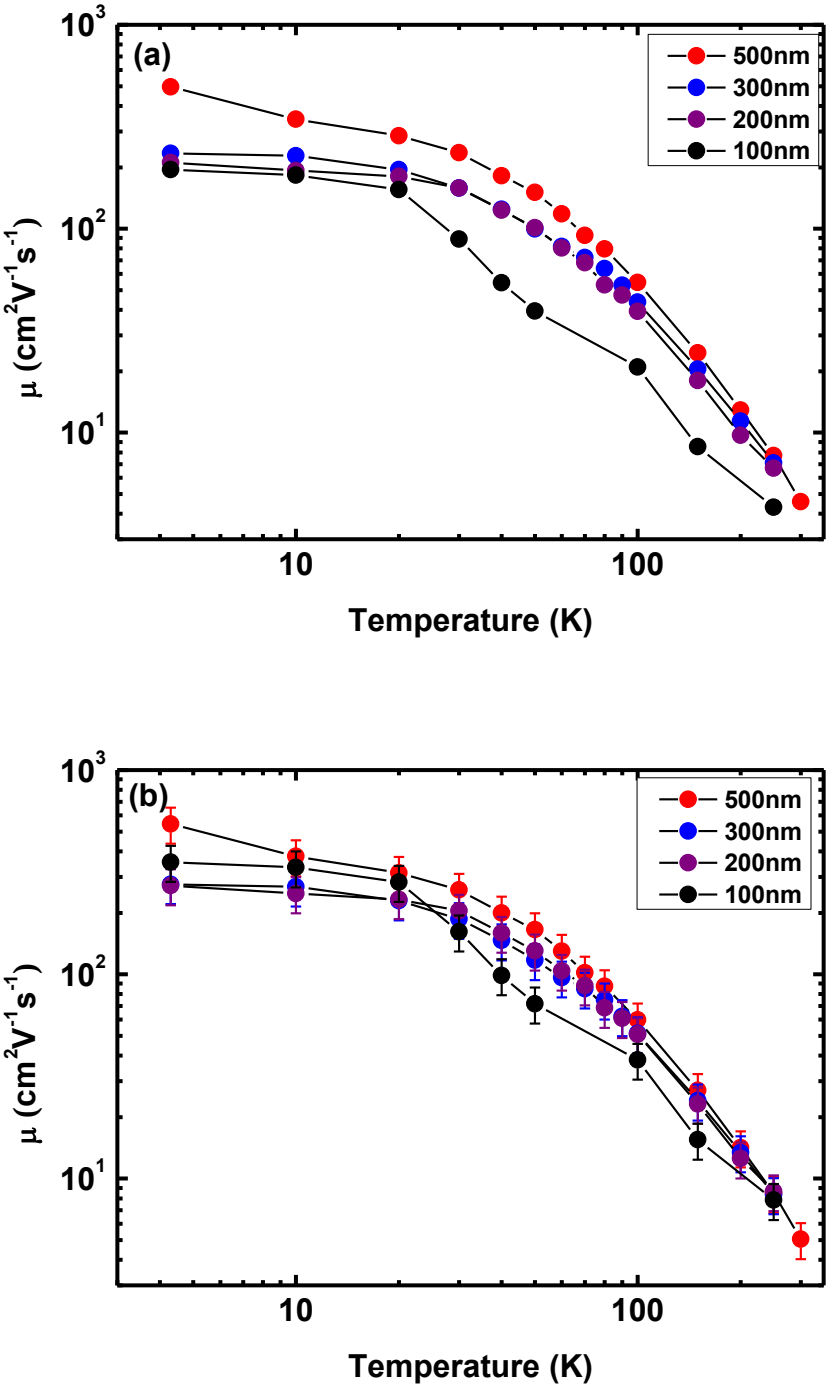

Figure 4.12: Temperature dependent carrier mobility μ of the nano Hall bars. (a) Calculated by using nominal width of the structures, (b) calculated by using effective width of the structures.

4.5 Nanopatterning by sequential deposition of LAO layers

We have also prepared nanostructures and large Hall bar (dimensions are in micometer range) samples by using the recipe of Schneider et al. with some modifications [105]. The detailed description of the patterning procedure and graphical illustration is given in Section 4.1.1. An epitaxial 2 uc LAO film is grown by PLD from a single crystal LAO target on TiO_2-terminated STO (001) substrates. The Oxygen pressure of 10^{-3} mbar, substrate temperature 850 °C, laser fluence and pulse frequency are kept at 2 J/cm^2 and 2 Hz, respectively, during the deposition. After deposition, the samples are slowly cooled down to room temperature while the oxygen pressure is maintained. Subsequently, negative e-beam lithography is done and 10 nm of amorphous LAO are deposited at room temperature. After the lift-off, epitaxial 4 uc LAO is deposited using the same parameter as mentioned above. The sample is then cooled down to room temperature in 1000 mbar of O_2. The cool-down includes a 1 h annealing step in oxygen at 600 °C. In this way, the LAO/STO interface is patterned, and all the structures are stable at ambient conditions.

After patterning the nanostructures, electrical measurements are carried out in a ^{4}He bath cryostat in the temperature range of 4.2 – 300 K as described in Section 4.3. The area between the structures is insulating at room temperature as well as at low temperature. All fabricated Hall bars show metallic behavior down to 4.2 K. Figure 4.13 (blue data points) shows the resistance as a function of the Hall bars inverse nominal width at four different temperatures, ranging from room temperature to 4.2 K. There should be linear relation between the resistance and inverse nominal width, but that is not the case. The effect can be seen more precisely when the sheet resistance is plotted as a function of width (see Figure 4.14 blue data points). In principle, the sheet resistance should be constant and independent from the width of the Hall bars.

We have also calculated the temperature dependence sheet resistance for larger area samples. For large area samples the sheet resistance is approximately $10 k\Omega/\square$ at room temperature, $4 k\Omega/\square$ at 200 K, $0.75 k\Omega/\square$ at 100 K and $0.10 k\Omega/\square$ at 4.2 K. In order to understand the origin of the fluctuation in sheet resistance in nanostructured samples, the dependence of the resistance on the width of the structures is analyzed in more detail. The samples are patterned by sequential deposition of LAO layer, so the defects may be introduced especially at the edges of the nanostructures or even in the whole sample during the lift-off process, which is done after the deposition of amorphous LAO layer. Due to these defects, the further epitaxial deposition of 4 uc LAO layer may not be homogeneous. As a result 2DEG is not formed homogeneously in the nanostructured samples, after the deposition of second crystalline LAO layer. The other possible reason could be the electron scattering at the edges of

the nanostructures. All these factors, may attribute to decrease in conductivity of the 2DEG in nanostructured samples. So we can say, that the lift-off process attributes to formation of depletion region at the edges of nanostructures and also to reduced homogeneity of 2DEG in whole structures.

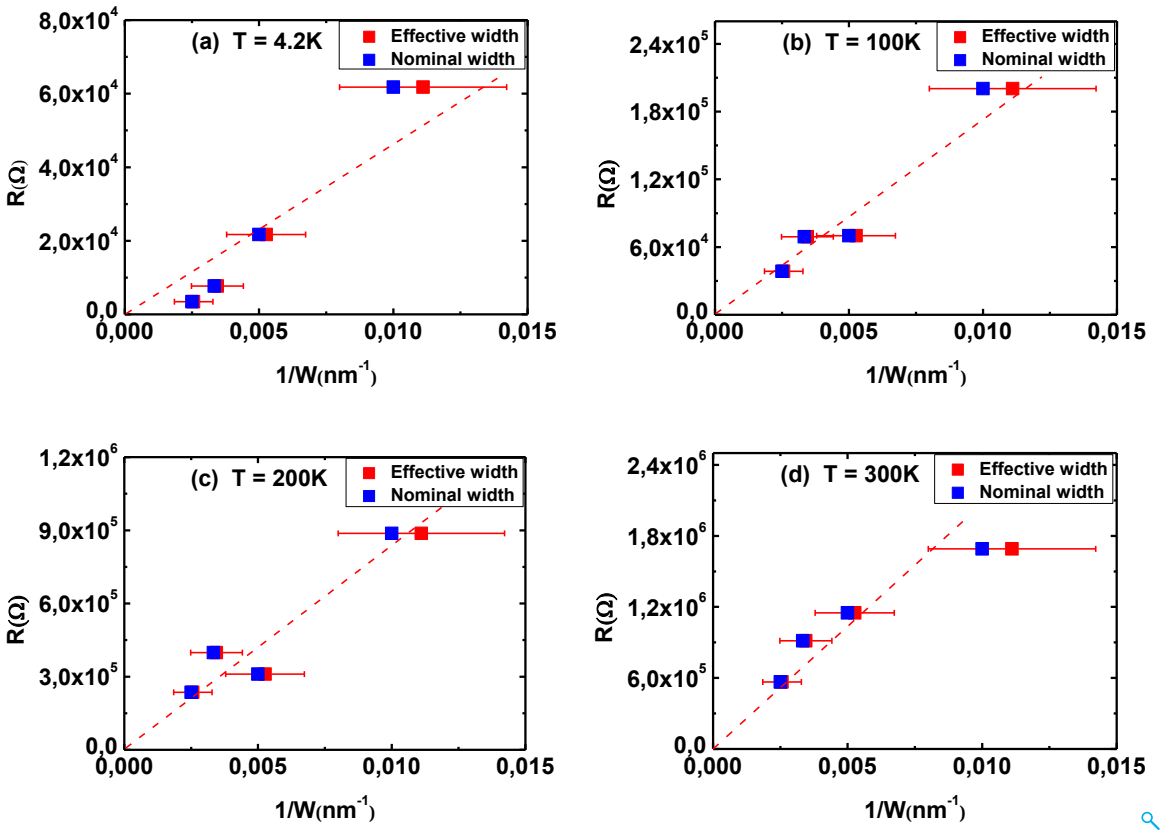

Figure 4.13: Resistance of the q2DEG in Hall bar geometry plotted as a function of the inverse effective (red) and nominal (blue) width of the Hall bars. (a) Measured at 4.2 K, (b) measured at 100 K, (c) measured at 200 K, (d) measured at 300 K.

We have applied the same model, which was previously applied for sample patterned by RIE method. We have divided the Hall bar along its width into two different regions as shown in the Figure 4.8. A central region with an effective width (W-$2w_d$), where w_d is the depletion width, exhibits the sheet resistance of large area structures and a depletion region along the edges which has a higher but also temperature dependent resistance. By using equation 4.1, the fitting is performed for each temperature separately, and constant value for w_d is obtained for each temperature. We get a best fit for the sidewall depletion of approximately 5 ± 0.5 nm on each side of the structure for all temperatures. By subtracting the depletion region, we obtained the effective width of the structures. We have plotted the

resistance as function of Hall bars inverse once nominal width (blue data points) and once effective width (red data points). For effective width within the error bars of approximately 28% we get approximately linear relation for all temperature except 4.2 K, as shown in Figure 4.13.

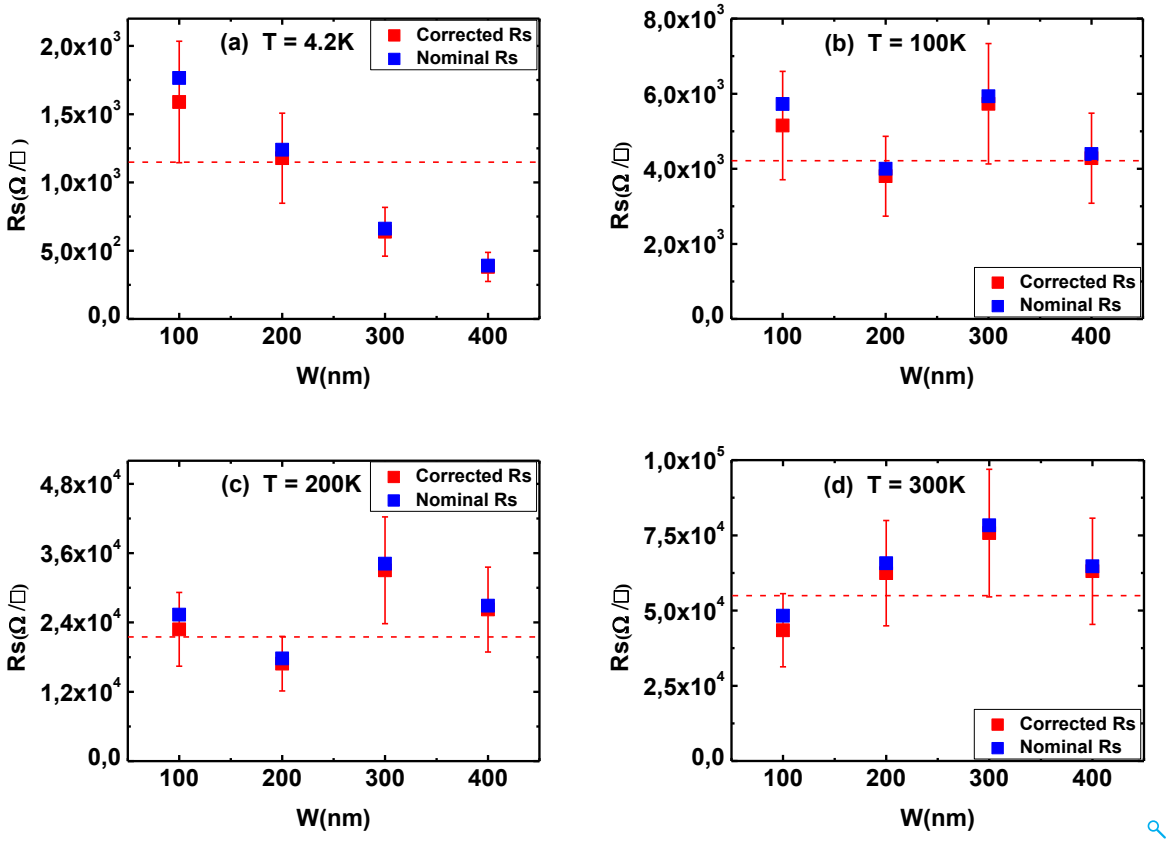

Figure 4.14: Sheet resistance of the q2DEG in Hall bar geometry plotted as a function of width. When the effective width is used, the sheet resistance is somewhat constant within the error bars. (a) Measured at 4.2 K, (b) measured at 100 K, (c) measured at 200 K, (d) measured at 300 K.

Figure 4.14 shows the sheet resistance plotted over the nominal width once calculated using the nominal width (blue data points) and once calculated using the effective width (red data points). Our model fits well for all temperatures except 4.2 K. At 4.2 K there is more variation in sheet resistance with respect to lateral size of the structure. For 100 nm structure, the sheet resistance is approximately 4 times larger than 400 nm structure. But at higher temperature the value which is obtained using the effective width is approximately constant within the error bars of approximately 28% at all temperatures as shown in the Figure 4.14.

4.5.1 Comparison of both patterning processes

Now, we can compare the sample patterned by E-beam lithography plus reactive ion etching (RIE) method and by sequential deposition of LAO layers method. Both processes allow to pattern the LAO/STO down to 100 nm or even below this lateral size of the structures by optimizing the process conditions. The width of the depletion region for the sample patterned by RIE method is in the range of 20 ± 3 nm at all temperatures, whereas it is 5 ± 0.5 nm for the sample patterned by sequential deposition of LAO layers. The sheet resistance of the sample patterned by sequential deposition method at all temperature is higher than the sheet resistance of the sample patterned by RIE method (see Figures 4.9 and 4.14). We can conclude that the nanopatterning of LAO/STO interface is more reliable by RIE method. The process conserves the electronic properties of the interface and is industry compatible.

4.6 Summary

In this chapter, the indirect-patterning techniques of the LAO and STO interface, which are reported in the literature are described. The drawbacks or limitations of these techniques are, when pre-patterned substrates or hard masks were used could have residual of hard mask material on the final devices, and also the surface was exposed to lithography and solvents before the deposition of LAO thin film. When AFM tip was used for patterning, the structures were not stable over time at ambient conditions and it was difficult to pattern large area devices or even integrated circuits.

In the second part of the chapter, the newly developed patterning technique is presented. This direct-patterning technique uses e-beam lithography in combination with dry etching to successfully pattern the LAO/STO heterostructures down to 100 nm. The process leaves the substrate insulating and preserves the conductivity of the electron gas except for a narrow depletion region. The width of the depletion region is approximately 20 ± 3 nm, which is constant, however, its conductivity is temperature dependent, which is in good agreement with traps introduced by the etching process. The process allows us to access device dimensions well below 100 nm and is fully industry compatible. It is expected that more detailed optimization of the process conditions can even further reduce the already small damage.

In the last part of the chapter, transport properties of the nanostructure samples patterned by sequential deposition of LAO layers is presented. By employing this method, we are also able to pattern the LAO/STO down to 100 nm. The area between the structure is completely insulating. The structuring process introduced the defects at the edges of the nanostructures, which may attribute to formation of depletion region with constant width with reduced con-

ductivity. The width of the depletion region is approximately 5 ± 0.5 nm at all temperature. The model fits well at all temperature except at 4.2 K.

The sheet resistance of all the samples at all temperatures patterned by the sequential deposition of LAO layers method is higher than those in RIE method. Patterning of LAO/STO by RIE is more reliable and also fully industry compatible.

Chapter 5

Tetragonal domains in $LaAlO_3/SrTiO_3$ interface

Since last decade, the LAO/STO interface has been intensively studied because of its intriguing properties. Initially, the main focus was to explore the electrical and magnetic properties of the conducting interface [7, 8, 13–15, 51, 52, 123], and not much attention was given to consider the influence of structural changes of the STO substrate on the interface properties. The main difficulty was that the standard surface science probes, such as scanning tunneling microscopy (STM) were inadequate to study the buried oxide interfaces. Nanoscale probes made it possible to explore the microscopic physics at the interface. Scanning nanoscale probes are used to map the spatial distribution of charge carriers at the LAO/STO interface [83], to explore the significance of microscopic structural domains on the transport properties of the interface [124, 125], and to realize the unique nanoscale devices at the interface [126, 127]. After exploring the material properties of the LAO/STO interface, the efforts are now devoted to fabricate the oxide devices. Hence, it is essential to understand the functionalities and boundaries of such devices. The main focus of this chapter is to study the effect of phase transitions of the STO substrate on the transport properties of 2DEG at LAO/STO interface, especially when the interface is patterned in nano Hall bar structures.

5.1 Tetragonal domains formation in $SrTiO_3$

At room temperature, STO has a cubic crystal structure with a titanium atom at the center and oxygen atoms in each of the six cube walls forming a cage around a titanium atom, and strontium atoms at the corners of the cube. At low temperature, T=105 K the oxygen octahedra rotate as a result cubic symmetry is broken and unit cell becomes a rectangular

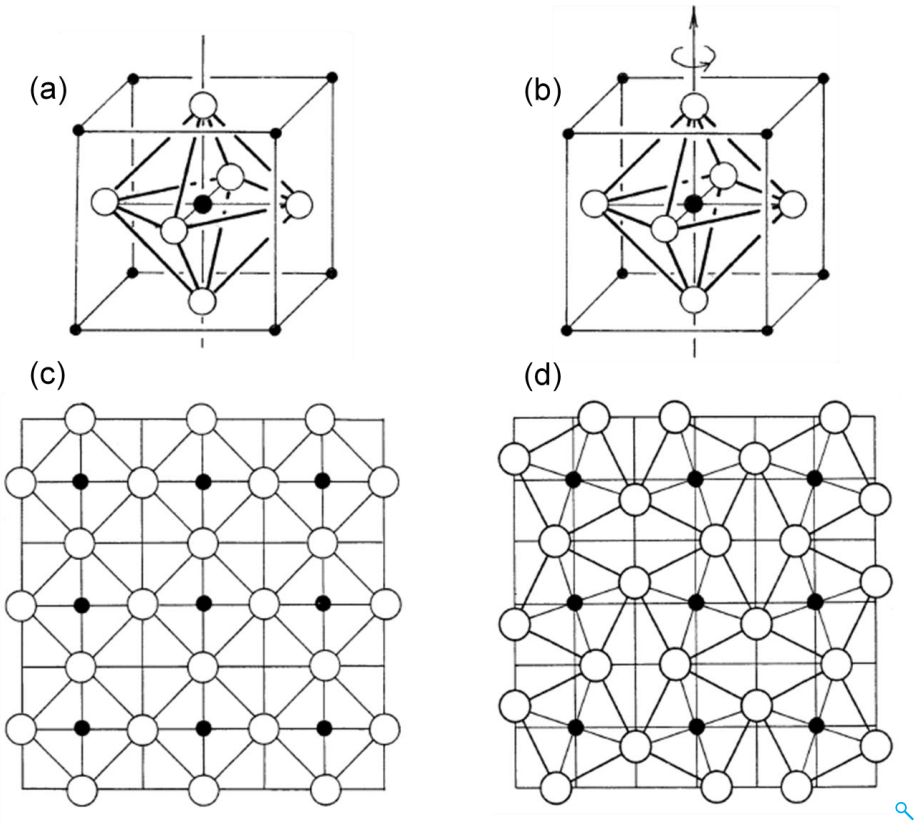

Figure 5.1: $SrTiO_3$ perovskite crystal structure, with a titanium atom at the center and oxygen atom in each of the six cube walls forming a cage around a titanium atom, and strontium atoms at the corners of the cube. (a) the normal phase, (b) rotation of TiO_6 octahedra around the C_4 axis in STO crystal, (c) atomic arrangement in the normal phase, (d) atomic arrangement after the TiO_6 octahedra rotation [130].

prism with one long axis (c-axis) and two short axes (a-axes). At 65 K the structure becomes orthorhombic and at 10 K possibly rhombohedral [33, 34, 128, 129]. The octahedra rotate in such a way that every neighboring octahedra in all three directions rotate in opposite direction as shown in the Figure 5.1. The long axis may be oriented along any of the crystal axes (X, Y, or Z) (see Figure 5.2). This structural transition leads to the formation of domains within STO characterized by the orientation of their unit cells. These domains follow a simple tiling rule: the dislocations are minimized, when tetragonal unit cells along X (100), Y (010) or Z (001) crystal directions share their short axes (a-axes) at domain walls (twin boundaries) [124], hence the boundary between X and Y domains must lie at 45° or 135°, between Z and X at 0°, and between Z and Y at 90° at the top surface as shown in Figure 5.2. Such domain wall patterns in bulk STO were first observed more than 50 years ago by polarized optical microscopy [34].

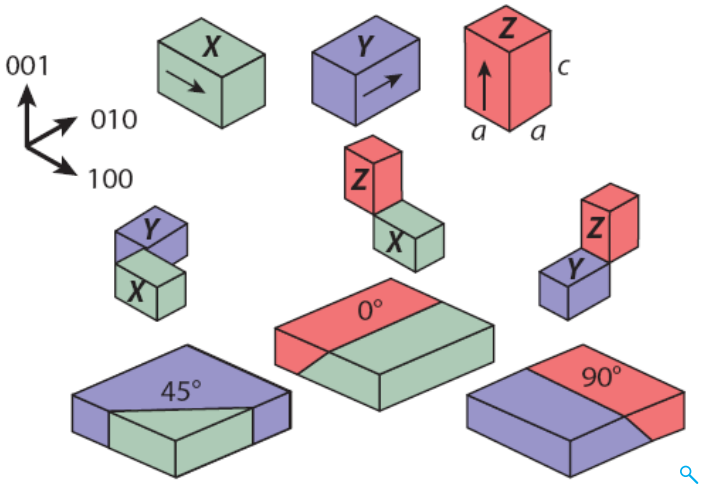

Figure 5.2: Below transition temperature the STO cubic unit cell becomes a prism, forming domains that are identified by the orientation of their long axis (c-axis), the c-axis may lie along the X (green), Y (blue), or Z (red) direction. To minimize the dislocations domains share their a-axis and as a result twin boundaries are formed having angles of either 0°, 45°, or 90° with respect to the crystallographic axes as viewed from above [124].

5.2 Influence of tetragonal domains on LAO/STO interface

The advent of novel suitable probes made it possible to study buried interfaces and to explore the influence of domain structure of the STO substrate on the properties of the LAO/STO interface. Using a nanotube quantum dot as a scanning charge detector, scanning single electron transistors (SET) are used to do noninvasive imaging of the mechanical response and electrostatic landscape in these buried interfaces [124]. These studies also revealed that domain walls could be moved by applied back-gate voltage, that coupled to the domain walls, perhaps through charged/polar domain walls or through anisotropic electrostriction [131, 132]. This domain wall motion leads to an anomalously large piezoresponse in STO. By considering the above mentioned tiling rules as shown in the Figure 5.2, the electromechanical response can be labeled in terms of domain orientations as shown in Figure 5.3 (right).

The tetragonal domains in STO lead to a varying potential landscape at the LAO/STO interface, which is constant for each domain but varies between in-plane (X or Y) and out-of-plane (Z) domains [124,133]. Due to the difference in surface potential, charge must transfer between domains of varying potentials in order to keep the electrochemical equilibrium. As a result, the 2DEG density is heavily enhanced at these walls. As the electron mobility strongly depends on the carrier density in the LAO/STO interface, such strong modulation

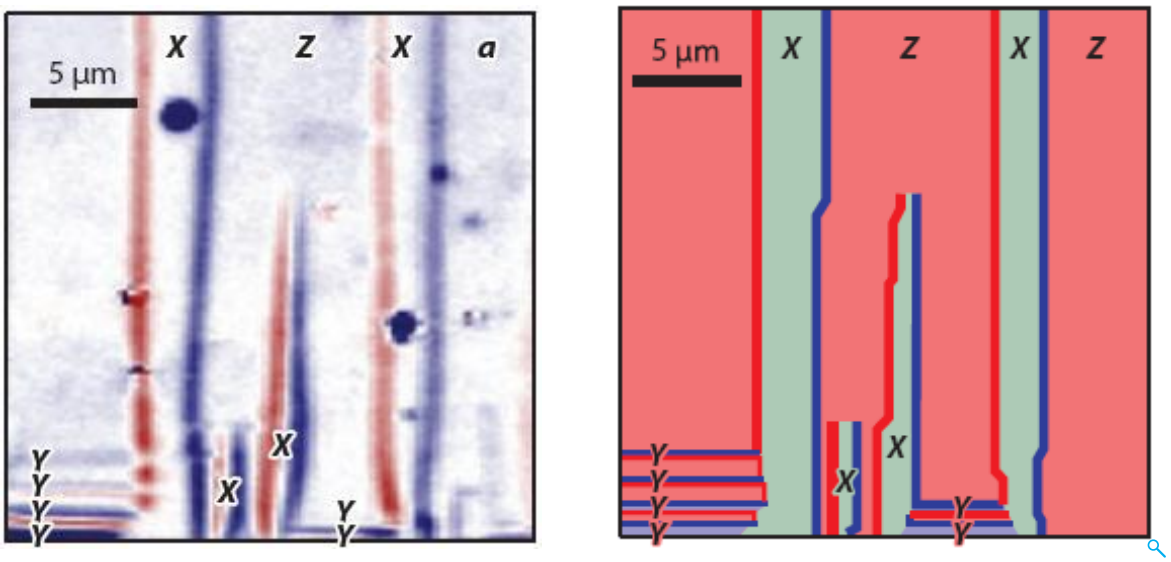

Figure 5.3: Voltage-induced domain wall motion in LAO/STO mapped by scanning SET across the LAO/STO surface, each stripe represents the motion of either the rising edge (red) or the falling edge (blue) of the potential step in the surface induced by an oscillating back-gate voltage (left). Labeling of schematic map according to color scheme of tiling rule, the dark red and blue line represent the domain wall boundaries (right) [133].

leads to channeled current flow between domains or at the domain walls. Another approach using scanning superconducting quantum interference device (SQUID) measurements also revealed the channeled current flow within the 2DEG [125]. In this approach, the SQUIDs pick up loop is used to capture the magnetic flux, which is generated by the current flowing in the interface, and these flux images are used to generate spatial map of current density at the LAO/STO interface. Different current maps are recorded that show current flows in channels at 4.2 K. After thermal cycling above 105 K, the pattern of current channels changes (see Figure 5.4). All these observations indicate the presence of domains in the STO. The current flow can be enhanced along the (100) and the (110) STO cubic crystallographic directions depending on the domain structure.

Polarized light microscopy is also used to confirm the tetragonal domains in the LAO/STO samples as a function of temperature [134]. Optical images of the LAO/STO domain structure taken at different temperatures, shows that the domains are present when the thermal cycle is performed above the transition temperature. They totally disappear when the images are taken above the transition temperature (see Figure 5.5). This temperature dependent view of domain configuration supports the channeled conduction due to the tetragonal domain configuration in STO. A strong modulation of the channel current was observed even

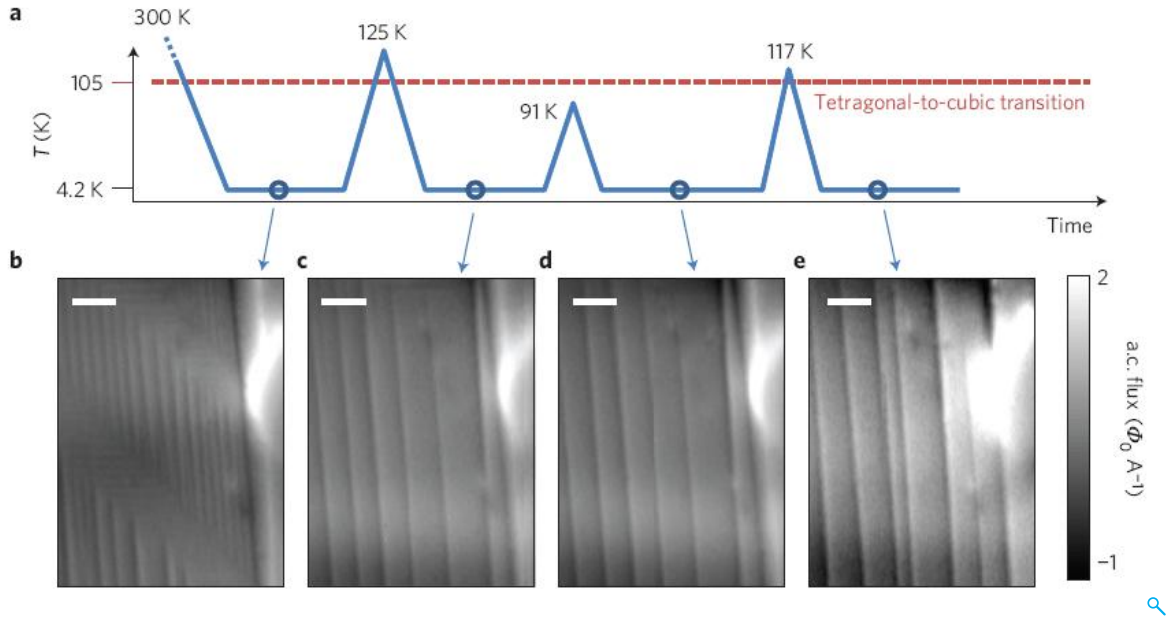

Figure 5.4: Narrow paths of enhanced conductivity originate from the tetragonal domain structure of STO. Thermal history dependent magnetic flux images taken at 4.2 K by SQUID pick up loop. (b) Initially cooling down from room temperature, (c) cycling to 125 K, (d) 91 K, (e) and 117 K. Pattern of the magnetic flux changes when the thermal cycle is performed above the transition temperature [125].

up to 95% when the microscopic distribution of current flow and macroscopic resistance measurement were performed simultaneously [135]. The interface is less resistive when the applied current flows along the tetragonal stripes as compared to when it flows perpendicular to the tetragonal stripes. This indicates how small structural changes in the crystal influence the electronic properties of LAO/STO heterostructures.

As with the other intriguing properties of the LAO/STO interface, domains at low temperatures has increased the complexity of this rich physical system. However, controlling this new degree of freedom at nanoscale may present new opportunities for engineering unique low dimensional nanostructures.

The effect of the domain configuration should become stronger as the lateral size of the nanostructures approach the characteristic size of the domains. For large structures, inhomogeneous current flow will statically average to zero, so no significant anisotropic transport can be expected in such samples. Until now, magnetic and optical studies have revealed the presence of tetragonal domains in STO at low temperature. The correlation between the interface conductivity and the local structure is not fully explored yet. We have patterned the LAO/STO interface in nano Hall bars to study this effect in detail. Here, we

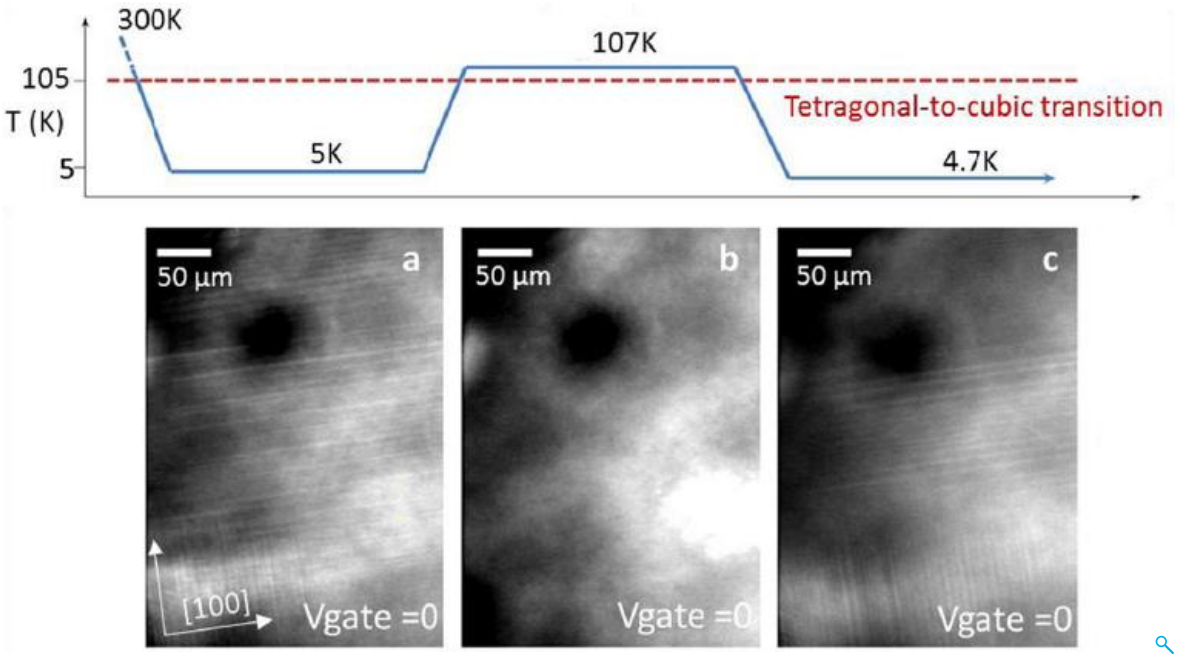

Figure 5.5: Optical images of the LAO/STO domain structure were taken at different temperatures by polarized light microscope. (a) Domains are observed at 5 K, (b) domains disappear above the transition temperature, (c) domains appear again with different configurations in the next cool-down [134].

present our results on the transport properties of the interface that focused on the regions where structural transitions take place. We have observed a huge increase in sheet resistance of the nanostructured samples due to structural transition of $SrTiO_3$ substrate [136].

5.3 Sample preparation

All films used in these experiments are deposited by pulsed laser deposition (PLD) as described in Section 3.2. During growth, the background oxygen pressure is kept at 10^{-3} mbar. LAO layers are deposited from a single crystal LAO target on TiO_2-terminated STO (001) substrates [72, 109]. The substrate temperature during deposition is 850 °C, and Laser fluence and pulse frequency are kept at 2 J/cm^2 and 2 Hz, respectively. Reflection high-energy electron diffraction (RHEED) is used to monitor the layer thickness with unit cell resolution during the growth. After deposition of 6 unit cells of LAO, the sample is slowly cooled down to room temperature, while the oxygen pressure is maintained. As a result we obtain layers with a sheet resistance of 133 Ω/□ and a typical mobility of $1.124\text{x}10^3 cm^2V^{-1}s^{-1}$ at 4.2 K.

In the next step, these layers are patterned into nanosized Hall-bars. Two different pro-

cesses are used in order to allow us to check for possible artifacts from processing.

5.3.1 Nanopatterning by e-beam lithography and RIE

For patterning, a thin film of novolack based image reversal resist is deposited by spin coating as described in Section 4.2. We have used AR-U4060 photoresist for a negative process. Subsequently, the sample is exposed by e-beam lithography. The exposed pattern consists of nanosized Hall-bars. The sample is developed with the developer solution (AR-300-26, we have used the developer in dilution of 1:4). After development, reactive ion etching is performed in an inductively coupled plasma reactive ion etching system (ICP-RIE, Oxford Plasmalab 100) using a BCl_3-based etching process to completely remove the LAO layer (for more detail see Section 4.2.2). After etching, the resist is removed using N-Ethylpyrrolidone at 60°C for 3 hours [104].

5.3.2 Nanopattering by amorphous LAO hard mask

To avoid possible artifacts from the patterning process, some samples are patterned by using an amorphous hard mask. With some modification, the recipe of Schneider et al. [105] is used. An epitaxial 2 uc of LAO is grown on STO using the same parameters as described above. Subsequently, negative e-beam lithography is done and amorphous LAO is deposited at room temperature and patterned by lift-off. Then a 4 uc layer of epitaxial LAO is deposited in an oxygen pressure of 10^{-3} mbar. However, epitaxial growth can only occur in the places where no amorphous LAO is present. As a consequence, only in these areas a conducting LAO/STO interface can form. The sample is then cooled down to room temperature in 1000 mbar of O_2. The cool-down includes a 1 h annealing step in oxygen at 600 °C. All resulting patterned structures are stable at ambient conditions.

5.3.3 Electronic transport measurements

The transport experiments are carried out in a ^{4}He bath cryostat with a variable temperature insert. The samples are cooled down at a rate of approx. 5 K/min and warm-up is done at a rate of approx. 2.5 K/min. The resistance is measured in a four probe geometry using a nanosized Hall-bar. The active region between the voltage leads has a length of 3.5 μm and the width varies from 500 nm to 100 nm. The applied DC voltage is 80 mV and the current is measured using a 1 MΩ series resistor. Voltages are measured using custom made zero drift voltage amplifiers and an Agilent 34420A 7.5 digit nanovoltmeter.

For large area Hall bars (length = 600 μm and width = 200 μm), the resistance of the electron gas at the interface between two band insulators LAO and STO typically drops monotonically with temperature, and R/T curves during cooling and warm-up look identical. During warm-up, the resistance follows the same temperature dependence as during cool-down. This behavior is in agreement with both transport models; polar catastrophe and the presence of oxygen vacancies. In literature, the transport in nanostructures is also reported, however, in one technique these structures were patterned from a non-conducting interface and conductivity was locally induced using a conductive atomic force microscope (AFM) tip [16] whereas, the other have used ion implantation to pattern the LAO/STO interface [108]. However, it should be noted that Aurino et al. [108] did not investigate cool-down and warm-up curves. None of these studies have observed the effect of structural transition of the STO substrate on the LAO/STO interface.

A unique behavior was observed when the temperature dependent resistance measurements were performed in nanostructured samples. Though the cooling curve corresponds to the one observed for large area structures however, the warm-up curve exhibits one or two massive peaks in resistance, which typically occur at the temperatures associated with structural phase transitions of STO substrate. We performed a series of experiments on a number of different samples in order to identify the origin of this effect.

5.4 Results

Figure 5.6(a) shows a typical temperature dependence of the conductance of a large area Hall-bar. The resistance decreases monotonically during cool-down. During warm-up the curve is reproduced, except for a small hysteresis. This artifact is due to lag of the sample temperature with respect to the sensor. Even when the sample was kept at low temperature for days no deviation appeared. For Hall-bars with a width of less than 500 nm, the cooling curve is similar to the one of a large area structure. During warm-up, however, a strong non-monotonicity is observed. At a certain temperature, the resistance increases up to a maximum, which can even be much higher than the resistance at room temperature (Figures 5.6 and 5.7). When the temperature is further increased, the resistance decreases again and finally the resistance curve again joins the one obtained during the cooling process. This resistance peak typically occurs at approximately 80 K. In some cases, this is followed by a second smaller peak well above 100 K.

We never observed this behavior for large area structures. It is almost universal for nano-sized Hall-bars. The exact shape and height of the resistance peak varies from structure to

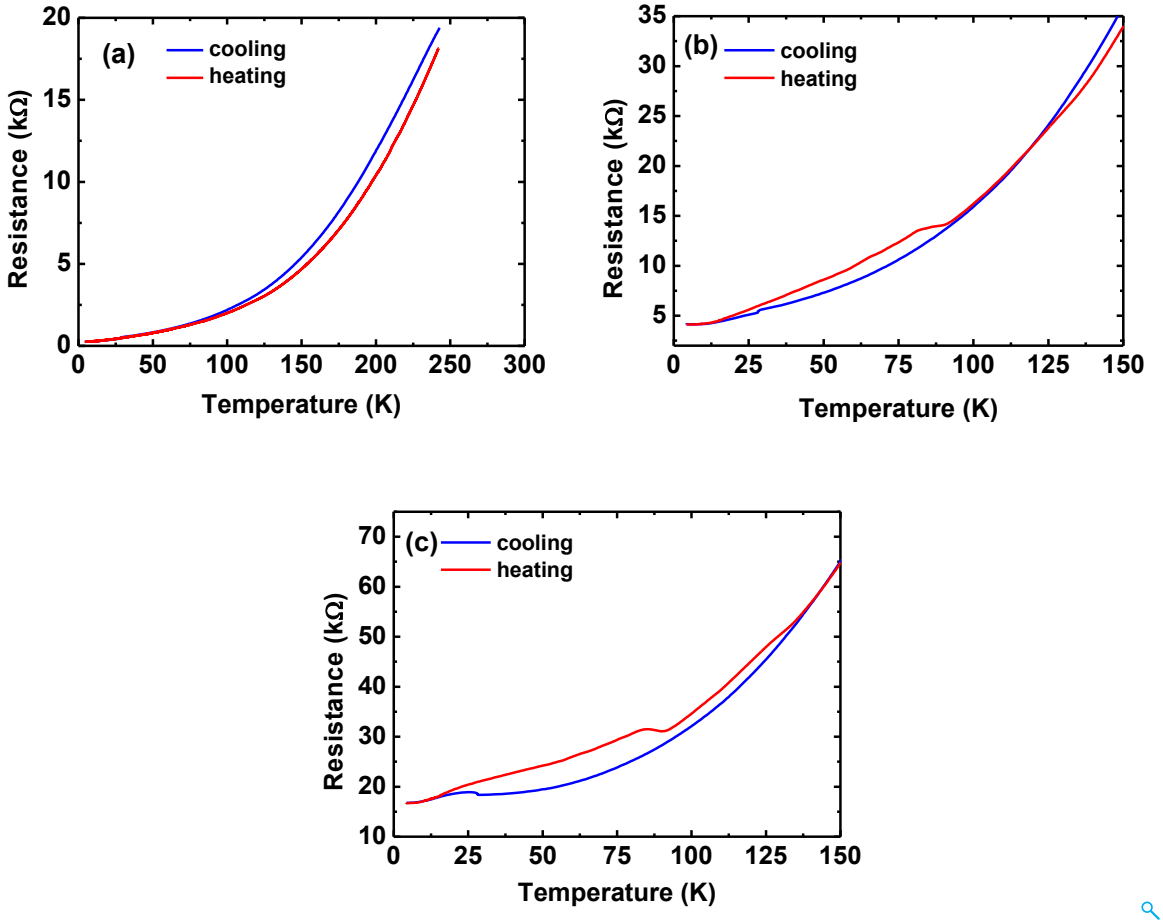

Figure 5.6: Temperature dependent resistance of the q2DEG for different size structures. (a) A large Hall bar structure, (b) a 400 nm wide Hall bar, (c) and a 200 nm wide Hall bar. For the nano Hall-bars a non-monotonic behavior is visible with a resistance peak at approximately 80 K. For 400 nm width the resistance at 80 K is only about 15% higher than in the cooling curve, for 200 nm the difference is 20% .

structure. The effect is reproducible, however, the height of the peak depends on the history of measurements. In order to identify the origin of the phenomenon, we performed a series of investigations by varying a number of parameters.

5.4.1 Temperature dependence

In first set of experiments, we vary the minimum temperature (T_{min}) of the cooling cycles. The sample is always kept for one hour at T_{min} before the sample is warmed up. As long as T_{min} is below the peak temperature T_{peak}, the peak appears reproducibly at the same temperature of approx. 80 K (see Figure 5.7), however, the peak height increases when

the minimum temperature is decreased. When the minimum temperature approaches the temperature of the resistance peak, the effect vanishes completely. The data is shown in Figure 5.7.

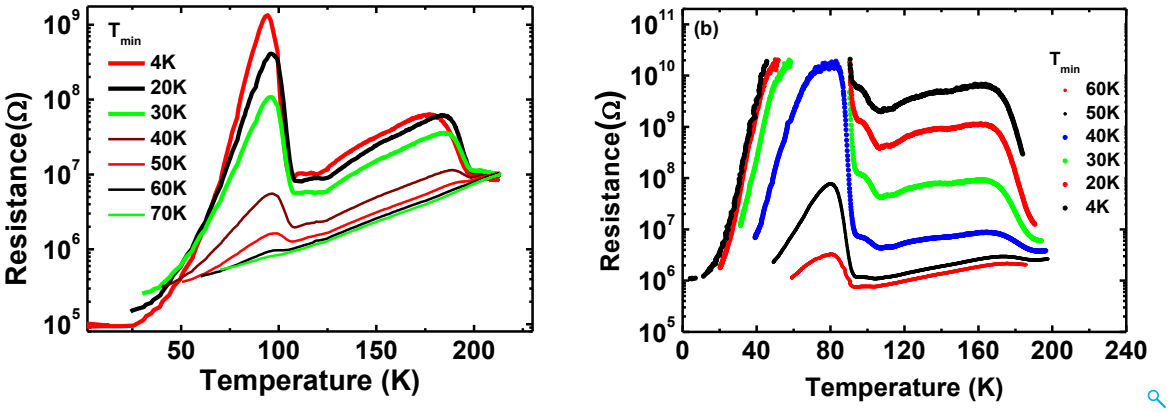

Figure 5.7: Warm-up curves for two 100 nm wide Hall bars starting at different minimum temperatures T_{min}. For lower T_{min} the peak is much higher. For the 2nd sample (b) the resistance maximum is well beyond the measurement limit for $T_{min} < 40$ K.

5.4.2 Stability over time

We have investigated two aspects of time dependence. In the first series of experiments, we vary the waiting time at the lowest temperature i.e. 4.2 K. The minimum time is obtained by cooling down and immediately warming up when 4.2 K is reached while the maximum waiting time is 24 hours at 4.2 K. In these experiments, we have observed small variations (as explained below that the measurement history can influence the experiment) but no systematic change in peak height is observed.

In the second experiment (Figure 5.8), we stop the warm-up procedure for approx. 12 minutes at 60 K and 70 K (below the peak temperature), respectively, and a third time at 80 K which for this sample is the temperature of maximum resistance. The curves obtained at 60 K and at 70 K, respectively show the following behavior. In both cases resistance has already increased. When the warm-up is stopped the resistance increase continues for several minutes and finally saturates. At 60 K, the starting point of this curve is at $5x10^6\Omega$ and the resistance increases up to $2.5x10^7\Omega$ within 4 minutes. At 70 K, the curve starts at $5x10^7\Omega$ and increases up to $2x10^8\Omega$ within another 4 minutes. At 80 K, however, the resistance does not increase any further, but decreases massively and after 10 minutes it approximately reached the corresponding value of the cooling curve.

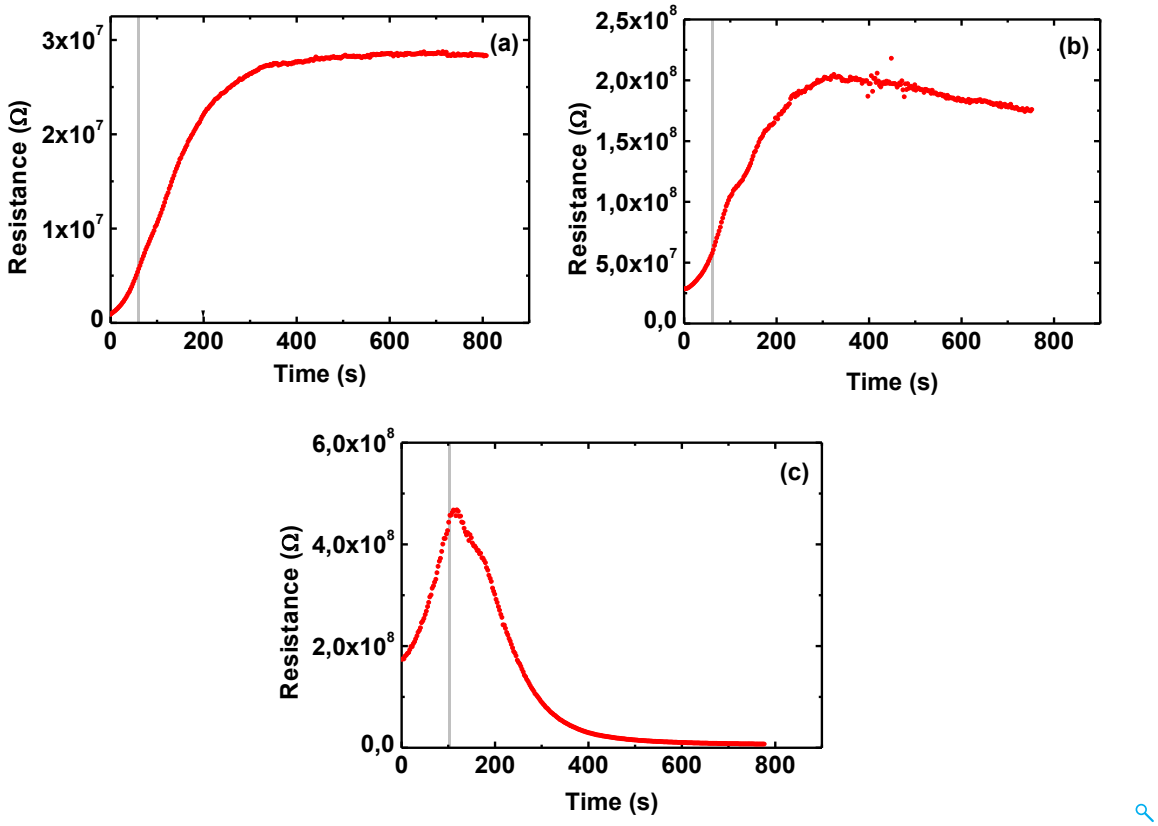

Figure 5.8: Warm-up curves for a 100 nm wide Hall bar with waiting times at different temperatures. (a) The sample is warmed from 50 K to 60 K (left hand side of grey line) and the temperature is then kept stable for approx. 12 minutes (right hand side of grey line). (b) Similar as (a) only now the sample is heated from 60 K to 70 K where the temperature is kept stable. In (c) the process is repeated, now heating from 70 K to 80 K. While below the peak maximum (a and b) the resistance further increases while the temperature is constant beyond the peak maximum at 80 K the resistance drops over time although the temperature is constant.

5.4.3 Sample patterned by other method

All the above mentioned results are obtained for the samples that have been fabricated using a subtractive etching process as mentioned in Section 5.3.1. In order to confirm the basic nature of the observation, we test additional samples fabricated by amorphous LAO hard mask as described in Section 5.3.2. For these samples, we also see a pronounced peak as shown in Figure 5.9, which confirms that the lateral size restriction is the relevant factor for an increase in resistance.

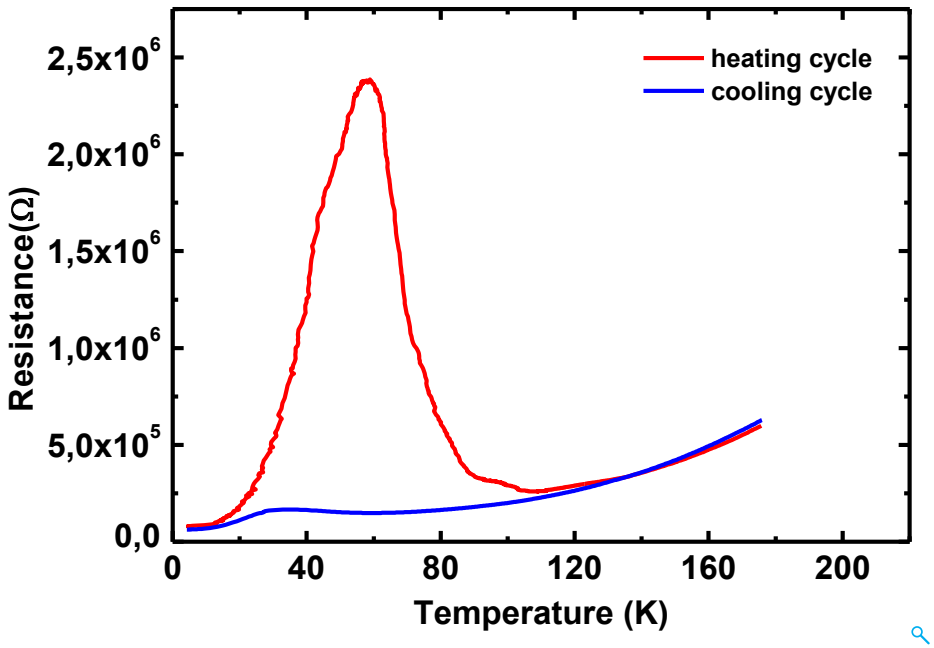

Figure 5.9: Cooling and warm-up curve for a 100 nm wide Hall bar fabricated using the process described by Schneider et al. Again a massive peak is observed. Even a small resistance peak is visible in the cooling curve.

5.5 Discussion

It is likely that temperatures at which the resistance peaks occur, the effect originates from various structural phase transitions that STO undergoes at low temperatures as described in Section 5.1. In the proceeding paragraphs, the upper phase transition temperature (T=105 K) will be labeled as TC_1, while the lower one (T=65 K) as TC_2. A third transition to a rombohedral phase well below 30 K is also suspected.

Modulation of the electrostatic potential on domain walls have been reported by scanning single electron transistor, which results in an enhanced current flow along domain walls [124]. Another approach using scanning SQUID microscopy also revealed that at low temperature the current distribution in large area LAO/STO heterostructures was no longer homogeneous, but current filaments were formed along the domain boundaries in the STO substrate [125]. In these experiments, a filamentary pattern of higher current density was observed at T= 4.2 K. This is in agreement with typical domain pattern in STO. The formation of domains was also confirmed by polarized light microscopy [134]. Optical images of temperature dependent domain structures support the channeled conduction due to the STO tetragonal domain configuration. Recently, a strong modulation of channel current was ob-

served even up to 95% when the microscopic distribution of current flow and macroscopic resistance measurement was performed simultaneously [135]. The study also reveals that the interface is less resistive when the applied current flows along the tetragonal stripes compared to when it flows perpendicular to tetragonal stripes (Section 5.2). Such modulation in conductivity on domain walls also supports recent study of local piezoelectric response in STO, accredited to domain wall polarity that arises well below the phase transition temperature (at ≈ 80 K) and becomes intense at 40 K [137].

The filamentary current distribution alone, however, is not sufficient to explain the non-monotonic temperature dependence that we observed in nanostructures. Since, the latter only appears during warm-up and not during cool-down, additional physics needs to be taken into account.

When the temperature falls below TC_2 during cool-down (Figure 5.10a), the appearing domain walls exhibit large electric field due to piezoelectricity and the large dielectric constant. Charge and thus current flow starts to accumulate at the domain boundaries as described in [125, 135] (cooling just below TC_1 yields no effect). This may be accompanied by the pinning of defects at the domain walls. These defects can trap and release carriers and lead to a longer time constant for charging and discharging. A marked increase in the dielectric constant of STO observed at lower temperatures may cause an additional stabilization of the current paths. The homogeneous conductivity decreases whereas filament conductivity increases, resulting in a maze of a limited number of conducting filaments at the domain boundaries with high-resistivity (Figure 5.10b) or even insulating regions (Figure 5.10c) inside the domains. Due to this maze, there are always conducting paths below the phase transition. During the cooling normally the resistance decreases for LAO/STO interface. This effect is not visible because accumulation of charge does not significantly alter the mobility. In fact, the accumulation of charge could lead to additional screening, which further reduces scattering. The effect itself is reminiscent of conducting domain walls in insulating $BiFeO_3$. Similarly, in our samples, large electric fields occur at the domain walls. They can attract charges and charged defects and thus lead to observations described below.

When the sample is warmed-up, the situation is different because the current is already concentrated in the filaments. When the temperature approaches the phase transition temperature, all the filaments are not broken all of sudden. On contrary, at some point close to TC_2 a few domain boundaries disappear, while the rest of the domain structures remain intact. As a result, only a few filaments become unstable showing that the charge is no longer pinned by local fields. The adjacent domain walls can now attract the remaining charge, which was formerly pinned and thus increase the local resistance up to infinity. Large area samples have

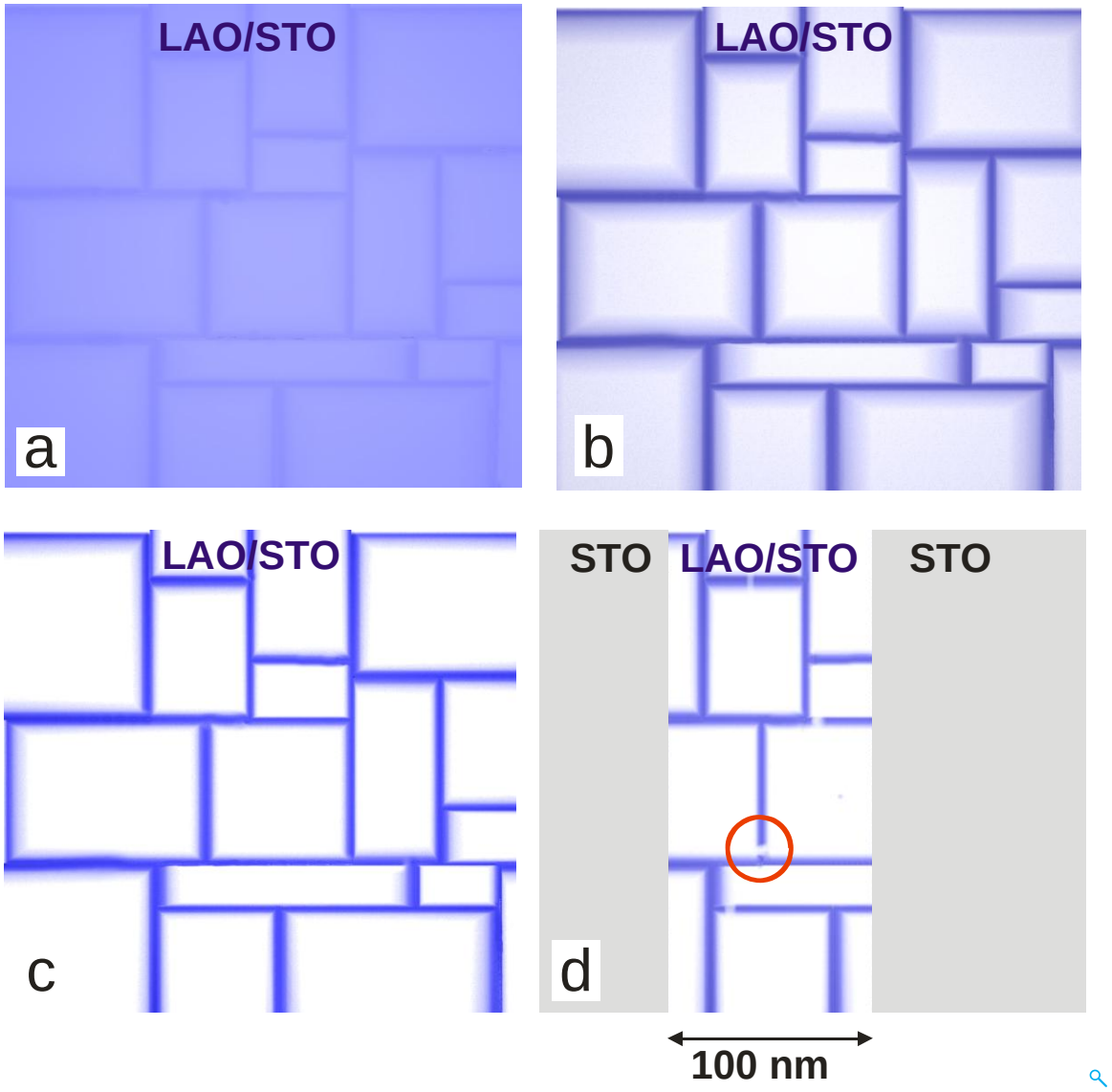

Figure 5.10: Simple sketch of a toy domain configuration, which can cause the effect observed in our experiments. Dark Blue (gray) regions correspond to higher conductivity, light areas have low conductivity and white areas are insulating. (a) Below TC_2, filaments form and oxygen vacancies start to accumulate at the domain boundaries. (b) After some time the domain boundaries are the main conducting paths, the inside of the domains is slightly conducting. (c) Finally, the full conductance of the sample is through the domain walls. Areas are insulating. (d) Situation in an etched nanostructure at warm-up. The STO (sides) is insulating while in the center (LAO/STO) filaments persist. The domain walls have disappeared, however, the vacancies have not yet been redistributed. If at a critical position a filament breaks (circle), no conductance is left.

literally millions of current filaments due to their lateral size. The interruption of some of filaments only leads to a redistribution of the current into other filaments, which is virtually undetectable. However, in nanostructures the current is limited to one or at least a few filaments at low temperatures (Figure 5.10d). Suppose a nanostructure has two filaments, when one of the filament is broken the resistance will be doubled. When the conduction is through a single filament, the resistance may increase dramatically or even become unmeasurable.

At temperatures below the phase transition, the situation is stable over time as charges are still bound to domain boundaries and the broken link cannot be mended. Only when the temperature is raised beyond TC_2, the domain walls disappear and charges become mobile again and are redistributed with a certain time constant. This redistribution is not instantaneous, even above TC_2 it occurs over certain span of time. Depending on the domain geometry, the process may be repeated at TC_1 if the charge is not yet fully redistributed, leading to a second peak in resistance. Obviously, the total number of filaments is higher in bigger structures. However, it should be noted that no direct proportionality is expected, because of the statistical distribution of lateral domain size. Statistically, this picture nicely corresponds to our observations. We did not observe any peak in resistance for large area structures. Nanostructures with a width of less than 500 nm, always show some peak in resistance. For some of them, especially for those of about 100 nm size, the resistance increases above the room temperature value or even beyond the measurement limit. In large area samples, small peaks in resistance have been reported by other groups previously [61, 138, 139], however, an adequate explanation was not given.

We now compare this model with our additional experimental data. The finite rise time of the resistance peak (Figure 5.8) is explained by the nature of the phase transition during warm-up. The phase transition occurs over a certain time and temperature range. Taking into account that the lattice also contracts further during cooling or expands during warm-up, the domain structure cannot be seen as static, but as something that undergoes small modifications with the change in temperature, at least close to TC. Therefore, an increase in resistance occurs gradually over a certain temperature range and starts below TC. Also, the charges need to migrate away from the vanishing domain wall towards the remaining one, which can be a slow process. This describes adequately the rise in resistance upon stoppage of warm-up at 60 K or 70 K (Figure 5.8 a and b), which are apparently below the phase transition in this sample. At 80 K, which is above the phase transition, the domain walls disappear and charges become mobile, leading to a drop in resistance over time (Figure 5.8 c). The time constant of this decrease is determined by charge diffusion and by trapping of defects, because there is no other restoring force to redistribute the charge in the sample.

Depending on the domain structure, the size of the rupture and the geometry of electric fields are different. We expect a variation of peak shape and stability over time not only from sample to sample but also in some cases from measurement to measurement.

It is important to realize that the maximum resistance is determined by the degree of depletion of the areas between filaments and not by the high conductivity of the filaments themselves. A simple gedankenexperiment shows that if the sheet conductance was reduced to 1% of the original value, the resulting increase in resistance for all filaments breaking still cannot be more than two orders of magnitude. The increase observed in our case, indicates quasi fully insulating domains. Based on this, the model also fits the experiments with different T_{min}. Apparently, cooling to lower temperatures takes more time and leads to stronger accumulation at the domain boundaries, because the dielectric constant of STO increases with lowering in temperatures. This leaves less charge carriers for sheet conductance at lower T. As the sheet conductance determines the peak height, the peak must be higher for lower T_{min} as seen in the experiment despite the identical pattern of the filaments. The second peak, which is occasionally observed (Figure 5.7a) is also readily explained. When the resistance has decreased from the peak maximum to the original value above TC_2 the sheet conductivity may not necessarily be completely homogeneous. It indicates that a new maze is established. The next phase transition at higher temperatures can thus again interrupt the current flow, provided that the temperature had fallen below TC_2 during the experiment. It is not even self-evident that at room temperature, the carriers again reach a completely homogeneous distribution. At low temperatures, the electric fields at the domain boundaries can collect the charge carriers whereas at higher temperature, the domain walls are no longer present so there is no electric field except for possible Coulomb repulsion which reestablishes a uniform distribution. As a consequence, any further experiment can be influenced by the history of measurements and the peak height may vary, even for apparently identical temperature cycles. The results are also consistent with the AFM induced conductivity, mentioned in the beginning, where electric fields create local conducting paths in an insulating environment, which are stable up to room temperature.

Theoretically, nanostructures may exhibit a peak in resistance even during cool-down. When the filaments are established below 80 K, the third phase transition (below 30 K) can lead to similar scenario. For at least one structure, we observed a resistance peak during cool-down below 30 K (Figure 5.9), especially after several temperature cycles. Accordingly the observations in large area structures [61, 138, 139] can be explained. Normally, the effect should not occur in the large area structures, it is however possible that the current distribution in a large area is inhomogeneous and close to the percolation limit. In this case,

the disappearance of a few filaments during warm-up can at least slightly decrease the conductance as observed in [61, 138, 139]. However, the statistical probability for observance of this effect is very low.

Although, the picture outlined above yields a good explanation for our observation it is pertinent to discuss few alternatives. Since, the effect appears at the phase transition temperature it has a relevance to domain structure and the question arises whether the conducting domains and the insulating domain walls could also be a suitable scenario? This can be quickly dismissed as vanishing domain walls during warm-up would lead to a decrease in resistance rather than an increase. Also, it is important to consider the role of defects induced by the etching process, which might also change the temperature dependence of the resistance. Here a number of arguments can be setup against. Indeed a depletion region had been observed as described in the previous chapter [104]. However, this region was very narrow and located at the edges of the structure. There might be an interplay of these defects with the domain boundaries. However, one would expect a strong decrease of the effect when the width was increased from 100 nm to 200 nm, which was not the case in actual. Also, we utilized two different patterning processes, one even without etching and both led to similar large effects. It seems that conducting domain walls with insulating regions in between is the most likely explanation, although we were not able to determine the exact pinning mechanism.

Finally, two examples of nanopatterned LAO/STO structures should be discussed which at first glance seem to contradict our findings [140, 141]. These investigations involved nanostructures which were not fabricated by conducting AFM and yielded a completely monotonous dependence of resistance on temperature. There is, however, a likely explanation. Firstly, Stornaiulo et al. [140] have only investigated a minimum width of 500 nm which was above the threshold of 400 nm emphasized in our case. Aurino et al. [141] used a minimum structure of 100 nm, but with a $SrCuO_2$ capping layer. Nevertheless, none of the two papers compared cool-down and warm-up curves, and most likely the measurements shown were done during cool-down.

5.6 Summary

In this chapter, the effect of phase transitions of STO substrate on the conductivity of the 2DEG at the LAO/STO interface has been thoroughly studied. We have observed that LAO/STO nanostructures show one or two peaks in resistance when warmed up from low temperatures. The peaks occur at the temperatures representing structural phase transitions

of STO. The peak height depends on the minimum temperature, from where the cool-down starts. Above the critical temperature, the maximum resistance is not stable over time, but goes back to normal value after approx. 10 minutes.

To avoid the possible artifacts from the patterning process, samples were patterned by using two different patterning procedures via, direct patterning by RIE and by using an amorphous LAO hard mask. All the samples showed same effect during warm-up from low temperatures. We can explain the behavior by considering the formation of current filaments at the boundaries of the domains that appear during the structural phase transition at TC_2 in the STO and which may break during warm-up. The filaments are formed because large electric fields at the domain boundaries together with an increasing dielectric constant leads to an accumulation of charge carriers at the boundaries, leaving area inside the domain basically insulating. The assumption of a homogeneously conducting LAO/STO interface seems to be no longer valid when the transport experiments are performed below the transition temperature of STO substrate.

Chapter 6

Electric Field Effect experiment by top gating

6.1 Electrical gating of LAO/STO heterostructures

Silicon field-effect transistors (FETs) are the backbone of modern electronics. About 10^{19} of such transistors are manufactured each year to operate the daily life electronic appliances including cellular phones, cars and computers. The conventional FETs consists of source (S) and drain (D), a conducting channel between them, and a gate (G) terminal. The conducting channel and gate electrode are separated by a dielectric layer. With this configuration the conducting channel and gate form two electrodes of a parallel plate capacitor. Application of gate voltage leads to the accumulation or depletion of charges in the conducting channel. As a result the carrier density and thus resistance of the conducting channel is altered [1, 142, 143].

Oxide materials have diverse electronic and magnetic properties as compared to semiconductors, which make these materials a good candidates for the field effect experiments. Oxides FETs are investigated to enhance the FET functionality and to overcome the scaling limitations of silicon-based devices [144]. There are two common methods (top gating and back gating) for electrical gating of LAO/STO structures. In top-gating the electrical field is applied from top and thin LAO layer is used as gate dielectric, whereas in back-gating the electrical field is applied from back and thick STO substrate is used as gate dielectric as shown in the Figure 6.1. The top gating was used to modulate the 2DEG carrier density in a 4 u.c LAO/STO heterostructures. In the negative biased configuration the 2DEG was depleted and metal-insulator transition took place by the application of gate voltage [145]. The back gate configuration uses larger dielectric constant of STO (≈ 300) as compared to LAO (≈ 25).

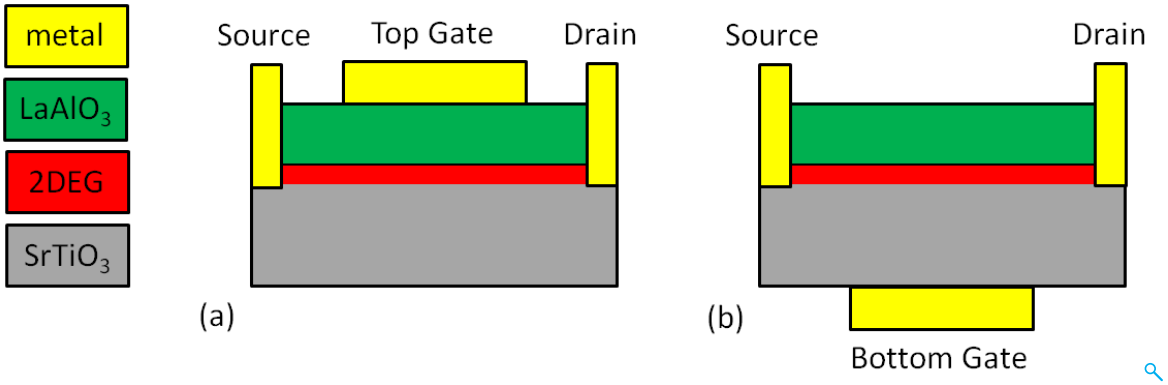

Figure 6.1: Two common methods for electrical gating of LAO/STO heterostructures. (a) Top gating, where the electrical field is applied from top and thin LAO layer is used as dielectric. (b) Bottom gating, where the electrical filed is applied from back and thick STO substrate is used as dielectric.

Back gating was successfully used to modulate the conductivity of 2DEG at LAO/STO interface through a quantum phase transition from an insulating to a metallic state [15], and was also used to discover interfacial superconductivity at the LAO/STO interface [82]. Moreover, using 2DEG at the LAO/STO interface as drain-source channels, field effect devices have been demonstrated by back-gating [17], side-gating [146] and top-gating [18–20, 30]. Also arrays of thousands of FETs and monolithic integrated circuit of functional oxides have been demonstrated [147].

Although the back gating is robust and reliable, still there are some drawbacks. Back gating is a global technique, it changes the carrier density in the whole sample upon application of electric field. Moreover, the high gate voltage up to several hundred of volts are required to achieve some reasonable effect due to thickness of gate dielectric, which is typically 0.5 mm. Structural phase transition of STO substrate at low temperature should also be considerd while using back gating. STO has a cubic crystal structure at room temperature. At low temperature, T=105 K oxygen octahedra rotate as a result cubic symmetry is broken and unit cell becomes tetragonal [33, 34, 128]. As mentioned in Chapter 5, this structural transition leads to the formation of domains within STO [124]. Recently, it has been revealed, that domain walls can be moved by applied back-gate voltage, which couples to the domain walls, perhaps through charged/polar domain walls or through anisotropic electrostriction [131, 132]. The domain walls movement causes the change of the conductivity at the surface of the STO substrate, which affects the properties of 2DEG at the LAO/STO interface.

To resolve these issues, we decided to use top-gating technique to fabricate the field-effect devices. We have physically patterned the q2DEG generated at the LAO/STO interface down to lateral dimension as small as 100 nm, while maintaining its conducting properties, using e-beam lithography in combination with dry etching as described in the Chapther 4. Now we want to fabricate field-effect devices that utilize the two-dimensional electron gas generated at the LAO/STO interface. Micrometer Hall bars are patterned, to explore field effect on the carrier density for various LAO thicknesses. In this chapter different approaches which are used to fabricate the FETs will be explained.

6.2 Patterning of top-gated LAO/STO heterostructures

Top-gating is a natural complimentary technique used to tune the electronic properties in the conventional semiconductor systems. Here we want to use top-gating technique to fabricate the field-effect devices. The LAO has large band gap (5.6 eV) and the high dielectric constant, so the thickness of LAO can be used as gate dielectric. The advantage of top gate is that the gate dielectric is very thin (a few mono-layers) and small voltage (a few volts) is required to operate the devices. We have tried following three processes for top-gating.

6.2.1 Patterning of LAO/STO heterostructures by RIE

The following process is used to deposit LAO/STO heterostrtuctures and subsequently ex-situ metal gate to realize the field-effect devices.

Thin layers of LAO are grown from a single crystal LAO target on TiO_2-terminated STO (001) substrates as described in the Section 3.2. Oxygen is used as a background gas at a pressure of 10^{-3} mbar during deposition. During deposition, the substrate temperature is 850 °C, and Laser fluence and pulse frequency are kept at 2 J/cm^2 and 2 Hz, respectively. To monitor the layer thickness up to unit cell level in-situ reflection high-energy electron diffraction (RHEED) is used during the growth. After deposition the samples are slowly cooled down to room temperature while the oxygen pressure is maintained. In this way, films of different thickness (6 uc and 20 uc) of LAO are deposited.

For patterning, a thin film of novolack based image reversal resist (AR-U4060) is deposited by spin coating as described in Section 4.2. Here, the photoresist is used for a negative process. Subsequently, the sample is exposed by photolithography. The exposed pattern consists of Hall bars with dimensions (length = 600 μm and width = 200 μm) including large area bond pads. The sample is developed using photolithographic developer solution (AR-300-26, we have used the developer in dilution of 1:4). After development, re-

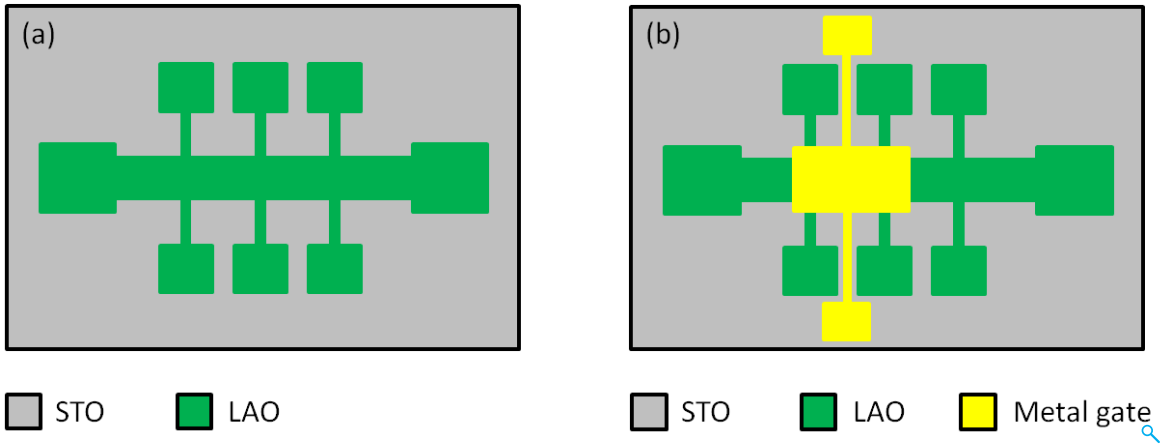

Figure 6.2: Top view of the patterned sample. (a) Patterned LAO Hall bar on STO substrate. (b) Metal gate on top of Hall bar.

active ion etching is performed in an inductively coupled plasma reactive ion etching system (ICP-RIE, Oxford Plasmalab 100) using a BCl_3-based etching process to completely remove the LAO layer (for more detail see Section 4.2.2). After etching, the resist is removed using N-Ethylpyrrolidone at 60 °C for 3 hours. The photolithography step is repeated to define the top-gate structure and subsequently top metal gate Pt/Au 10/90 nm is deposited by e-beam evaporation and lift-off is done. The top view of the patterned sample can be seen in Figure 6.2. The Hall bars and metal gate are bonded using Al wire for electrical transport measurements. The bonds are placed directly on the LAO without additional metallization.

Electrical characterization

After patterning and bonding the samples, electrical transport measurements are carried out in a ^{4}He bath cryostat in the temperature range of 4.2 – 300 K. The voltage drop over the sample and the reference resistor are measured using high impedance difference amplifiers and an Agilent 34420A nanovoltmeter. First, we checked the conductivity of the patterned Hall bar structures; the sheet resistance is $10 k\Omega/\square$ at room temperature, and $0.20 k\Omega/\square$ at 4.2 K. The resistance between different Hall bars is in the range GΩ at room temperature as well as at 4.2 K, showing good insulation between the devices.

During the measurements we have realized that the gate leakage current I_G (in the range of 10^{-6} A) is significantly big and is same order of magnitude as that of drain source current I_{DS} at room temperature. We have also done measurements at 4.2 K and found gate leakage current I_G (in the range of 10^{-5} A) which was also comparable to drain source current I_{DS} at 4.2 K. We have grown another thicker sample LAO (20 uc), but found the same results. It

means that the thickness of LAO layer has no effect on the high gate leakage current. The possible explanation of this high gate leakage current could be that the metal gate directly sees the 2DEG at the LAO/STO interface.

To minimize this high gate leakage current I_G we added an extra step during the fabrication of device. Instead of depositing the metal gate directly on top of Hall bars, we deposited 20 nm AlO_x blanket by e-beam evaporator in between the LAO and metal gate. After the measurement we obtained the same results, AlO_x blanket has no significant effect on the leakage current. The possible reason for this could be the tunneling of metal through the dielectric materials during the deposition. By e-beam evaporator it is not possible to deposit fully oxidized AlO_x layer, which could be the reason of high gate leakage current. It may be avoided by depositing AlO_x layer in high oxygen pressure.

6.2.2 Additional $LaSrMnO_3$ layer on LAO/STO heterostructures

In literature [18] attempts have been described, where a conducting oxide layer was epitaxially deposited on top of the LAO, which led to improved gate action. We used LSMO as conducting oxide to mimic the process and to check its suitability. The following steps are followed to prepare the sample.

First thin layers of LAO are grown from a single crystal LAO target on TiO_2-terminated STO (001) substrates as described in the Section 3.2. Oxygen is used as a background gas at a pressure of 10^{-3} mbar during deposition. During deposition, the substrate temperature is 850 °C, and Laser fluence and pulse frequency are kept at 2 J/cm^2 and 2 Hz, respectively. To monitor the layer thickness up to unit cell level, in-situ reflection high-energy electron diffraction (RHEED) is used during the growth. After deposition the samples are slowly cooled down to 700 °C and subsequently 20 nm LSMO is deposited. During LSMO deposition oxygen background pressure is kept at 0.2 mbar, and Laser fluence and pulse frequency are kept at 2.5 J/cm^2 and 5 Hz respectively. After deposition the samples are slowly cooled down to room temperature while the oxygen pressure is maintained. In this way, films of different thickness (10 uc and 20 uc) of LAO are deposited while keeping the thickness (20 nm) of LSMO layers constant as shown in Figure 6.3.

For patterning, a thin film of novolack based image reversal resist (AR-U4060) is deposited by spin coating as described in Section 4.2. Here the photoresist is used for negative process. The LSMO layer was patterned by wet etching. We used 2.6 M of citric acid solution to etch the LSMO layer. The etching was done at 55 °C for 10 min bearing in mind 2.5 nm/min etching rate for LSMO layer at this temperature. After removing the photoresist by N-Ethylpyrrolidone at 60 °C for 3 hours, again the photoresist is deposited for the next nega-

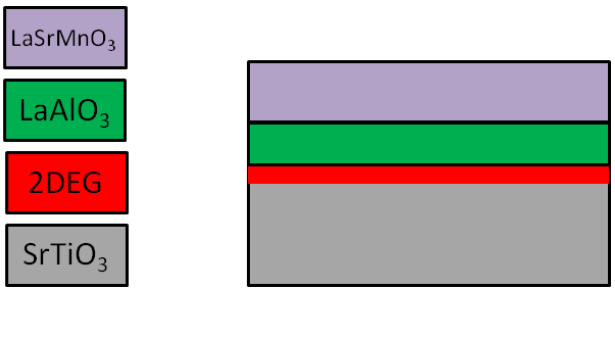

Figure 6.3: Illustration of LAO and subsequently LSMO layers grown by PLD on TiO_2-terminated STO (001) substrates.

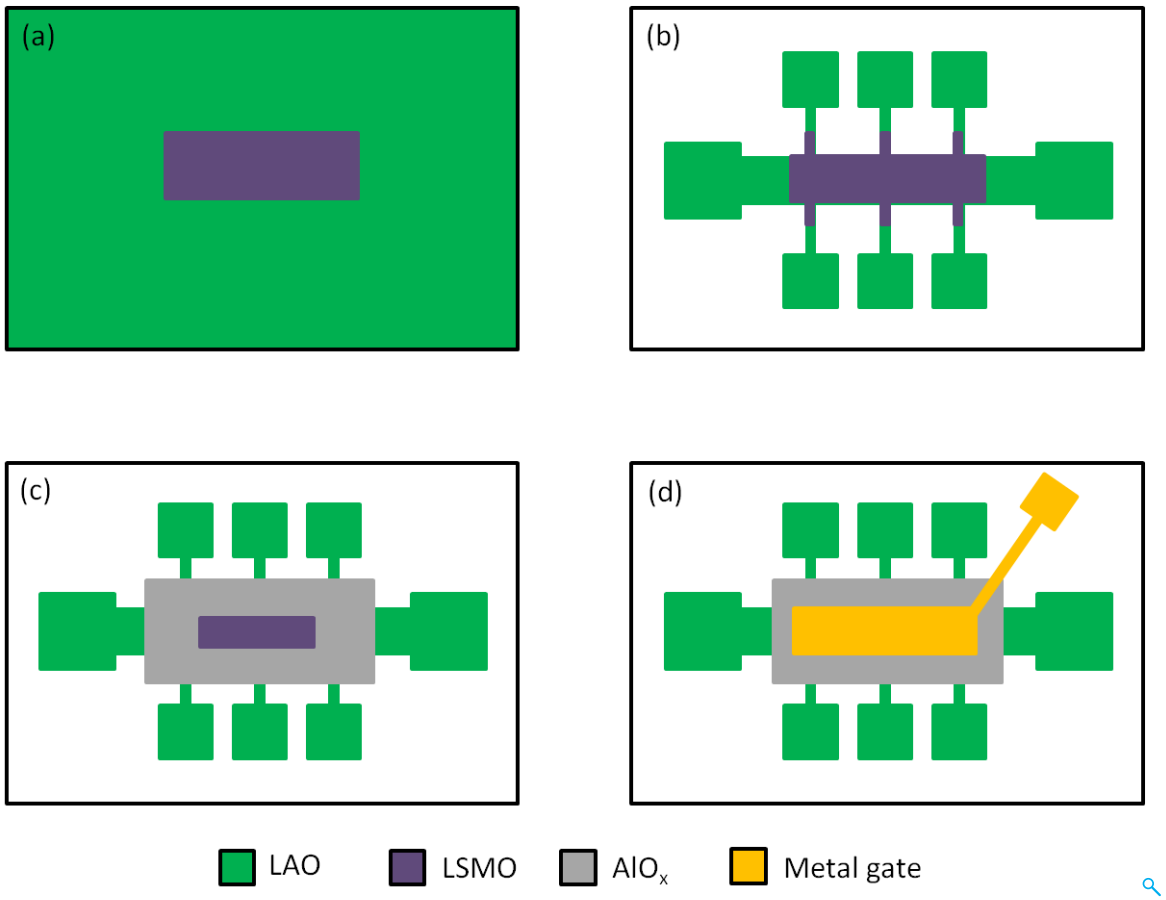

Figure 6.4: Top view of the patterned sample. (a) LSMO is patterned by wet etching with acidic solution. (b) In the second step LAO is patterned by reactive ion etching (RIE). (c) AlO_x layer is deposited by evaporation. (d) Finally metal gate is deposited by evaporation.

tive process by spin coating. Subsequently, the sample is exposed by photolithography. The exposed pattern consists of Hall bars with dimensions (length = 600 μm and width = 200 μm) including large area bond pads. The sample is developed using photolithographic developer solution (AR-300-26, we have used the developer in dilution of 1:4). After development, reactive ion etching is performed in an inductively coupled plasma reactive ion etching system (ICP-RIE, Oxford Plasmalab 100) using a BCl_3-based etching process to completely remove the LAO layer (for more detail see Section 4.2.2). After etching, the resist is removed using N-Ethylpyrrolidone at 60 °C for 3 hours. In the third step the photoresist (AR-U4060) is deposited by spin coating, now for positive process. After exposure and development a 100 nm AlO_x blanket is deposited by e-beam evaporator and lift-off is done. The previous step is repeated for the deposition of top metal gate Pt/Au 10/100 nm by e-beam evaporator, and finally lift-off is done. The top view of the patterned sample including all patterning steps can be seen in Figure 6.4. The Hall bars and metal gate are bonded using Al wire for electrical transport measurements.

Electrical characterization

After patterning and bonding the samples, electrical transport measurements are carried out in the same setup as described in Section 6.2.1. During the measurement, we have realized that there is no insulation between different Hall bars. The reason is not clearly understood. One possibility is that during the wet etching, we could not remove LSMO layer properly which later on, affected the reactive ion etching and as a result we did not have properly patterned hall bars. This short circuit between different Hall bars may be avoided by optimizing the wet etching parameters.

6.2.3 Patterning by sequential deposition of LAO layers

A sequence of thin crystalline LAO, patterned amorphous LAO and crystalline LAO were used to achieve lateral insulation and patterning of conducting areas [105] as described in Section 4.1.1. Here we investigated similar processes, but reduced the process steps using the following deposition method.

First, the Hall bars are patterned by using image reversal resist (AR-U4060) on the STO (001) substrates. Then amorphous 10 nm LAO is deposited by PLD on the patterned sample at room temperature. Oxygen is used as a background gas at a pressure of 10^{-3} mbar during deposition. During deposition, Laser fluence and pulse frequency are kept at 2 J/cm^2 and 2 Hz, respectively. After lift-off, the sample is ex-situ annealed in the Tube oven at 800 °C for 1 hour with the continuous Oxygen flow. The ex-situ annealing step renders the a-LAO/STO

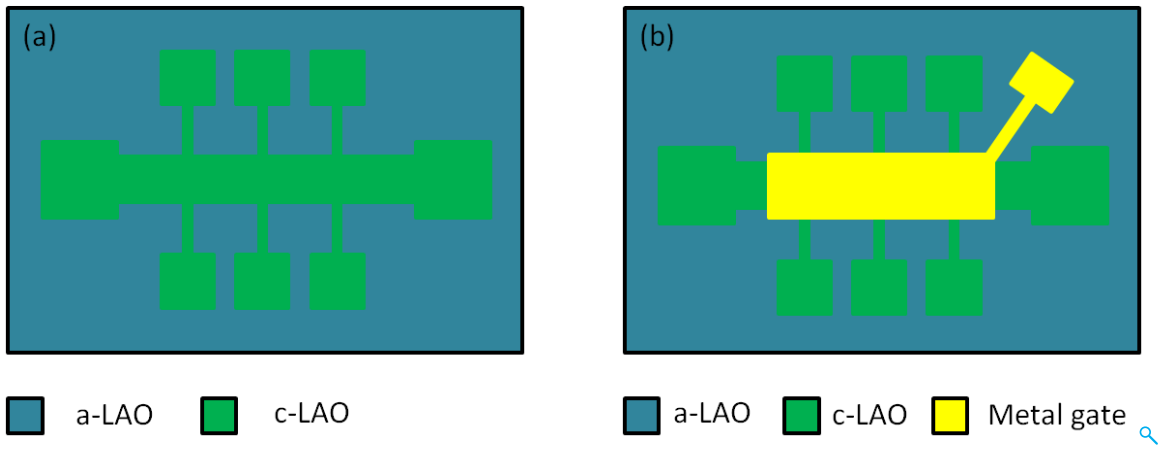

Figure 6.5: Top view of the patterned sample. (a) Patterning of LAO Hall bar is done by deposition of amorphous 10 nm LAO layer on STO substrate. (b) Metal gate on top of Hall bar.

areas fully insulating. Then crystalline LAO layer is deposited at 850 °C using Laser fluence, pulse frequency and Oxygen pressure 2 J/cm^2, 2 Hz and 10^{-3} mbar respectively. After deposition, the sample was cooled down without performing extra annealing step. We deposited different samples by varying the thickness (10 uc and 12 uc) of LAO. The photolithography step is done to define the top-gate structure and subsequently top metal gate Pt/Au 10/100 nm is deposited by e-beam evaporation and lift-off is done as shown in the Figure 6.5. The Hall bars and metal gate are bonded using Al wire for electrical transport measurements. The bonds are placed directly on the LAO without additional metallization.

Electrical characterization

Electrical transport measurements are carried out at low as well as at room temperature. The sheet resistance of the Hall bars is approximately $8\,k\Omega/\square$ at room temperature, and $0.20\,k\Omega/\square$ at 4.2 K. The area between the structures is insulating at room temperature as well as at low temperature having resistance in the range of GΩ.

In order to observe the gating effect, we swept the drain-source voltage from -1V to +1V and measured the drain-source current by applying constant gate-source voltages. During the measurements, we realized that when the devices were turned on, the gate leakage current I_G was always significantly smaller than the drain current I_D. I/V characteristics at $T = 4.2\,K$ are shown in the Figure 6.6. The DS channel is conducting. As expected for n-type channels, positive (negative) voltages applied to the gate increase (decrease) I_{DS} as shown in the Figure 6.6. We applied V_{GS} from -0.8 V to 1.1 V and obtained current gain of approximately 5% as

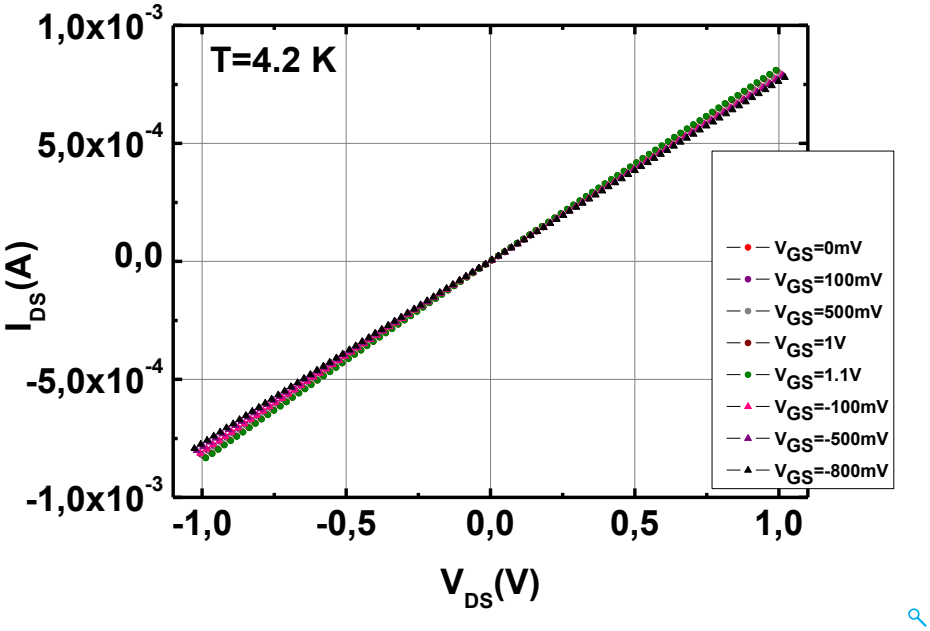

Figure 6.6: I_{DS} (V_{DS}) curves of the 10 uc of LAO Hall bar structure with top-gate, the gate-voltage is varied from -0.8V to +1.1V. Measurements are done at 4.2 K.

shown in the Figure 6.6.

For this sample we tried to measure gating effect at room temperature, but at room temperature the I_G was high and comparable to I_D, so it was not possible to measure the gating effect at room temperature.

6.3 Summary

In this chapter, the possibility of using oxides materials as a field effect devices has been explained.

We used the top-gating technique and fabricated field effect devices. The LAO/STO heterostructures are patterned by RIE and then top metal gate is deposited by e-beam evaporator. In these samples, during the measurement, we realized that the gate leakage current I_G (in the range of 10^{-6} A at room temperature and 10^{-5} A at 4.2 K) was significantly big and comparable to drain source current I_{DS}. The possible explanation of this high gate leakage current could be that the metal gate directly sees the 2DEG at the LAO/STO interface. To improve the gate action some sample were also prepared by adding an extra conducting oxide (LSMO) layer on LAO/STO heterostructures. For these samples, there was no good insulation between the different Hall bars after patterning, the possible reason could be that

LSMO was not completely removed by wet etching as a result Hall bars were not properly patterned. The sample which was patterned by sequential deposition of LAO layers showed gating effect at 4.2 K, approximately 5% of current gain was obtained by applying V_{GS} from -0.8 V to 1.1 V. At room temperature the I_G was high and comparable to I_D.

Chapter 7

Summary and Outlook

The LAO/STO interface has been thoroughly studied in this thesis. The main aim was to deposit high quality LAO thin films, develop a nanopatterning technique to pattern the LAO/STO interface, explore the transport properties in the nanostructures and to investigate field effect devices by using a top metal gate.

After optimization of the PLD process, high quality LAO/STO layers were obtained. Structural and stoichiometric quality of the deposited films were characterized by X-ray diffraction (XRD) and transmission electron microscopy (TEM). Reciprocal space map (RSM) around asymmetric +103 Bragg reflections indicated that all films were fully strained. Transmission electron microscopy (TEM) measurements revealed that high quality and defect free LAO/STO interfaces could be achieved by using high (10^{-3} mbar) background oxygen pressure.

We have successfully patterned the LAO/STO interface in nano-meter scale, using a direct nanopatterning technique that was developed during the course of this thesis. This technique uses e-beam lithography in combination with (BCl_3-based) reactive ion etching (RIE), and allows patterning nanostructures down to 100 nm. The process leaves the substrate insulating and preserves the conductivity of the electron gas, except for a narrow depletion region. This depletion region is attributed to the plasma etching process. The width of the depletion region is approximately 20 ± 3 nm on each side of the structure for all temperatures. The depletion region is less conductive and its conductivity is temperature dependent, which is in good agreement with traps introduced by the etching process.

The carrier density (n_s) and carrier mobility (μ) in these nanostructured samples were calculated by Hall measurements. The carrier density is in the range $n_s \approx 10^{13}$ cm^{-2} for all structures at all temperatures, which is in good agreement with the literature values. The mobilities are in the range of ≈ 500 cm^{2}V^{-1}s^{-1} and ≈ 5 cm^{2}V^{-1}s^{-1} at 4.2 K and 300 K re-

spectively. These values are smaller than those reported in literature. These differences may be attributed to sidewall depletion, because the depletion region is less conductive as compared to the central region and the mobility values are the average of central and depletion region of the structures.

After successful nanopatterning, the next goal was to study the correlation between the LAO/STO interface conductivity and the local structure of the STO substrate. STO undergoes cubic to tetragonal structural transition at T=105 K. This structural transition leads to the formation of domains within STO. These domains modulate the conductivity of LAO/STO interface and the current is no more homogeneous within the domains, rather it flows in filaments at the boundaries of the domains. The filaments are formed by the migration of charges towards the domain boundaries and may be accompanied by the pinning of defects at the domain walls, leaving the domain area basically insulating. We identified this effect in the nanostructures during the transport measurements.

During the temperature dependent resistance measurement in nanostructures, the current filaments are ruptured due to structural transition of STO and massive peaks in resistance are seen during the warm-up cycle. We observed this effect for nanostructures having width less than 500 nm. For some of the nanostructures (100 nm), the resistance increases above the room temperature value or even beyond the measurement limit. The peak height depends on the minimum temperature of the cool-down (from where the warm-up cycle was started). It increases when the minimum temperature is decreased and when the minimum temperature approaches the temperature of the resistance peak, the effect vanishes completely.

The effect is observed in nanostructures, because in these structures the current is limited to one or at least a few filaments. On the other hand, large area samples have large number of current filaments due to their lateral size. Therefore, the breaking of single or few filaments have greater effect on the conductivity of nanostructures than that of large area samples.

We have confirmed the basic nature of the observation by pattering the nanostructures by an amorphous LAO hard mask method. Also, for these samples, we obtained a pronounced peak, confirming that the lateral size restriction was relevant factor for increase in resistance. The effect can be observed when the transport properties of LAO/STO nanostructures are investigated above and below the structural transition temperature.

We have tried to develop field effect devices using a top metal gate, but these attempts did not yield desired results. The LAO/STO heterostructures were patterned by RIE and then top metal gate was deposited by e-beam evaporator. In these samples, during the measurement at 4.2 K, we realized that the gate leakage current I_G (in the range of 10^{-5} A) was significantly large and comparable to drain source current I_{DS}, similar behavior was observed during the

room temperature measurement.

The sample which was patterned by sequential deposition of LAO layers showed a gating effect at 4.2 K. Approximately a 5% of current gain was obtained by applying V_{GS} from -0.8 V to 1.1 V. However, at room temperature I_G was high and comparable to I_{DS}.

Our findings suggest further optimization of the technique in order to minimize sidewall depletion width and also to reduce the lateral size of the nanostructures. The filamentary current in LAO/STO nanostructures due to domains at low temperature has opened a new dimension for exploring the underlying physics of LAO/STO interface. It is vital to explore it before employing this interface into devices. For field effect devices, the high gate leakage current may be minimized by deposition of an AlO_x layer in high oxygen pressure. For samples which were patterned by sequential deposition of LAO layers, an additional annealing step may be included during cooling in PLD to improve the sample quality and to minimize the gate leakage current. Another possibility could be to use different top-gate metal.

In conclusion, the experimental work presented in this thesis has deepened the knowledge about the LAO/STO interface.

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Journals and Conference contributions

1. M. Z. Minhas, A. Müller, F. Heyroth, H. H. Blaschek, and G. Schmidt, "Temperature dependent giant resistance anomaly in $LaAlO_3/SrTiO_3$ nanostructures", (arXiv: 1610.07382).

2. A. Müller, M. Z. Minhas, H. H. Blaschek, B. Fuhrmann, and G. Schmidt, "A nano sized field effect transistor based on a complex oxide lateral heterostructure", (under preparation).

3. M. Z. Minhas, H. H. Blaschek, F. Heyroth, and G. Schmidt, "Sidewall depletion in nano-patterned LAO/STO heterostructures", AIP Advances **6**, 035002 (2016).

4. M. Z. Minhas, H. H. Blaschek, F. Heyroth, and G. Schmidt, "An industry compatible low-damage nano-patterning process for LAO/STO heterostructures", Talk, In DPG Spring conference, Berlin, Germany (2015).

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Hiermit erkläre ich an Eides statt, dass ich die Arbeit selbständig und ohne fremde Hilfe verfasst, keine anderen als die von mir angegebenen Quellen und Hilfsmittel benutzt und die den benutzten Werken wörtlich oder inhaltlich entnommenen Stellen als solche kenntlich gemacht habe.
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