Silicon Nanowires: Synthesis, Fundamental Issues, and a First Device

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Preface

The purpose of this thesis is to illuminate several aspects regarding the synthesis of silicon nanowires, their electrical properties, and the fabrication of a first device made thereof. Following an introductory survey of important results in silicon nanowire research, Chapter 1 deals with silicon nanowire growth from an experimental point of view. After a detailed description of the experimental setup, the wafer preparation, and the growth procedure, experimental results concerning the epitaxial growth of silicon nanowires with gold are presented. Gold is presently the standard catalyst material for silicon nanowire growth. Yet, serious concerns exist, whether silicon nanowires grown with gold as catalyst can ever become compatible with existing electronics fabrication technology. Therefore, replacing gold by an alternative catalyst material is of great importance. In the second half of Chapter 1 we present silicon nanowire growth results using different catalyst materials: palladium, iron, dysprosium, bismuth, indium, and aluminum.

The three chapters following thereupon each addresses a fundamental silicon nanowire growth issue. Chapter 2 is devoted to the diameter dependence of the silicon nanowire growth velocity. Since the silicon nanowire length is usually controlled by adjusting the growth time, a knowledge of the factors that determine the growth velocity is crucial. Concerning the diameter dependence of the growth velocity, seemingly contradictory observations were made by different groups. Considering the steady state supersaturation of the catalyst droplet we will derive a model that conclusively explains the differences in the observed behavior. Furthermore, our model links the pressure dependence of the growth velocity to the diameter dependence of the growth velocity; an insight that might be useful for an optimization of the growth conditions. Focus of Chapter 3 is on the diameter increase at the nanowire base that can be observed for nanowires grown via the vapor-liquid-solid mechanism on a solid substrate. An explanation for this phenomenon is given in terms of a model that takes the shape of the catalyst droplet into account. In addition, the influence of the line tension on the nanowire morphology is discussed. Chapter 4 deals with the crystallographic growth direction of silicon nanowires, a parameter that is of great importance especially in view of the technical applicability of epitaxially grown silicon nanowires. Experimental results presented in this chapter indicate a diameter-dependent change of the growth direction. We will propose a possible explanation for this growth direction change by taking the interplay of the surface and interface tensions of silicon nanowires into account.

After these partially theoretical considerations with regard to the nanowire morphol-

ogy, the electrical properties of silicon nanowires will be subject of Chapter 5. In the beginning of this chapter we will derive a model for the dependence of the charge carrier density of a silicon nanowire on the density of interface traps and interface charges located at the Si/SiO_2 interface. Subsequently, temperature-dependent electrical measurements of both p-doped and n-doped silicon nanowires are presented and discussed in detail. It will be seen that indeed the influence of interface traps and interface charges on the electrical properties can not be neglected. To some degree, the electrical characterization described in Chapter 5 may be seen as a preparatory work for Chapter 6. Having electronic applications of silicon nanowires in mind, the fabrication of a silicon nanowire field-effect transistor is naturally the first step. In this context, epitaxially grown silicon nanowires offer the decisive advantage that, owing to the vertical arrangement of the nanowires, a transistor gate can be wrapped around the silicon nanowire. In Chapter 6 we will present a process flow for the fabrication of an array of vertical surround-gate field-effect transistors out of epitaxially grown silicon nanowires. The feasibility of the fabrication process and the basic functionality of the devices is at last demonstrated by an electrical characterization of such an array of silicon nanowire surround-gate field-effect transistors.

For the convenience of the reader, magnified versions of all graphs are reproduced in the appendix.

Contents

Introduction and Survey

Recently, silicon nanowires experienced a considerable increase in attention, with the number of publications in this field doubling about every two years. This renewed interest in silicon nanowires is so much the more a noteworthy fact as the first report on artificial silicon fiber growth by Treuting and Arnold [Tre57] dates back to almost five decades ago. Moreover it is most remarkable that their result concerning the crystallographic growth direction of the silicon filamentary crystals, called whiskers at that time, is still valid, even for most of the silicon nanowires synthesized nowadays. However, before going deeper into the subject, it shall be plainly stated here that a silicon wire is defined as a rod-like silicon structure having a length that considerably exceeds its diameter. Silicon wires with diameters in the nanometer range will be referred to as silicon nanowires. These definitions, though not applied too strictly, will be adopted throughout this thesis.

In the early years of silicon wire research, the growth mechanism leading to the unidirectional silicon wire growth was still under discussion, when in 1964, R. S. Wagner and W. C. Ellis [Wag64a] in a pioneering publication proposed the vapor-liquid-solid (VLS) mechanism of crystal growth. At least for the growth of silicon wires and nanowires, where it is still the most prominent synthesis technique, the validity of the vapor-liquid-solid growth mechanism is widely accepted. The validity range of the vapor-liquid-solid mechanism is astonishingly broad, as wires with diameters from a few nanometers up to a few hundred micrometers can be synthesized via the vapor-liquid-solid growth mechanism. Although this mechanism applies to a much broader range of synthesis methods, it will be discussed exemplarily on the basis of the chemical vapor deposition of silicon wires using silane as precursor gas and gold as catalyst.

I.1 Vapor-Liquid-Solid Growth Mechanism

It has been observed experimentally, that the addition of a catalyst metal, like gold for example, strongly enhances the growth of silicon wires. As schematically shown in Fig.I.1(a), silicon wires grown with the help of gold usually exhibit a Au/Si alloy particle at their tip, and it is this Au/Si alloy particle that plays the central part in the model of Wagner and Ellis. The Au/Si phase diagram, displayed in Fig. I.1(b), is of the simple eutectic type; dominated by a low temperature eutectic point at 363 °C [Mas90a]. Hence at temperatures above the eutectic temperature the Au/Si alloy particle transforms into a liquid droplet of a composition that approximately corresponds to the silicon rich branch of the Au/Si phase

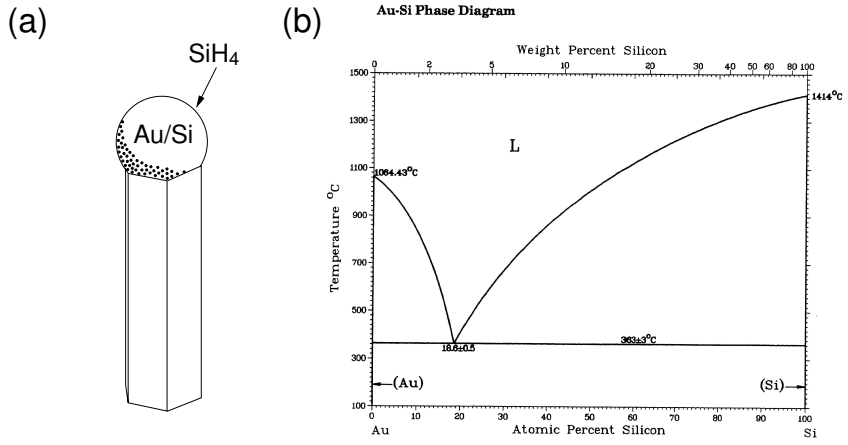

Figure I.1: (a) Schematic depicting the vapor-liquid-solid nanowire growth. (b) Au-Si phase diagram [Mas90a], see also Fig. A.1.

diagram, shown in Fig. I.1(b). During growth, silicon is supplied via the gaseous silicon precursor, silane. The silane molecules from the vapor phase are adsorbed on the droplet surface and cracked into silicon and hydrogen [Hog36].

$$\mathrm{SiH_4} \rightarrow \mathrm{Si} + 2\ \mathrm{H_2}\ . \tag{I.1}$$

After the incorporation of the silicon atoms, resulting from the chemical reaction at the droplet surface, the silicon atoms diffuse through the droplet to the liquid-solid interface, separating the metal alloy droplet from the silicon wire. Under growth conditions, the silicon concentration in the droplet is higher than the equilibrium concentration at this temperature, which is equivalent to a silicon chemical potential in the liquid μ^l that exceeds the chemical potential of the silicon nanowire μ^s. The droplet is then said to be supersaturated, where

$$\Delta\mu = \mu^l - \mu^s\ . \tag{I.1}$$

defines the silicon supersaturation $\Delta\mu$ [Giv87a]. The supersaturation of the Au/Si alloy droplet represents the driving force for the growth of the silicon wire.

Thus the vapor-liquid-solid mechanism of silicon wire growth basically consists of three steps: first, the adsorption and cracking of the gaseous silicon precursor, providing atomic silicon for the growth, followed by the incorporation of silicon atoms into the droplet; second, the diffusion of the silicon atoms through the droplet; and third, the condensation of silicon onto the silicon wire at the liquid-solid interface. The question, which of these three steps effectively determines the silicon wire growth rate was controversially discussed. It was only agreed upon that the diffusion step can not be rate determining, since the diffusion through the liquid alloy droplet is simply too fast [Giv87b]. Concerning the other two steps, Bootsma and Gassen [Boo71] favored step one, whereas Givargizov [Giv87b] took the opinion that the condensation of silicon onto the nanowire at the liquid-silicon interface is rate determining. Concerning this discussion, it must however be clear

that under steady state growth conditions the incorporation rate has to equal the condensation rate, which requires some kind of interaction between both processes. Thus they can not be dealt as independent processes, and a discussion whether in general one step or the other is rate determining over-simplifies the problem. A general description, therefore, has to consider both processes, such that a situation where in fact one process is rate determining can be discussed as a special limit of the general solution.

One somehow related issue in this context is the radius dependence of the growth velocity. Considering the surface contribution of the energy of the droplet, the chemical potential of the silicon wire is rendered by an additional radius-dependent term. This is usually referred to as the Gibbs-Thomson effect. As a consequence, also the supersaturation of the droplet, defined in equation (I.1), becomes radius-dependent. Since the supersaturation is the driving force for the silicon wire growth, this implies a radius dependence of the growth velocity. However, here things start to become more complex, as some silicon wire growth experiments indicate an increase of the growth velocity with increasing wire radius [Giv75], whereas others [Wey78, Neb05] show a decrease of the growth velocity with increasing radius. How this riddle can be solved will be subject of Chapter 2, where we present a model considering the interplay of the incorporation and the condensation step under steady state conditions. We will see that both steps can not be dealt independently of each other, and that it is indeed the interplay of both steps that determines the growth velocity.

In the vapor-liquid-solid growth mechanism, the properties of the droplet surface play an important role for the unidirectionality of the silicon wire growth. In general, the droplet surface is assumed to be ideally rough, such that all the impinging vapor molecules are captured. At least for silane as vapor phase silicon source, the adsorption and cracking efficiency of the Au/Si droplet surface is significantly higher than the adsorption and cracking efficiency of the pure silicon surface. This important property of the droplet surface, i.e. the high adsorption and cracking efficiency, is usually referred to as the catalytic ability of the Au/Si droplet. However, as pointed out by Givargizov [Giv87b], speaking of catalytic ability is somehow misleading in this context, as it does not imply a catalysis of the silane reaction in a chemical sense. The so-called catalytic ability of the droplet more relates to the high sticking coefficient of the droplet with respect to the precursor gas [Wag65]. By measuring the axial and radial wire growth rates, Bootsma and Gassen [Boo71] could determine that under their growth conditions, the adsorption and cracking efficiency of the droplet is roughly three orders of magnitude higher than the corresponding efficiency of the silicon surface. To conclude, the high adsorption and cracking efficiency of the Au/Si droplet surface, compared to the corresponding efficiency of the silicon surface, leads to the growth of silicon wires with almost constant radius.

Taking wire growth via the vapor-liquid-solid mechanism into account, it becomes immediately clear that the radius r of the wire is directly related to the radius R of the droplet. Considering the situation where a droplet in thermal equilibrium is sitting on top of a cylindrical silicon rod, additionally assuming a flat interface, the radius r of the wire

is determined by the droplet radius R

$$r = R\sqrt{1 - \left(\frac{\sigma_{ls}}{\sigma_l}\right)^2} \qquad \text{[Neb03]}. \tag{I.1}$$

Here σ_{ls} and σ_l denote the liquid-solid interface tension and the liquid surface tension σ_l of the droplet. Thus the radius of the Au/Si catalyst droplet is larger than the radius of the wire, which was taken to be constant for now. This however, does not hold for the initial growth stage of silicon wires, grown epitaxially on a silicon substrate. They exhibit a strong expansion in the region where the wire is attached to the substrate (see e.g. [Wag67]). As pointed out by Givargizov [Giv87c], this expansion, however, is not related to an overgrowth of the silicon wire caused by a direct deposition of silicon atoms on the nanowire flanks. As discussed in detail in Chapter 3, this phenomenon can be explained by a change of the droplet shape in the initial growth stage [Shc90, Neb96, Sch05c].

Silicon wires synthesized using gold as catalyst are in general single crystalline, although sometimes crystallographic defects like stacking faults or dislocations are observed [Wag67]. Experimental results indicate that the crystallographic growth direction of silicon nanowires grown with gold is diameter dependent [Wu04a, Sch05a]. For large diameters, greater than about 50 nm, the nanowires tend to grow in a $<111>$ direction. This is, by the way, the most often reported silicon wire growth direction. In addition to the $<111>$ direction also the $<110>$ and $<112>$ growth directions are observed, especially for diameters smaller than about 50 nm. The diameter dependence of the growth direction is discussed in detail in Chapter 4, where also a model for this direction change is proposed.

I.2 Growth Methods and Catalyst Materials

Several methods for the synthesis of silicon nanowires have been established in the last fifty years. These methods mainly differ with respect to the catalyst material used and with respect to the means by which the silicon is supplied. Concerning the silicon supply, the most popular method seems to be the chemical vapor deposition (CVD) using a gaseous silicon precursor like silane, SiH_4 [Boo71, Wes97a, Wes97b], silicon tetrachloride, $SiCl_4$ [Wag64a, Giv71, Hoc05], or silicon diiodide, SiI_2 [Gre61, Wag61]. Also disilane, Si_2H_6 [Han06], is sometimes used; especially if low pressure growth conditions are desired. In order to enhance the effectiveness of the chemical vapor deposition at low temperatures for example, a plasma might be used to pre-crack the silicon precursor and to facilitate thereby the growth of the silicon nanowires [Hof03, Zen03]. Also strong electric fields were shown to influence the growth of silicon nanowires [Che03, Eng05]. Another prominent synthesis approach is based on the thermal evaporation of silicon monoxide, SiO. At elevated temperatures SiO decomposes at the silicon nanowire tip into Si and SiO_2, leading to the formation of silicon nanowires that are usually covered by a thick silicon oxide shell. Concerning silicon nanowire growth via SiO decomposition, both growth via the vapor-liquid-solid mechanism [Kol04] as well as catalyst-free growth [Zha99] has been reported in literature. Other silicon nanowire synthesis methods mostly rely on the direct

evaporation of silicon. This can either be achieved with the help of a molecular beam epitaxy (MBE) system [Sch04, Fuh05], by simple thermal evaporation [Fen00], or by means of laser ablation [Mor98, Bar02].

Regarding the catalyst materials, a large number of different materials has been tested for their ability to catalyze silicon wire growth. Figure I.2 displays a table of the elements that have been tested so far, giving also the corresponding literature references. The elements in green framed boxes are reported to promote silicon wire growth, whereas the elements in red framed boxes have been tested unsuccessfully. Concerning the elements in blue framed boxes, the reports in literature are somewhat controversal.

Be											B	C [Wag64b]	N	O
Mg [Wag64b]											Al [Osa79] [Neb03]	Si	P	S
Ca	Sc	Ti [Kam00] [Kam01]	V	Cr	Mn [Wag64b]	Fe [Mor98] [Fen00] [Bar02] [Wan98] [Sch05b]	Co	Ni [Wag65] [Giv75] [Tat81] [Wan98] [Neb05]	Cu [Wag65] [Wag64b] [Boo71] [Neb03] [Neb05]	Zn [Miy76] [Yu00] [Chu00] [Neb03] [Neb05]	Ga [Giv71] [Sun01] [Sha04] [Neb03]	Ge [Wag64b]	As	Se
Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd [Wag64a] [Wag64b] [Boo71] [Giv75] [Neb03]	Ag [Wag65] [Wag64b] [Tat78] [Tat79] [Neb05]	Cd [Wag64b]	In [Giv71] [Miy76] [Boo71] [Neb03]	Sn [Wag64b] [Boo71] [Neb03]	Sb [Neb03]	Te [Miy76]
Ba	La	Hf	Ta	W	Re	Os [Wag64b]	Ir	Pt [Wag65] [Giv75] [Wey78] [Neb03] [Neb05]	Au [Wag64a] ...	Hg	Tl	Pb [Miy76] [Neb03]	Bi [Miy76] [Boo71] [Neb03]	Po
		Ce	Pr	Nd	Pm	Sm	Eu	Gd [Wag64b]	Tb	Dy [Sch05b]	Ho	Er	Tm	Yb

Figure I.2: Table of elements tested with regard to their ability of catalyzing silicon nanowire growth; green box: successful, red boxes: unsuccessful, blue boxes: controversal reports

Besides gold, the first elements that were reported as catalyst materials for silicon wire growth are the elements nickel, copper, palladium, silver, and platinum [Wag64a]. The resulting silicon wires, synthesized at temperatures between 850 °C and 1050 °C in a CVD process using $SiCl_4$, show large similarities with the wires obtained with gold as catalyst. They are almost constant in diameter and exhibit a globular catalyst particle at their tip. In addition, they are single crystalline and mostly <111> oriented. The main disadvantage of these catalysts is, however, that a low temperature vapor-liquid-solid growth, like in case of gold, is not possible for the above mentioned metals. The melting points of the corresponding metal/Si alloys are in all cases above 800 °C.

Other possible catalyst materials for the chemical vapor deposition of silicon nanowires are the group III elements indium and gallium. The Ga/Si and In/Si phase diagrams are very similar. Both are of the simple eutectic type, with a eutectic point at very low temper-

atures of $30\,^{\circ}$C and $157\,^{\circ}$C, respectively. So from this point of view it is not too astonishing that silicon nanowire growth experiments using gallium or indium as catalyst provide similar results [Giv71]. Although a vapor-liquid-solid growth of silicon nanowires using gallium or indium is possible, it appears to be more difficult than for nickel, copper, or the precious metals. Moreover, the wires grown at high temperatures using gallium and indium are strongly tapered [Giv71]. This might be related to the loss of the catalyst material during growth, either by incorporation of the catalyst material into the silicon wire or by loss through a volatile reaction product. Another explanation for the tapering is provided by Nebolsin et al. [Neb03]. According to their model, a stable vapor-liquid-solid growth of nanowires having a constant diameter requires that the surface tension of the liquid droplet, σ_l, is greater than $\sigma_s/\sqrt{2}$; with σ_s being the silicon surface tension. This criterion for the growth of cylindrical silicon nanowires is not met by gallium and indium, which might be a possible explanation for the tapering of the wires. A different route for the synthesis of silicon nanowires using gallium as catalyst was followed by Sunkara et al. [Sun01], who demonstrated the synthesis of polycrystalline silicon nanowires by a plasma enhanced chemical vapor deposition (PECVD) process. To this end, 700 W of microwave power and a substrate temperature around $450\,^{\circ}$C were applied to a gallium covered silicon substrate in hydrogen atmosphere. With the help of the hydrogen plasma, volatile silicon compounds were produced, which served as vapor phase source for the growth of the silicon nanowires. Silicon nanowires of higher crystalline quality were produced in a similar PECVD process by Sharma et al. [Sha04] at slightly higher temperatures ($550\,^{\circ}$C), with the only difference that silane was used as vapor phase silicon source.

Similar to gallium and indium, the Zn/Si phase diagram exhibits a single eutectic point at moderate temperature ($420\,^{\circ}$C). According to Yu et al. [Yu00], who report on silicon nanowire growth with zinc as catalyst, a vapor-liquid-solid growth using diluted silane (5% in Ar) is possible at temperatures between $450\,^{\circ}$C and $500\,^{\circ}$C. Silicon nanowires with diameters down to $10\,$nm could be produced this way. They found two types of nanowires: $<111>$ and $<112>$ oriented ones, both of them single crystalline, with few crystallographic defects.

One of the most promising elements for vapor-liquid-solid silicon nanowire growth seems to be aluminum. The Al/Si phase diagram shows the closest similarities with the Au/Si phase diagram. It exhibits a single eutectic point at a temperature and a silicon concentration comparable to the eutectic point of the Au/Si phase diagram. However, only little is reported on the growth of silicon nanowires with the help of aluminum. Our own results, presented in Section 1.5 indicate that silicon nanowires grown with the help of aluminum tend to be stronger facetted and tapered than nanowires grown with gold as catalyst. However, recent results show that the tapering of the wire can be strongly reduced by optimizing the growth parameters. The resulting wires obtained with aluminum as catalyst are in general single crystalline with few crystallographic defects.

An element which seems to work well, though at extremely high temperatures, is iron. The lowest melting point of the Fe/Si phase diagram is at $1207\,^{\circ}$C, and correspondingly high temperatures have to be applied for a vapor-liquid-solid silicon nanowire growth.

Morales et al. [Mor98] first demonstrated the laser assisted synthesis of silicon nanowires with iron as catalyst. With the help of a frequency doubled Nd:YAG laser they ablated silicon and iron from a Si:Fe (9:1) target mounted in a quartz oven that was heated to 1200 °C and filled with 0.5 bar of argon. Owing to the high argon background pressure, the ablated iron and silicon atoms could collide and react in the vapor phase, which then led to the growth of single crystalline, <111> oriented silicon nanowires. Similar results were obtained by Feng et al. [Fen00] by simply heating a Si:Fe (19:1) target at 1200 °C for twenty hours in an argon filled quartz oven. As presented in Section 1.5, iron can also be used for silicon nanowire growth at temperatures far below the melting point of the alloy, although the crystalline quality of the nanowires obtained that way is poor [Sch05b]. It seems probable that in this case, a solid iron silicide particle is responsible for the nanowire nucleation. Thus growth would proceed via a vapor-solid-solid mechanism. Such a vapor-solid-solid growth of silicon nanowires can also be observed if titanium [Kam00] or dysprosium [Sch05b] are used instead of iron, and growth temperatures below the melting point of the corresponding alloy are applied.

The group IV and V elements germanium, tin, lead, and bismuth do not seem to promote silicon nanowire growth [Neb03, Boo71], although Miyamoto [Miy76] reports on the growth of amorphous silicon nanowires using bismuth and lead. Concerning the remaining elements magnesium, manganese, gadolinium, osmium, and tellurium only little information is available [Wag64b, Miy76]. It is reported that, with the exception of magnesium, the latter elements do promote silicon nanowire growth [Wag64b, Miy76].

I.3 Silicon Nanowire Heterostructures

Semiconductor heterostructures in general offer interesting perspectives for electronic and optoelectronic devices. For two reasons semiconductor nanowires are very attractive for this aim. The first is that semiconductor nanowires offer the possibility of epitaxially combining materials with a large lattice misfit. If two bulk materials having a lattice misfit are brought together in the form of a thin film of one of the materials on top of the other, the strain in the material, caused by the lattice misfit at the heterojunction, is reduced by the creation of misfit dislocations if a certain critical layer thickness is exceeded. These dislocations have detrimental influence on the electrical and optical properties. However, a semiconductor nanowire of sufficiently small radius can react elastically to the stress caused by the lattice misfit, without producing dislocations [Ert03, Käs04]. The second advantage of semiconductor nanowires with respect to the synthesis of heterostructures is the intrinsic radial confinement of the charge carriers in the nanowire. Owing to this radial confinement, three-dimensional quantum dots can be produced in a relatively simple way. This has, for example, been demonstrated by Björk et al. [Bjö02] for an InAs/InP nanowire heterostructure. The electronic properties of this heterostructure have been calculated by Zervos et al. [Zer04].

With respect to silicon nanowire heterostructures, a combination of silicon with the other group IV semiconductor, germanium, seems to be the natural choice. Especially, as

a perfect Si/Ge superlattice offers the interesting perspective that the combined material might develop a direct band gap [Pre92]. However, there have only been few reports on axial Si/Ge heterostructure wires. Givargizov et al. demonstrated in an early work [Giv71] the synthesis of Si/Ge heterostructure wires produced by chemical vapor deposition using $SiCl_4$ and $GeCl_4$ as precursors. In a more recent work, Wu et al. [Wu02] were able to produce Si/SiGe heterostructure nanowires by a hybrid approach combining chemical vapor deposition with pulsed laser deposition. In their experiments, $SiCl_4$ was used as gaseous silicon source. The germanium was supplied by ablating a germanium target using a pulsed Nd:YAG laser.

Also radial heterostructures offer interesting opportunities, especially with regard to electronic applications. Covering a nanowire with a shell material, having a larger band gap, would confine the charge carriers to the core of the nanowire heterostructure. This might be an interesting route to reduce the surface scattering of the charge carriers, for example. In addition, the energetic alignment of different band gap materials might be used to alter the electronic properties of core and shell, and to circumvent this way the problem of doping.

The synthesis of epitaxial Si/Ge, Ge/Si, and Si/Ge/Si core-shell and core-multishell heterostructure nanowires, respectively, has been demonstrated by Lauhon et al. [Lau02]. In a first step they synthesized silicon or germanium nanowires via a CVD process using silane and germane as precursors and gold as catalyst. The shell material was subsequently deposited at temperatures below the Au/Si or Au/Ge eutectic point, and annealed afterwards. Their electrical characterization of a p-Si/i-Ge/SiO_x/p-Ge heterostructure revealed a promising performance characteristic, with a transconductance of $1.5\ \mu A\,V^{-1}$.

Aiming more at optoelectronic applications, Hayden et al. [Hay05] were able to produce a Si/CdSe core-shell heterostructure nanowire that functioned as a light emitting diode. For this purpose, single crystalline p-type silicon nanowires, grown in a CVD process using gold as catalyst were covered with an n-type polycrystalline CdSe shell by pulsed laser deposition. By separately contacting core and shell of a single nanowire and applying a voltage across the pn-junction, an electroluminescence signal with a peak at 528 nm could be produced.

I.4 Doping and Electrical Properties

One issue that has not been addressed so far is the question of wanted and unwanted impurities in silicon nanowires. As practically all semiconductor devices rely on a controlled doping of the semiconductor material, clearly, a both quantitatively and spatially controlled doping of the silicon nanowire is desirable. In principle, the vapor-liquid-solid growth mechanism offers two possible routes to dope silicon nanowires. The easiest way, at least from a technical point of view, is to vaccinate the Au/Si droplet with the dopant prior to growth, i.e. to grow the nanowires with a Au/Si/dopant mixture as catalyst. Cui et al. [Cui00] demonstrated silicon nanowire synthesis with the help of a 200:1 Au:P mixture. They electrically characterized the thereby obtained nanowires by placing sin-

gle nanowires on an oxidized silicon substrate and contacting them with the help of an e-beam lithography system. They performed two-terminal measurements on the contacted nanowires, additionally using the oxidized silicon substrate as a back-gate, by which they applied a gate voltage. Measuring the gate voltage dependence they were able to show that the phosphorus-doped silicon nanowires indeed behaved like highly n-doped silicon rods. The resistivity of heavily phosphorus-doped silicon nanowires was found to be as low as $0.023\,\Omega\,\mathrm{cm}$.

The more advanced alternative doping method is to add a small amount of a gaseous dopant precursor, like phosphine, PH_3, or diborane, B_2H_6, to the gaseous silicon precursor. This theoretically offers the possibility of varying the doping of the nanowires during growth, by changing the partial pressure of the corresponding dopant gas. However, sharp transitions between differently doped nanowire regions seem hard to achieve experimentally, since the Au/Si droplet might act as a reservoir for the dopant atoms. Cui et al. [Cui00] also characterized boron doped silicon nanowires that were grown by chemical vapor deposition using silane as silicon source and diborane as dopant gas. The SiH_4:B_2H_6 ratio was varied between 1000:1 and 2:1. The low doped silicon nanowires showed a resistivity of $390\,\Omega\,\mathrm{cm}$, whereas the silicon nanowire grown with a silane to diborane ratio of 2:1 exhibited almost metallic behavior with a resistivity of $0.007\,\Omega\,\mathrm{cm}$. From gate voltage dependend measurements they determined a carrier mobility of $3\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ for the heavily doped nanowires. Wu et al. [Wu04b] report a mobility of $325\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ for medium boron-doped nanowires, which is a mobility value comparable to that of bulk silicon. Zheng et al. [Zhe04] fabricated n-doped silicon nanowires doped with phosphine as the dopant source at a silane to phosphine ratio between 4000:1 and 500:1. The electrical characterization was performed as described before, by contacting a nanowire placed on an oxidized silicon substrate. Gate voltage dependent measurements revealed a mobility of $260\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ for the lightly and $95\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ for the heavily doped silicon nanowires, respectively. Nebolsin et al. [Neb95] determined the resistivity of silicon wires grown with gold, nickel, platinum, and copper as catalyst. For all four metals the resistivity at room temperature was found to be of the order of $10^3\,\Omega\,\mathrm{cm}$, which is about the value of intrinsic silicon. An electrical characterization of undoped silicon nanowires grown with gold and zinc as catalysts was performed by Chung et al. [Chu00] and Yu et al. [Yu00]. They found that both kinds of nanowires are p-type with a resistivity of $10^5\,\Omega\,\mathrm{cm}$ for the Zn-catalyzed and $> 10^3\,\Omega\,\mathrm{cm}$ for the Au-catalyzed wires. To conclude, the electrical measurements prove the possibility of doping silicon nanowires either using gaseous dopant precursors or by directly adding the dopant to the catalyst droplet prior to growth. The measured electrical properties are in overall compliance with the properties of bulk silicon.

Another important issue are unwanted impurities in the silicon nanowire caused by the presence of the catalyst droplet itself. Especially for gold this is critical as gold is known to create a very effective recombination center in silicon [Lan80]. Although this issue was first brought up more than 40 years ago [Tho66], the question how much gold is typically dissolved in the silicon nanowire, grown at low temperatures, has still not yet

been satisfactorily answered. As a comparison, the analysis of InAs nanowires using a local electrode atom probe microscope revealed an extremely high gold concentration of the order of 1×10^{18} cm^{-3} in the InAs nanowire [Per06]. Shchetinin et al. [Shc91] have determined a gold concentration of 3.5×10^{19} cm^{-3} in silicon wires grown at $1097\,^{\circ}$C by performing local electron-probe microanalysis. Such a concentration would exceed the equilibrium concentration of gold in silicon at this temperature by about two orders of magnitude [Sze81a]. If also at low growth temperatures the gold concentration in silicon nanowires would exceed its equilibrium value by two orders of magnitude, a replacement of gold by an alternative catalyst material may become unavoidable.

Chapter 1

Silicon Nanowire Growth

In this chapter our experimental results on the growth of silicon nanowires will be presented. We begin with the description of the wafer cleaning procedure, the experimental setup and the growth process. Afterwards, the epitaxial growth of silicon nanowires on silicon substrates using gold as catalyst is demonstrated. Our experimental results, using other catalyst materials than gold, are discussed subsequently.

1.1 Wafer Preparation

Before we come to the silicon nanowire growth itself, shortly the wafer preparation is to be described. In most cases, low doped, $<111>$ oriented 100 mm silicon wafers are used as substrates. Prior to growth, the residual contamination of these wafers is reduced by a two-step wet chemical cleaning process. In preparation of the wafer cleaning, first the necessary equipment is cleaned. For this purpose, two wafer holders and the tweezers are placed inside a quartz bowl and carefully rinsed with high purity water. The quartz bowl is then filled with the RCA1 solution [Ker93] consisting of 2 l of high purity water, 200 ml of NH_4OH, and 400 ml of H_2O_2, both of very-large-scale integration (VLSI) quality. The cleaning solution is then heated on a hot plate (Schott SLK 2) at maximum power for ten minutes to remove organic contaminations. Care should be taken that the temperature of the solution does not exceed 70 °C, since higher temperatures lead to a degradation of the cleaning solution and a concomitant reduction of the cleaning efficiency [Ker93]. After pouring out the RCA1 solution, the quartz bowl and its contents are rinsed again with high purity water. The cleaning procedure is repeated with the RCA2 solution [Ker93], that removes residual metal contaminations. For this aim, the quartz bowl with the holders and the tweezers inside is filled with 1.8 l of high purity water, 300 ml of concentrated HCl, and 300 ml H_2O_2, both of VLSI quality, and heated on the hot plate at maximum power for ten minutes. After pouring out the RCA2 solution, the bowl, the wafer holders, and the tweezers are rinsed with high purity water. With this, the preparations are completed. The wafers that are to be cleaned, usually eight or twelve, are placed in a wafer holder inside the quartz bowl, and the cleaning procedure is repeated as described before. The wafers are heated for ten minutes in the RCA1 solution, rinsed with high purity water, heated in

the RCA2 solution for ten minutes, and again rinsed with high purity water. To protect the wafers against dust particles from the ambient air, the wafers are kept immersed during and after the cleaning process. The easiest way to remove the native SiO_2 layer of the wafers is to dip the wafers for a few seconds into hydrofluoric acid. For this purpose a Teflon bowl is filled with 1.9 l of high purity water and 100 ml of concentrated HF (50%), corresponding to a concentration of 2.5%. Now a pair of wafers each is dipped for thirty seconds in the diluted HF to obtain an oxide free silicon surface. Together with the removal of the SiO_2 the silicon wafer surface becomes hydrogen terminated and hydrophobic. The wafer pair is then mounted with the polished sides face to face on a spinner, where three spacers keep the wafers at a distance of about 1 mm. The wafer pair is rotated at about 3000 turns/min for a few seconds to remove last HF drops from the wafer surface. Then the spacers are retracted and the wafers are slightly pressed together. If the wafer surfaces are sufficiently clean, this initiates a hydrophobic bonding of the wafers. The advantage of this hydrophobic bonding of the wafers is that from the moment of the bonding on, the cleaned polished surfaces of the wafers are protected against further dust and hydrocarbon contamination. The bonded wafers are then transferred into the UHV system without further delay.

1.2 Experimental Setup

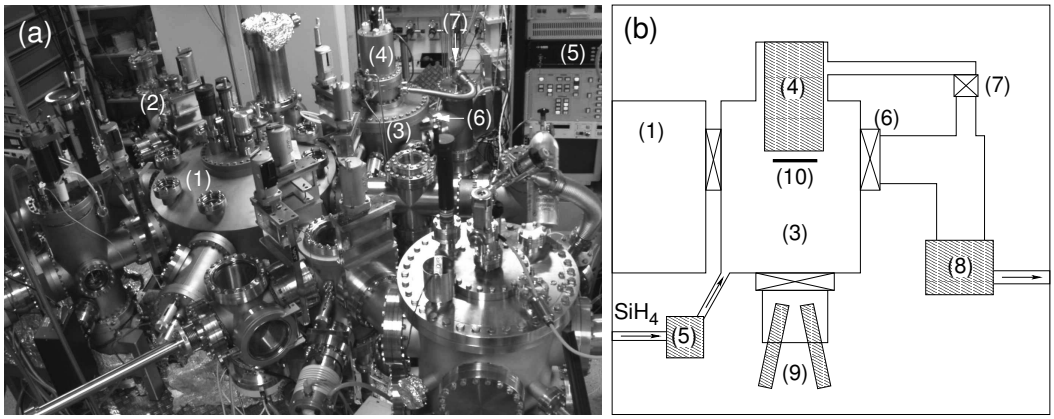

Figure 1.1: (a) Photograph of the UHV system. (b) Schematic side view of the growth chamber. (1) Main chamber, (2) metal deposition chamber, (3) growth chamber, (4) radiative heater, (5) mass-flow controller, (6) main valve, (7) dosing valve, (8) turbo pump, (9) antimony and boron evaporation sources, (10) silicon wafer.

The UHV system Fig. 1.1(a) is a cluster tool, consisting of the main chamber (1), having a base pressure around 1×10^{-10} mbar, and several attached side chambers, designed for different purposes. One of the necessary side-chambers for silicon nanowire growth is the metal deposition chamber (2), in which usually four electron beam evaporation sources (Tectra) are mounted. They are designated to the deposition of different catalyst materials for nanowire growth, as well as to the deposition of backside metal contacts to the

silicon wafers. The thickness of the evaporated metal layer can be controlled by a quartz deposition controller (Inficon). After depositing the catalyst metal, gold in most cases, the wafer can be transported in situ to the growth chamber (3). A schematic side view of the growth chamber is shown in Fig. 1.1(b). There the wafer (10) is positioned directly below a radiative heater (4) (Roth + Rau). This heater, designed for 100 mm wafers, basically consists of a graphite coil through which a high current is driven. To achieve a better homogeneity of the radiated heat, a graphite plate is located between the graphite coil and the wafer. The temperature of the heater and the ramping speed are controlled by a PID-controller (Eurotherm 216e). The heater was calibrated using a low doped silicon wafer of standard thickness onto which five thermocouple elements were tightly attached at different distances from the center of the wafer. The flow of diluted silane and other gases into the growth chamber is adjusted by an eight-channel mass flow controller (5) (MKS Instruments 647B). In order to achieve a constant growth pressure during nanowire growth, the main valve (6) that separates the growth chamber from the turbo pump (8) (Pfeiffer Vacuum TMU 520 C) is closed, while the dosing valve (7) is opened just wide enough to keep the pressure constant. The outgoing flow through the dosing valve can be indirectly controlled via the power consumption of the turbo pump (8). As discussed before, a doping of the nanowires can be achieved by mixing a small amount of a dopant metal to the catalyst droplet. For this aim two evaporation sources (9) are mounted right below the growth chamber. Antimony is deposited by an electron beam evaporation source (Tectra), while a thermal high temperature evaporation source (MBE Komponenten, HTS) is used for the boron evaporation.

1.3 Catalyst Deposition and Annealing

After transferring the pre-bonded wafer pairs into the UHV system, the wafers are either stored inside the UHV system at a pressure of 1×10^{-10} mbar or separated in situ for nanowire synthesis. For the deposition of the catalyst material, one wafer is transported into the metal deposition chamber. Usually, a layer, 0.1 nm to 0.5 nm thick, is evaporated onto the hydrogen terminated wafer surface. After the deposition, the wafer is transported in situ to the growth chamber for an annealing of the catalyst metal layer. An annealing of the catalyst is the easiest method to produce a large number of separated catalyst particles, necessary for the nanowire synthesis.

As shown in Fig. I.1(b), the characteristic feature of the Au/Si phase diagram is its low temperature eutectic point at 363 °C, at temperatures significantly lower than the melting points of pure gold, 1064 °C, or pure silicon, 1414 °C. Upon annealing the gold film at a temperature above the eutectic temperature, silicon from the substrate will diffuse into the gold layer, producing a liquid Au/Si alloy. In order to reduce its total surface and interface energy, the Au/Si film will break up into a distribution of Au/Si droplets. In addition to these droplets, a certain density of gold ad-atoms will be present on the silicon surface. These ad-atoms can diffuse on the silicon surface. Since the larger droplets with their smaller surface-to-volume ratio are energetically more favorable than the smaller droplets,

gold ad-atom diffusion will lead to a net transport of gold from the smaller to the larger droplets. Thus the larger droplets will grow at the expense of the smaller ones. This process of particle growth is known as Ostwald ripening. A first theory of Ostwald ripening was developed by Lifshitz and Slyozov [Lif61]; a comprehensive treatment based on their theoretical model was presented by Chakraverty [Cha67] and Wynblatt et al. [Wyn76b, Wyn76a]. The outcome of the model is threefold. First, the existence of a critical time-dependent droplet radius $r^\star(t)$ is predicted. At a time t, droplets that are smaller than the critical radius $r^\star(t)$ will shrink, while droplets having a radius greater than $r^\star(t)$ will increase in size. If the transition of gold ad-atoms to or from the droplets is taken to be the rate determining step of the ripening process, the critical radius $r^\star = 8/9\ \bar{r}$, with $\bar{r}$ being the average droplet radius [Wag61]. Second, one can show that the average radius of the distribution will increase as a power law in time

$$\bar{r}(t) = \bar{r}(0)\Big(1 + \kappa t\Big)^{1/2} \qquad \text{[Wag61]}\,, \tag{1.1}$$

where κ is a kinetic coefficient. The third outcome is that the droplet distribution function $f(\rho)$, with $\rho = r/\bar{r}$, becomes a time independent function in the limit $t \to \infty$. Normalized to unity, the distribution function $f(\rho)$ is given by [Wag61].

$$f(\rho) = \frac{16\rho}{27\big(1 - \frac{4\rho}{9}\big)^5} \exp\big(\frac{-12\rho}{9 - 4\rho}\big)\,. \tag{1.2}$$

This distribution is plotted in Fig. 1.2(a) as a solid line.

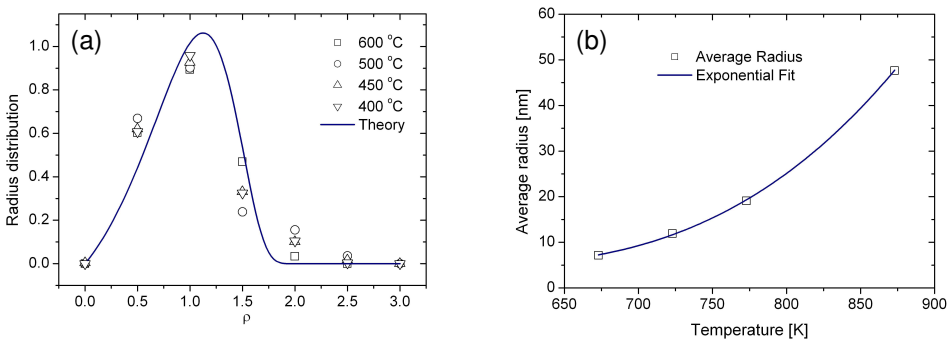

Figure 1.2: (a) Radius distribution of Au/Si droplets after 20 minutes of annealing at different temperatures, see also Fig. A.2. (b) Mean radius of Au/Si droplets as a function of the annealing temperature, see also Fig. A.3.

In order to compare these theoretical predictions with experimental results, we deposited $0.5\,$nm of gold onto hydrogen-terminated silicon wafers. These wafers were annealed at different temperatures for 20 minutes. At the end of the annealing time the temperature was rapidly decreased. The distribution function was obtained by measuring the droplet radii of overall about two thousand droplets in scanning electron micrographs. The experimentally determined radius distribution is displayed in Fig. 1.2(a). One can see

that the theoretical curve is in fair agreement with the experimentally obtained data. Note that the distribution is plotted versus the dimensionless variable $\rho = r/\bar{r}$ and that this disguises that the mean radius $\bar{r}$ varies by about a factor of six between the sample annealed at $600\,^{\circ}\mathrm{C}$ and the one annealed at $400\,^{\circ}\mathrm{C}$.

Figure 1.2 (b) shows the experimentally determined mean radii as a function of temperature and an exponential fit to these data. Suppose, the temperature dependence of the kinetic coefficient κ can be described by an exponential relation with a constant κ_o and an activation energy ΔG, then the mean radius $\bar{r}$ can be expressed as

$$\bar{r}(t,T) = \bar{r}(0)\Big(1 + \kappa_o t \exp(-\frac{\Delta G}{kT})\Big)^{1/2}. \tag{1.3}$$

From the least square fit, shown in 1.2 (b), we could obtain the following parameters $\bar{r}(0) = (5 \pm 1)\,\mathrm{nm}$, $\kappa_o = (1.5 \pm 0.4) \times 10^5\,\mathrm{s}^{-1}$, and $\Delta G = (1.08 \pm 0.03)\,\mathrm{eV}$. Using these parameters together with equation (1.3) we can estimate the annealing times and annealing temperatures that are necessary to obtain the desired mean droplet radius. Another parameter at hand that can be used for adjusting the droplet size is the initial thickness of the gold film. Thus by varying the initial gold thickness, the annealing temperature, and the annealing time, we are able to adjust both the average droplet size and the droplet density within a certain range.

1.4 Experimental Results Using Gold as Catalyst

After the annealing of the gold-covered samples, the wafer temperature is lowered to the desired growth temperature, which is usually between $400\,^{\circ}\mathrm{C}$ and $500\,^{\circ}\mathrm{C}$. The main valve to the turbo pump and the dosing valve are closed, and the growth chamber is filled with diluted silane (5 % in argon) till an overall chamber pressure of about $2\,\mathrm{mbar}$ is reached. The silane flow during growth is usually set to $40\,\mathrm{sccm}$. If the desired growth pressure is reached, the dosing valve is slightly opened to establish a constant growth pressure, while maintaining a continuous flow of diluted silane. This state is kept for a few to many minutes. Depending on the growth temperature and pressure the growth velocity varies, but is typically of the order of $1\,\mathrm{nm\,s}^{-1}$. The progress of nanowire growth can be observed through a window of the growth chamber, which is quite helpful, as the visual appearance of the wafer changes considerably during growth. If the desired nanowire length is reached, the silane flow is switched off and the silane remaining in the growth chamber is pumped via the dosing valve, till a chamber pressure of 0.1 mbar is reached. Then the main valve to the turbo pump is opened, which causes a rapid decrease of the chamber pressure to below $10^{-6}\,\mathrm{mbar}$. At last, the heating power is reduced and the wafer is cooled down to room temperature. Figure 1.3 (a) shows a scanning electron micrograph of silicon nanowires grown epitaxially on a (111)-oriented substrate. In this experiment $0.5\,\mathrm{nm}$ of gold were deposited onto the wafer, and the wafer was annealed at the growth temperature of $450\,^{\circ}\mathrm{C}$ for 38 minutes. Silicon nanowire growth proceeded within six minutes, at a chamber pressure of 2 mbar and a flow of 40 sccm of diluted silane (5% in argon). One can see that the resulting nanowires have a relatively large diameter of $50\,\mathrm{nm}$ and an aspect ratio of

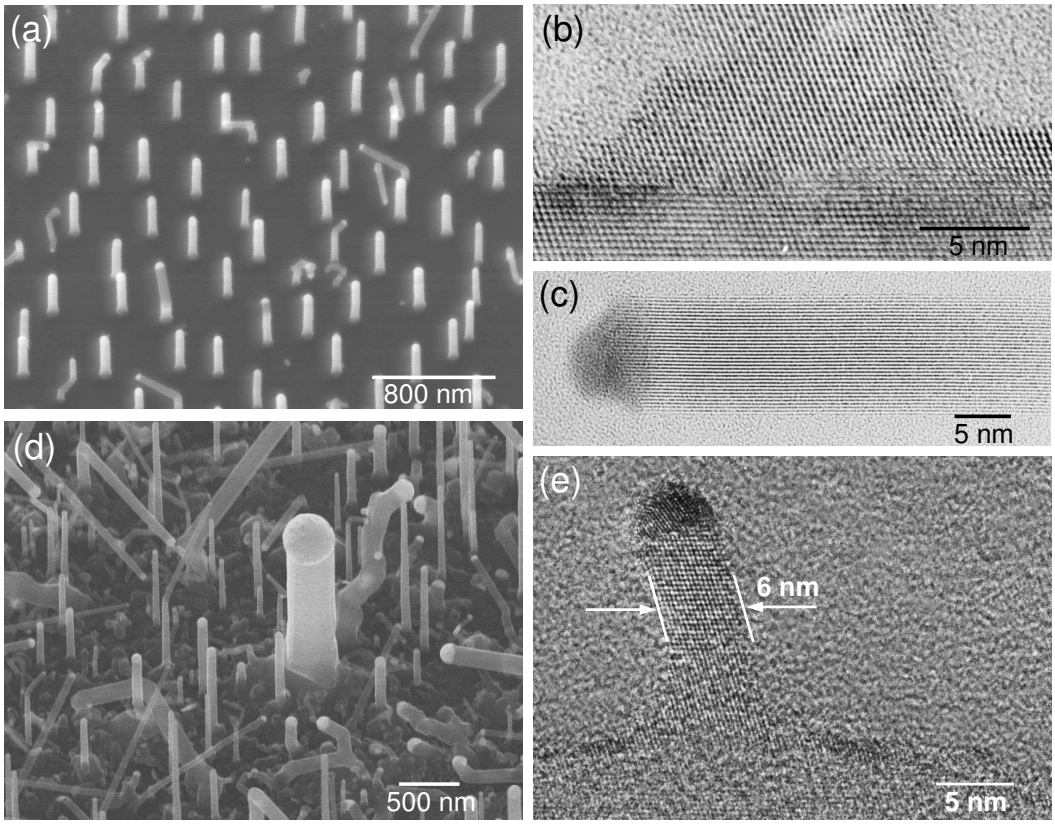

Figure 1.3: (a),(d) Scanning electron micrograph of silicon nanowires grown with gold on a <111> oriented silicon substrate. (b),(e) High resolution TEM image of a silicon nanowire grown epitaxially on a <111> oriented silicon substrate. (c) High resolution TEM image of the tip region of a thin silicon nanowire.

about ten. A large percentage of the wires are grown in the [111] direction perpendicular to the substrate surface, which is an indication for epitaxial growth. Due to the extended annealing, the nanowires are quite homogeneous in diameter and well separated from each other. Some of the nanowires exhibit kinks, i.e. abrupt changes in their growth direction. This is an often observed phenomenon [Wag68] that might be related to the low growth pressure [Oza98] or/and the low growth temperature [Wes97a]. The nanowires show only slight tapering, if any, which is typical for silicon nanowires grown at low temperatures with gold as catalyst. Figure 1.3 (b) shows a cross section transmission electron microscope (TEM) image (Jeol 4010) of the region where a thin silicon nanowire is attached to the substrate. Clearly, the epitaxial nature of the transition between the (111)-oriented substrate and the nanowire can be observed. In addition, the single crystalline nature of the silicon nanowire is apparent. This can also be seen in Fig. 1.3(c), where the gold tip and the tip region of a silicon nanowire with 10 nm diameter is shown. Figure 1.3 (d) and (e) show the largest and smallest nanowire we found so far. It is remarkable that the growth process works equally well from 6 nm to about 600 nm, hence over a diameter variation

of about two orders of magnitude. Note also the epitaxial contact to the substrate, and the expansion at the nanowire base, visible in Fig. 1.3(e).

1.5 Using other Catalysts than Gold

Gold is the catalyst most frequently used for nanowire synthesis in general, and silicon nanowire growth in particular. There are some criteria which make gold a well suited catalyst material. The first, and maybe most important one, is related to the low temperature eutectic point of the Au/Si phase diagram (see Fig. I.1). This allows for growth temperatures as low as $360\,^{\circ}\mathrm{C}$, which becomes important, if silicon nanowire synthesis is combined with process steps that do not allow high temperatures. Another important aspect of the Au/Si phase diagram is the relatively high silicon solubility at the eutectic temperature. This makes the growth process robust against fluctuations of the silicon concentration, as will readily be shown. Let us consider a half-spherical Au/Si catalyst particle of $10\,\mathrm{nm}$ in diameter. At the eutectic point the number of gold atoms in this droplet is approximately $1.5{\times}10^4$, compared to about $2.5{\times}10^3$ silicon atoms. Given the smallest possible fluctuation of plus or minus one silicon atom, the relative concentration change will be only 0.04%. However, suppose the silicon solubility at the eutectic point would be very small, let's say 0.004%, like for an In/Si alloy of eutectic composition. Then a fluctuation of plus or minus one silicon atom would cause a relative concentration change of more than 100%. This might have severe effects on the stability of the growth process.

Another argument for the use of gold as a catalyst is the low vapor pressure at the moderate growth temperatures. A re-evaporation of the catalyst material during growth can practically be neglected. The high chemical stability of gold is an additional advantage, especially in view of a pre-growth processing of the substrate. A patterning of the substrate with a well defined arrangement of gold particles, for example, including subsequent nanowire growth can be easily done [Wes97b].

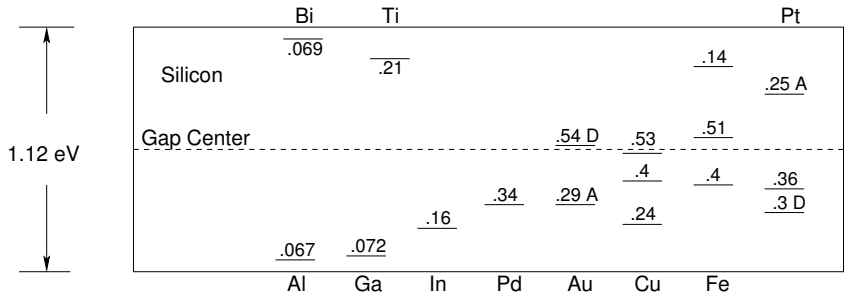

Figure 1.4: Ionization energies of different impurities in silicon, after [Sze81b]

On the other hand, the high chemical stability of gold is one of the most severe drawbacks. A possible gold contamination of equipment used for a post-growth processing of the nanowires can hardly be removed. This alone would not be that severe, if gold would not be known to create very efficient recombination centers in silicon - a feature of special

importance for those electronic applications, which rely on a low electron-hole recombination rate. Assuming identical electron and hole cross sections σ, the recombination rate U of a trap is given by

$$U = \sigma\sqrt{3kT/m*}N_t \frac{pn - n_i}{p + n + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)} \qquad \text{[Sze81b]}\,, \tag{1.4}$$

where N_t is the trap density and E_t is the energy level of the trap. One can see that the recombination rate strongly depends on the energy difference between the trap level E_t and the band gap middle E_i, such that deep levels, located close to the band gap middle, cause a maximal recombination rate. As shown in Fig. 1.4, gold does create such deep levels.

Therefore, especially in view of future electronic applications, it is desirable to replace gold with a catalyst material ideally offering all the advantages of gold, but being less problematic with respect to the defects it creates. We tested six different materials - palladium, iron, dysprosium, indium, bismuth, and aluminum. The first three are known to form metal silicides, having melting points beyond the growth temperature that can be applied in our system. Thus growth is presumably catalyzed by a solid catalyst particle. The last three elements - indium, bismuth, and aluminum - are characterized by a eutectic point at low or moderate temperatures, which in principle allows for the vapor-liquid-solid growth of silicon nanowires.

1.5.1 Palladium

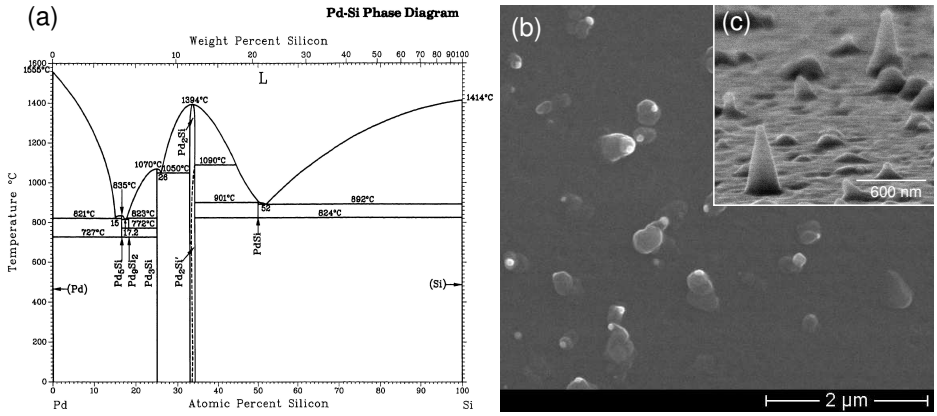

Figure 1.5: (a) Pd/Si phase diagram [Mas90b], see also Fig. A.4. (b) Top view SEM image of growth attempt using Pd as catalyst. Inset: tilted view (80°) SEM image of nanowires grown with Pd as catalyst.

From the point of view of electronic compatibility, palladium is an interesting catalyst. It only produces one electric defect, 0.34 eV above the conduction band (see Fig. 1.4). The Pd/Si phase diagram in Fig. 1.5(a) shows different palladium silicides for temperatures below $800\,^{\circ}$C. The lowest temperature eutectic point is located at about $800\,^{\circ}$C, a temperature beyond the possibilities of our equipment. For the growth experiment we in situ deposited

a thin layer of palladium onto a hydrogen-terminated (100)-oriented silicon wafer using an electron beam evaporation source. After transferring the wafer to the growth chamber, the wafer was annealed at 670 °C for ten minutes to break up the palladium film. Then the growth chamber was flooded with diluted silane (5% in argon, 40 sccm) till a pressure of 2 mbar was reached. This pressure was kept constant for 6 min. Afterwards the silane flow was switched off, and the chamber is evacuated. A top view scanning electron micrograph of the sample is shown in Fig. 1.5(b). One can see that a low density of nanostructures was obtained. Most of them show a small particle at their tip, presumably consisting of palladium silicide. As shown in Fig. 1.5(c), some of these nanostructures are grown vertically with respect to the substrate, and these might be classified as strongly tapered nanowires.

1.5.2 Iron

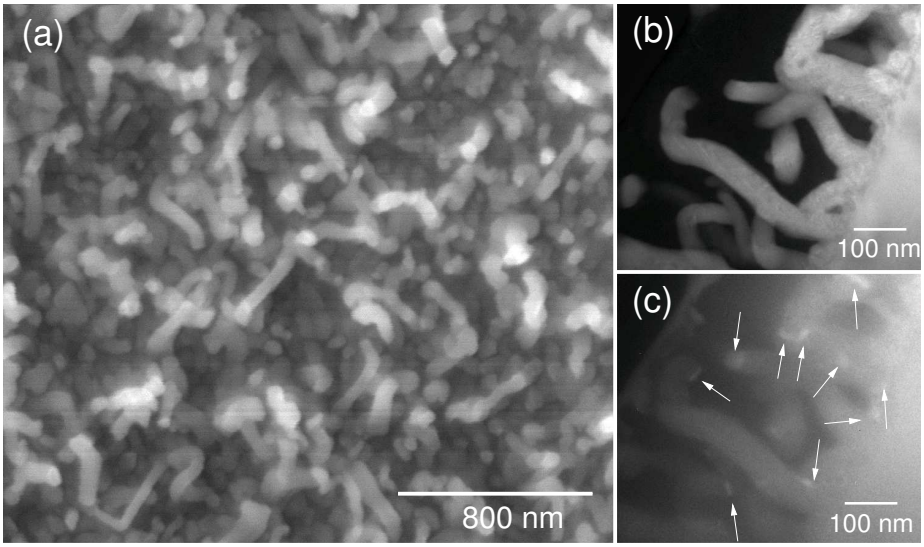

Figure 1.6: (a) Top view scanning electron micrograph of silicon nanowires grown with Fe. (b) TEM cross section image of the silicon nanowires grown with Fe. (c) EFTEM image at the Fe L-edge; white arrows indicate the iron rich particles.

As mentioned before, one element that proved to be able to promote the growth of silicon nanowires, is iron. But either extremely high temperatures (1200 °C) [Mor98], or oxygen-rich conditions [Liu01] had to be applied. Our experiments, on the contrary, were performed at low temperatures and in nominally oxygen-free environment. Iron was deposited in situ as a film of 1 nm thickness onto a hydrogen-terminated silicon wafer, using an electron beam evaporation source. Without an intermediate annealing step, the wafer was heated to 580 °C. After reaching this temperature the chamber was flooded with diluted silane, reaching a pressure of 2.8 mbar after two minutes. Growth was terminated

after six minutes. As shown in Fig. 1.6(a), a large quantity of wire-like structures was produced this way. A preferential growth direction could not be identified. In contrast to the nanowires grown with gold, TEM investigations revealed that the wires exhibit a large number of crystallographic defects. Growth starts with a few layers of defect free silicon. The longer the wire grows, the greater the density of crystallographic defects becomes. Finally, the nanowires are polycrystalline. According to the Fe/Si binary phase diagram, a liquid phase is absent at the growth temperature, and indeed, droplet-like structures at the tip of the wires can neither be seen in Fig. 1.6(a), nor in the cross section transmission electron micrograph (Philips CM20FEG) shown Fig. 1.6(b). However, energy filtered TEM (EFTEM) (Fig. 1.6(c)) at the iron L-edge revealed several iron-containing, plate-shaped particles. Analogously to the growth of silicon nanowires using titanium [Kam01] as catalyst, the particles presumably consist of an iron silicide. In this case, growth cannot be described by the vapor-liquid-solid mechanism, but rather by a vapor-solid-solid mechanism.

1.5.3 Dysprosium

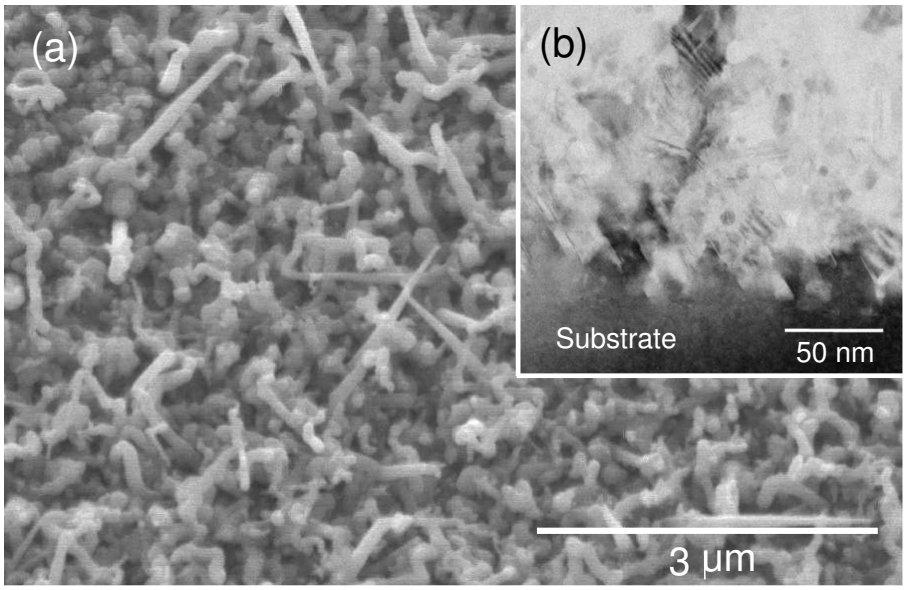

Figure 1.7: (a) Top view scanning electron micrograph of silicon nanowires grown with Dy. (b) TEM cross section image of the silicon nanowires grown with Dy.

A metal, which to our knowledge has not been reported by other groups as a catalyst for silicon nanowire growth, is dysprosium. In our experiments 0.4 nm of dysprosium were in situ deposited on a hydrogen-terminated silicon wafer. The wafer was subsequently heated to the growth temperature of 630 °C with the silane partial pressure set to 0.15 mbar.

The wires produced in this way are shown in Fig. 1.7(a). Most interesting are the long, tapered, needle-like structures. Their strong tapering might be explained by an additional overgrowth of the wire. In the cross section transmission electron micrograph shown in Fig. 1.7(b) one can see that also the wires grown with dysprosium exhibit a large number of crystallographic defects. Similar to iron, the Dy/Si binary phase diagram shows no liquid phase at the growth temperature. Hence growth, catalyzed by a solid dysprosium silicide particle, offers the most probable explanation.

1.5.4 Bismuth

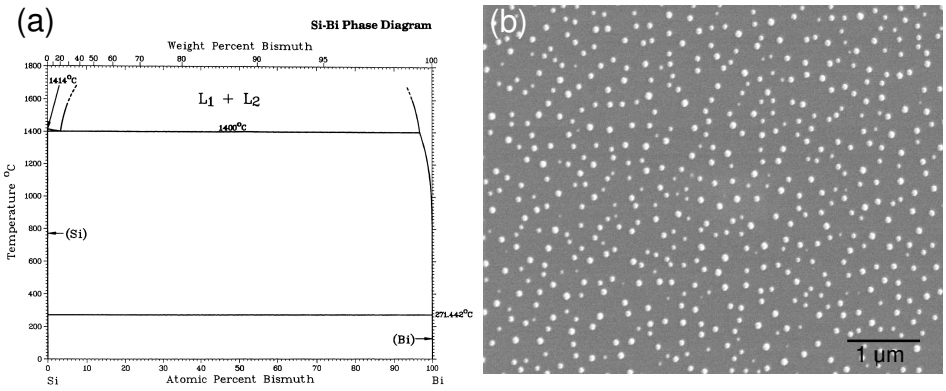

Figure 1.8: (a) Bi-Si phase diagram [Mas90a], see also Fig. A.5. (b) Top view SEM of growth attempt using Bi.

Let us now turn to the catalyst metals that are characterized by a eutectic point in the binary metal/Si phase diagram. Bismuth is an interesting candidate for replacing gold. The electronic level is close to the conduction band, thus bismuth would cause an n-doping of the nanowires. As shown in Fig. 1.8(a), the Bi/Si phase diagram has a eutectic point at $271\,^{\circ}$C, which in principle would allow for silicon nanowire growth at very low temperatures. For the growth experiments, about 1 nm of bismuth was in situ deposited onto hydrogen-terminated $<111>$ oriented silicon wafers by an electron beam evaporation source. Different growth conditions were tested with similar outcome. Figure 1.8 (b) shows a typical top view scanning electron micrograph of a sample that was processed at a temperature of $510\,^{\circ}$C and a pressure of 1.9 mbar. A high density of droplets with a size of the order of 100 nm can be observed, but apparently no nanowires are present. One possible reason for the failure of the growth experiments might be the small surface tension, σ_l, of the Bi/Si droplets. According to Nebolsin et al. [Neb03] the surface tension of the liquid σ_l has to be greater than $\sigma_s/\sqrt{2}$, with σ_s being the surface tension of solid silicon. This requirement is not met by a Bi/Si alloy. Also the extremely small silicon solubility at $500\,^{\circ}$C might be a possible cause for the failure of the experiments.

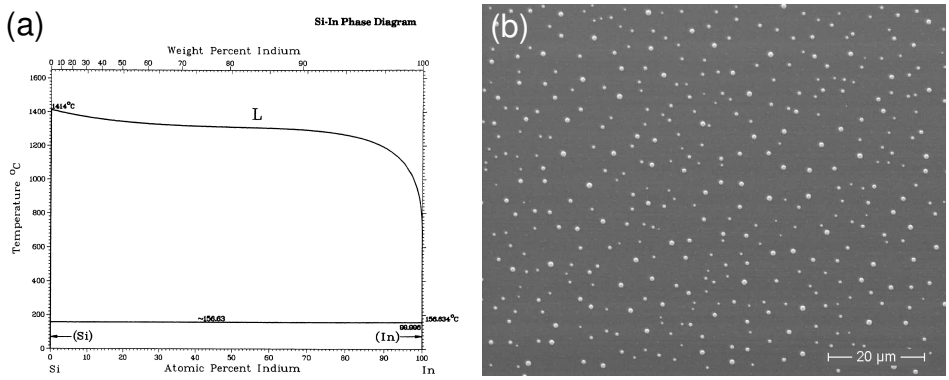

Figure 1.9: (a) In-Si phase diagram [Mas90b], see also Fig. A.6. (b) Top view SEM of growth attempt using In.

1.5.5 Indium

The characteristic of the binary In/Si phase diagram, shown in Fig. 1.9(a), is similar to the Bi/Si phase diagram, as it also exhibits a low temperature eutectic point at $180\,^{\circ}\mathrm{C}$ at a very low silicon concentration. But in contrast to bismuth, indium creates an electronic level in silicon that is located $0.16\,\mathrm{eV}$ above the valence band edge, thus causing a p-doping of the nanowires. Different growth conditions were tested, yet without success. The result presented in Fig. 1.9(b) was obtained with about $4\,\mathrm{nm}$ of indium, deposited onto a hydrogen-terminated (111) silicon wafer. We used a growth temperature of $570\,^{\circ}\mathrm{C}$ and a pressure of 1.8 mbar. Figure 1.9 (b) exhibits a distribution of large droplets, but no silicon nanowires can be found. Like for bismuth, the small indium surface tension might account for the failure of the experiment. As previously discussed, also the low silicon solubility at the growth temperature could have prevented the growth of nanowires.

1.5.6 Aluminum

Aluminum is probably the most promising candidate for the replacement of gold as catalyst for silicon nanowire synthesis, as the Al/Si phase diagram (see Fig. 1.10(a)) exhibits the closest similarity to the Au/Si phase diagram. Like this, it is of the simple eutectic type, with a single eutectic point located at a moderate temperature of $577\,^{\circ}\mathrm{C}$. Also the silicon concentration of 12% is comparable to the silicon concentration of 19% at the Au/Si eutectic point. However, regarding the electronic properties, aluminum offers great advantages compared to gold. Aluminum creates an electronic defect $0.067\,\mathrm{eV}$ (see Fig. 1.4) above the valence band edge such that nanowires grown with aluminum would be p-doped. The most important argument in favor of aluminum is that it is compatible with existing electronics fabrication technology.

In our experiments we deposited about $1\,\mathrm{nm}$ of aluminum, using a thermal evaporation source, in situ onto a hydrogen terminated (111)-oriented silicon wafer. After heating the wafer to a temperature of $510\,^{\circ}\mathrm{C}$, the silane flow (40sccm 5% in argon) was switched

on. Three minutes later, at a chamber pressure of 4.3 mbar, the wafer temperature was increased to 620 °C. Directly after reaching this temperature, a change of color of the wafer could be observed. Temperature and pressure were kept constant for another 16 minutes. A tilted scanning electron micrograph of the resulting nanowires is displayed in Fig. 1.10(b). The silicon nanowires are strongly tapered and facetted, showing a three-fold symmetry and in addition a particle at their tip. The SEM image shown in Fig. 1.10(d) gives a better impression of the shape of the nanowires. Interesting are the well defined surface planes, which we, however, could not clearly identify yet. The TEM image (Philips CM20) of Fig. 1.10(c), shows a cross section of the sample that was cut with respect to the vertical image axis of Fig. 1.10(b). Therefore the left flank of the nanowire appears at a steeper angle than the right flank. One can see that the nanowires are grown epitaxially on the silicon wafer and that they are single crystalline, exhibiting only few defects. Recent experiments indicate that both the tapering and the diameter of the silicon nanowires grown with the help of aluminum can be strongly reduced by optimizing the growth conditions.

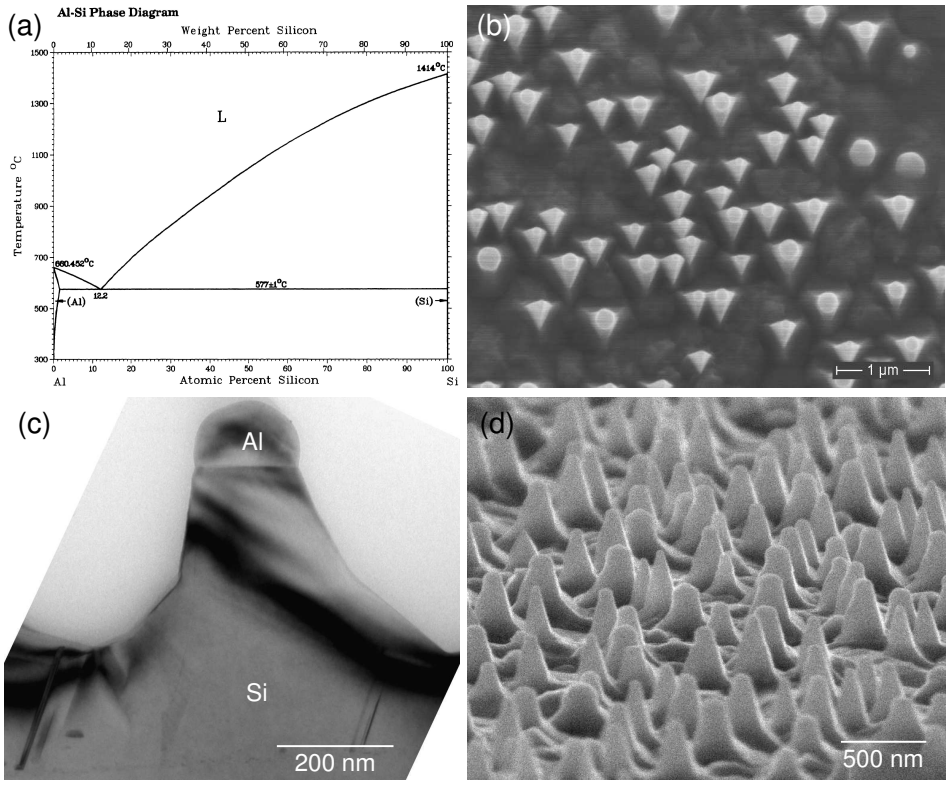

Figure 1.10: (a) Al-Si phase diagram [Mas90a], see also Fig. A.7. (b) Tilted view (24°) SEM image of silicon nanowires grown with Al. (c) TEM cross section image of the silicon nanowires grown with Al. (d) Tilted view (80°) SEM image of silicon nanowires grown with Al.

1.6 Conclusions of Chapter 1

To conclude, we have seen that gold is a well suited catalyst for silicon nanowire growth at moderate temperatures. By choosing the proper annealing conditions, both the average diameter and the density of the Au/Si alloy particles can be adjusted. The resulting nanowires are usually single crystalline and grown epitaxially on the substrate. In addition, different metals have been tested with regard to their ability of replacing gold as catalyst for nanowire growth. Palladium, iron, and dysprosium proved to be able to catalyze the growth of silicon nanowires at temperatures around $600\,^{\circ}\mathrm{C}$. However, the crystalline quality of the nanowires synthesized with the help of iron and dysprosium was rather poor. Silicon nanowire growth with the help of bismuth and indium did not succeed, at least in the parameter range we tried. The most promising alternative to gold seems to be aluminum, with which nanowires of high crystalline quality can be produced at temperatures around the eutectic point of the Al/Si alloy.

Chapter 2

Diameter Dependence of the Growth Velocity

A possible integration of epitaxially grown silicon nanowires into a complex device architecture necessarily demands a high level of control over the nanowire morphology. One has to be able to control the nanowire length, diameter, and growth direction simultaneously; and ideally independently of each other. However, a well-defined nanowire morphology cannot be achieved without a fundamental understanding of the factors that determine length, diameter, and growth direction of the nanowires. Particular attention has to be payed to possible inter-dependencies between these three parameters, as this of course limits the parameter space.

This chapter and the two chapters following thereupon, each deal with one specific fundamental aspect of the length, the diameter, and the growth direction of silicon nanowires. In Chapter 3 the diameter of epitaxially grown silicon nanowire is considered. Although the diameter is basically constant over almost the entire length, the base of the nanowire, that is the region where the nanowire is attached to the substrate, exhibits a diameter expansion. We will demonstrate that the origin of this expansion is directly related to the vapor-liquid-solid (VLS) mechanism, and that the equilibrium mechanics of the liquid catalyst droplet in the initial stage of growth accounts for the shape of this expansion. Chapter 4 deals with the diameter dependence of the crystallographic growth direction. We present experimental results proving that the crystallographic growth direction of epitaxially grown silicon nanowires is diameter-dependent and propose a model for this diameter dependence.

In this chapter we focus on the nanowire length, or - more accurately speaking - on the main factor that determines the nanowire length - the growth velocity. The nanowire growth velocity is known to be diameter-dependent, a phenomenon related to the Gibbs-Thomson effect. However, we will see in the course of this chapter that the influence of the Gibbs-Thomson effect on the growth velocity is more subtle than usually expected, as the diameter dependence of the growth velocity is strongly affected by the applied growth conditions.

2.1 Introduction

A schematic of the vapor-liquid-solid (VLS) growth mechanism, the most widely used approach for the synthesis of silicon nanowires, is shown in Fig. 2.1(a). The essential ingredient for this technique is a liquid metal/silicon alloy droplet that enables the growth of rod-like structures. The necessary silicon for the nanowire growth is usually supplied by a gaseous silicon precursor like silane, SiH_4, or silicon tetrachloride, $SiCl_4$. Due to the larger sticking coefficient of the droplet, compared to the bare silicon surface, unidirectional growth is favored. At the droplet surface, the silane molecules are cracked, and the resulting silicon atoms are incorporated in the droplet. There they diffuse through the droplet to the liquid-solid interface at the bottom of the droplet, where they form the silicon nanowire. Thus, the vapor-liquid-solid mechanism of silicon nanowire growth basically consists of three steps, see Fig. 2.1(a). First, the adsorption and cracking of the Si precursor at the surface of a liquid metal/Si alloy droplet (i); the thereby produced Si is incorporated in the droplet at a rate ρ_{inc} [mol/unit time]. Second, the diffusion of Si through the droplet (ii). And third, the crystallization of the Si nanowire at the liquid-solid interface (iii), proceeding at a rate ρ_{cry} [mol/unit time].

Especially in the 1970s several authors [Giv75, Boo71, Wey78] discussed, which of these three steps is rate-determining for the VLS growth, and just recently this topic was brought up again [Kod06]. Only the diffusion step can be excluded with a high probability, since for droplets of microscopic dimensions, diffusion through the liquid alloy is too fast as to be rate determining. Bootsma and Gassen [Boo71], mainly in view of the pressure dependence of the growth velocity, favored step one, the incorporation step. In contrast to this, Givargizov [Giv87b] took the opinion that the crystallization of the nanowire at the liquid-silicon interface is rate determining. His main argument was that the growth velocity depends on the crystallographic growth direction, which, from his point of view, could only be explained if step number three is taken to be the rate determining one.

Yet, this discussion, whether ρ_{inc} or ρ_{cry} is rate determining, does not account for the full complexity of the problem. First of all, the influence of the growth parameters, e.g. silane pressure or temperature, on the rate balance is not considered. One cannot exclude a priori that for one parameter range one step is rate determining, whereas for another parameter range, the other. Furthermore, both rates are implicitly dealt as independent processes - an assumption, which is most likely unjustified, as both ρ_{inc}, and ρ_{cry} probably depend on the silicon chemical potential of the liquid droplet. In this case, both processes could interact with each other via this chemical potential. In a steady state situation, where ρ_{inc} equals ρ_{cry}, the silicon chemical potential of the droplet needs to adjust in a way that both rates level out. As a consequence of this, we are generally facing a situation where the interplay of both rates determines the growth velocity instead of one rate.

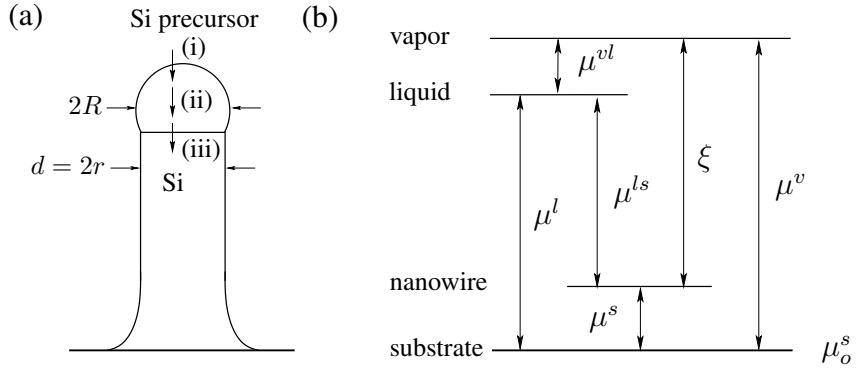

Figure 2.1: (a) Schematic of the VLS mechanism: (i) incorporation, (ii) diffusion, (iii) crystallization. (b) Chemical potentials (CPs): μ_o^s = CP of the Si substrate, μ^v = CP of the Si vapor, μ^s = CP of the Si nanowire, μ^{vl} = CP difference between the Si vapor and the liquid droplet, μ^{ls} = CP difference between the liquid droplet and the Si nanowire, ξ = CP difference between the Si vapor and the Si nanowire.

2.2 Definitions and Experimental Results

We only consider the silicon chemical potentials. As a refence point we choose the chemical potential of the substrate μ_o^s, which is fixed by the boundary conditions. Also fixed by the boundary conditions is the chemical potential of the vapor μ^v. Due to the surface contribution to the Gibbs free energy, the chemical potential of a nanowire of radius r is increased by an amount proportional to the surface to volume ratio, to the specific surface energy of the nanowire, $\sigma^s \approx 1.24\,\mathrm{J\,m^{-2}}$ [Jac63], and to the molar volume of solid silicon, $\Omega^s \approx 12\,\mathrm{cm^3/\,mol}$. This is the so-called Gibbs-Thomson effect, sometimes also referred to as Laplace-Young effect. Thus, the chemical potential of a silicon nanowire μ^s with respect to the silicon substrate can be expressed as

$$\mu^s = \frac{C^s}{r} \qquad [\text{Def66, Tan04}], \tag{2.1}$$

with C^s defined as $C^s = 2\Omega^s\sigma^s$. A similar relation holds for μ^l, the chemical potential of the liquid metal/silicon droplet

$$\mu^l = \mu_o^l + \frac{C^l}{R}\,. \tag{2.2}$$

Here, R is the droplet radius and μ_o^l is the chemical potential of a droplet of infinite size. The constant $C^l = 2\Omega^l\sigma^l$, with σ^l and Ω^l being the surface tension and the molar volume of the liquid alloy. As shown in Fig. 2.1, μ^{vl} and μ^{ls} are the chemical potential differences between the vapor and the liquid droplet, and between the liquid droplet and the silicon nanowire, respectively. The quantity ξ is defined as the chemical potential difference between vapor and silicon nanowire. According to their definitions, these three quantities have to fulfill the following relation

$$\xi = \mu^{vl} + \mu^{ls}\,. \tag{2.3}$$

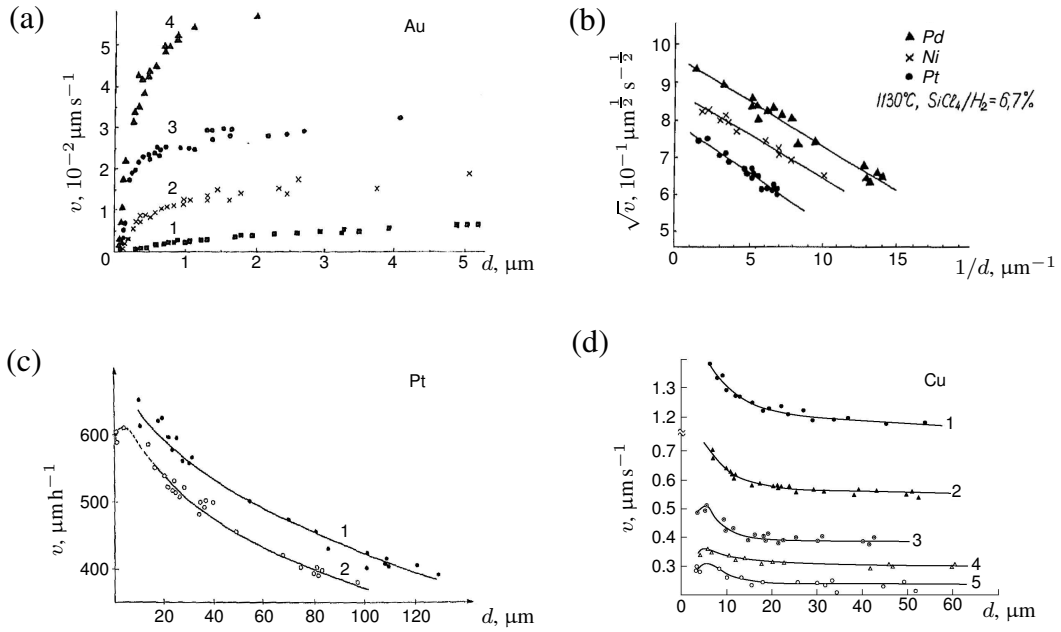

Figure 2.2: Diameter dependence of the growth velocity; all experiments performed with $SiCl_4$ as precursor. (a) Growth velocity v as a function of the wire diameter d; $SiCl_4$ pressure increases from 1 to 4; after [Giv75], see also Fig. A.8. (b) $\sqrt{v}$ as a function of the inverse wire diameter $1/d$; after [Giv75], see also Fig. A.9. (c) v as a function of d; temperature 1000 °C to 1100 °C; 1) $SiCl_4$:$H_2 = 0.9\%$ 2) $SiCl_4$:$H_2 = 0.95\%$; after [Wey78], see also Fig. A.10. (d) v as a function of d; temperature: 1) 1027 °C, 2) 1047 °C, 3) 1067 °C, 4) 1087 °C, 5) 1107 °C; after [Neb05], see also Fig. A.11.

After these preparatory works, let us come back to the diameter dependence of the growth velocity. Figure 2.2 shows some experimental observations of the growth velocity of silicon nanowires produced via the VLS growth mechanism using different catalysts. The diameter dependence of the growth velocity of silicon nanowires grown with $SiCl_4$ as precursor and gold as catalyst was measured by Givargizov [Giv75]. His experimental results are reproduced in Fig. 2.2(a). He observed an increase of the growth velocity for increasing nanowire diameters, which he explained [Giv75] by the radius dependence of μ^s, according to equation (2.1). He argued that the growth velocity directly correlates with the supersaturation of the droplet, i.e. the chemical potential difference between liquid droplet and silicon nanowire. The increase of μ^s, according to equation (2.1), leads to a decrease of the supersaturation by an amount $2\Omega^s\sigma^s/r$, and this term is directly responsible for the diameter dependence of the growth velocity. However, we will see later on that this result is only valid in the limit where the crystallization rate determines the growth velocity.

In his work [Giv75], Givargizov also presented results on the radius dependence of the growth velocity using other catalyst materials than gold (see Fig. 2.2(b)). His growth experiments with platinum, nickel, and palladium agree with the gold observations inasmuch as they also show an increase of the growth velocity with increasing diameter.

Furthermore, note that according to Fig. 2.2(a) the growth velocity increases with increasing $SiCl_4$ partial pressure. Although this is the usual and expected behavior (see [Boo71, Giv75, Wes97a, Lew03]), it is emphasized here, as this point will later on turn out to be important.

Interestingly, the experimental results of Weyher [Wey78] (Fig. 2.2(c)) with Pt as catalyst show an opposite radius dependence compared to the Pt results of Givargizov, see Fig. 2.2(b). Since the catalyst is the same, one has to conclude that either the different growth conditions and/or the different radii of the silicon wires are responsible for the observed difference in behavior. In any case, it demonstrates that the radius dependence of the growth velocity is a more complex phenomenon than usually expected.

Another important aspect, considering the gold results of Fig. 2.2(a) and the platinum results of Fig. 2.2(c), is that not only the radius dependence, but also the pressure dependence differs. In Fig. 2.2(c), the growth velocity decreases with increasing pressure, which is a rather odd behavior; usually one would expect the opposite [Boo71, Giv75, Wes97a, Lew03]. A possible explanation can be found by considering the adsorption and cracking efficiency of the metal alloy droplet. For a low vapor pressure, it is expected that the number of incoming silicon atoms ρ_{inc} per unit time increases with the partial pressure of the precursor gas; simply because more atoms hit the droplet surface per unit time. However, this relation can not hold in the limit of infinite precursor gas pressures. From some point on, the number of impinging precursor gas molecules and the number of resulting silicon atoms will be higher than what the droplet can incorporate at a time. The surface concentration of silicon atoms at the droplet surface will reach a point where the adsorption and cracking efficiency of the droplet starts to degrade. As a consequence, the incorporation rate of silicon atoms, expressed as a function of the precursor gas pressure, is expected to exhibit a maximum at high pressures.

One experimental observation that has not been discussed so far is the most unusual decrease of growth velocity with increasing temperature, shown in Fig. 2.2(d). However, considering that a temperature increase, similar to a pressure increase, increases the silicon supply (e.g. due to the higher $SiCl_4$ cracking efficiency), the analogy between the anomalous pressure dependence of Fig. 2.2(c) and the anomalous temperature dependence of Fig. 2.2(d) becomes apparent.

2.3 Theoretical Model

The first assumption of our model is that surface diffusion of silicon ad-atoms can be neglected. Furthermore, we assume that the diffusion of silicon through the liquid metal alloy droplet is sufficiently fast as not to influence the growth velocity, and that we can therefore concentrate on the interplay of the crystallization and incorporation rate, $\rho_{cry}(\mu^{ls})$ and $\rho_{inc}(p, \mu^{vl})$, respectively. We assume that the incorporation rate $\rho_{inc}(p, \mu^{vl})$ depends on both the pressure p and on the chemical potential difference between vapor and liquid, $\mu^{vl} = \mu^v - \mu^l$. The pressure dependence is caused by the pressure-dependent impingement of precursor molecules, whereas the μ^{vl} dependence is related to the cracking of the

precursor.

In addition, it is obvious that the incorporation rate ρ_{inc} is proportional to the droplet surface area, which in turn is proportional to the cross section area πr^2 of the nanowire. Thus dividing ρ_{inc} by the nanowire cross section area πr^2 should give a quantity, which does not directly depend on the nanowire radius. Additionally multiplying with Ω^s, the molar volume of solid silicon, defines the incorporation velocity

$$\alpha(p, \mu^{vl}) = \frac{\rho_{inc}(p, \mu^{vl})\Omega^s}{\pi r^2} \, . \tag{2.4}$$

We assume that the velocity $\alpha(p, \mu^{vl})$ is radius-independent for constant μ^{vl}. In a similar way, one can define the velocity $\omega(\mu^{ls})$

$$\omega(\mu^{ls}) = \frac{\rho_{cry}(\mu^{ls})\Omega^s}{\pi r^2} \, , \tag{2.5}$$

that reflects the crystallization process at the liquid-solid interface. Also $\omega(\mu^{ls})$ is assumed to be radius-independent for constant μ^{ls}. Under steady state conditions, it is clear that the ρ_{inc} has to equal ρ_{cry}, and we assume that the supersaturation μ^{ls} adjusts in a way to level both rates out. This value of μ^{ls} where both rates equal each other defines the steady state supersaturation $\Delta\mu$. In addition, it is obvious from the above definitions (2.4) and (2.5) that a steady state situation implies an equality of the above defined velocities α and ω. This defines the steady state growth velocity

$$v = \omega(\Delta\mu) = \alpha(p, \xi - \Delta\mu) \, , \tag{2.6}$$

where we used equation (2.3) to express μ^{vl} in terms of ξ and μ^{ls}. This situation is schematically depicted in Fig. 2.3, where $\omega(\mu^{ls})$ and $\alpha(p, \mu^{ls} - \xi)$ intersect at $\Delta\mu$. Note that in Fig. 2.3 $\alpha(p, -\mu^{vl})$ is plotted instead of $\alpha(p, \mu^{vl})$, which means that the α-curve is flipped with respect to the vertical-axis.

As discussed before, at not too high pressures the incorporation velocity $\alpha(p, \mu^{vl})$ is expected to increase with increasing pressure, or equivalently with increasing μ^{vl}. Due to the degradation of the adsorption efficiency, $\alpha(p, \mu^{vl})$ is assumed to exhibit a maximum; both if expressed as a function of p as well as if expressed as a function of μ^{vl}. This is the point, where the adsorption efficiency of the droplet surface starts to decrease. If μ^{vl} or the pressure is increased further, the incorporation velocity $\alpha(p, \mu^{vl})$ starts to decrease, as indicated by the experimental data of Fig. 2.2(c).

Figure 2.3 schematically depicts the incorporation velocity $\alpha(p, \mu^{ls} - \xi)$ and the crystallization velocity $\omega(\mu^{ls})$ as a function of the supersaturation μ^{ls}. The crystallization velocity $\omega(\mu^{ls})$ is assumed to be a monotonously increasing function of μ^{ls}. The grey curve in Fig. 2.3 is a schematic of the incorporation velocity $\alpha(p, \mu^{ls} - \xi)$ for a specific wire radius r_o. The intersection point of $\alpha(p, \mu^{ls} - \xi)$ and $\omega(\mu^{ls})$ defines the steady state growth velocity v_o and the steady state supersaturation $\Delta\mu_o$ for this radius r_o. If the radius is decreased from r_o to r, the α-curve is shifted to the left by an amount $\delta\xi = C^s/r_o - C^s/r$. Consequently also the position of the intersection point changes. The steady state growth

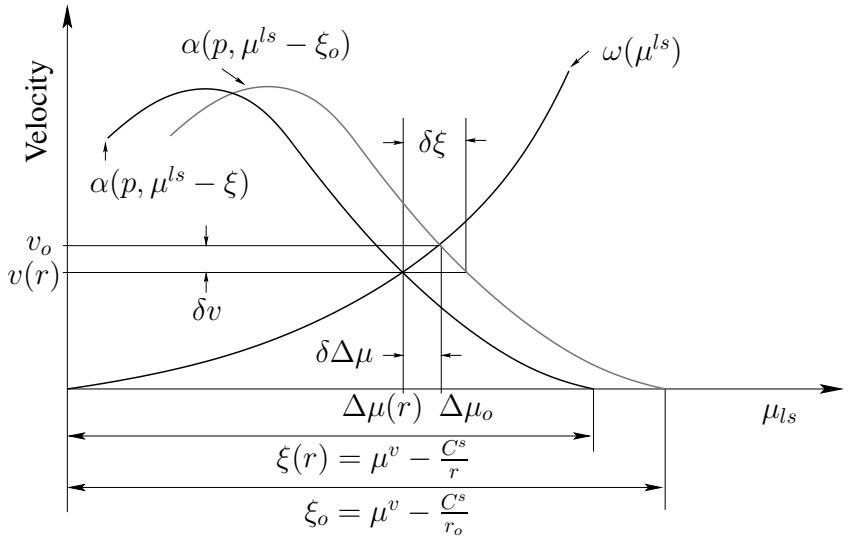

Figure 2.3: Schematic of the incorporation velocity $\alpha(p, \mu^{ls} - \xi)$ and the crystallization velocity $\omega(\mu^{ls})$ as a function of the droplet supersaturation nanowire μ^{ls}; $\alpha(p, \mu^{ls} - \xi)$ is given for two different radii, r_o (gray curve) and r.

velocity v and the supersaturation $\Delta\mu$ change by an amount δv and $\delta\Delta\mu$, respectively. If the shift $\delta\xi$ is sufficiently small, i.e. considering large radii, we can locally expand $\alpha(p, \mu^{ls} - \xi)$ and $\omega(\mu^{ls})$ in a Tailor series expansion to first order around the intersection point at $\mu^{ls} = \Delta\mu_o$

$$\omega(\mu^{ls}) = \omega_o + \omega_1 \cdot \left(\mu^{ls} - \Delta\mu_o\right) \tag{2.7}$$

$$\alpha(p, \mu^{ls} - \xi) = \alpha_o + \alpha_1 \cdot \left((\mu^{ls} - \Delta\mu_o) - (\xi - \xi_o)\right) . \tag{2.8}$$

Here $\alpha_1 = \partial\alpha/\partial\mu^{ls}|_{\mu^{ls}=\Delta\mu_o}$ and $\omega_1 = \partial\omega/\partial\mu^{ls}|_{\mu^{ls}=\Delta\mu_o}$ are the slopes at $\mu^{ls} = \Delta\mu_o$. Using the steady state conditions $\mu^{ls} = \Delta\mu$, $\omega_o = \alpha_o = v_o$, and $\omega(\Delta\mu) = \alpha(p, \Delta\mu - \xi)$ we can solve for the steady state supersaturation $\Delta\mu$

$$\Delta\mu = \Delta\mu_o - \frac{\alpha_1}{\omega_1 - \alpha_1}(\xi - \xi_o) \tag{2.9}$$

A good starting point for the expansion is the intersection point for infinite wire radius, because we already know that in this limit $\xi - \xi_o = -C^s/r$ and $\Delta\mu_o = \mu_o^l$. So we finally end up with the following expressions for the steady state supersaturation

$$\Delta\mu = \mu_o^l + \frac{\alpha_1}{\omega_1 - \alpha_1}\frac{2\Omega^s\sigma^s}{r} , \tag{2.10}$$

and the steady state growth velocity

$$v = v_o + \frac{\omega_1\,\alpha_1}{\omega_1 - \alpha_1}\frac{2\Omega^s\sigma^s}{r} . \tag{2.11}$$

One can see that finally both the steady state supersaturation and the steady state growth velocity becomes radius-dependent, and that in addition the steady state supersaturation

$\Delta\mu$ and the steady state growth velocity v depend on the slopes α_1 and ω_1. Regarding this, different cases have to be discussed.

Let is first concentrate on the limiting cases where either the incorporation or the crystallization step determines the growth rate. A scenario where only the incorporation rate determines the growth velocity corresponds to $\omega_1 \to \infty$. In this limit, the steady state supersaturation is radius-independent and the steady state growth velocity becomes $v = v_o + \alpha_1(2\Omega^s\sigma^s/r)$. Thus the growth velocity additionally depends on α_1. Considering the usual case where the incorporation rate increases with increasing pressure, i.e. $\alpha_1 < 0$, this leads to an increase of the growth velocity with increasing radius.

In the other limiting case, $\alpha_1 \to \infty$, corresponding to a situation where the crystallization step is rate determining, the steady state supersaturation becomes $\Delta\mu = \mu_o^l - 2\Omega^s\sigma^s/r$. This agrees with the result derived by Givargizov, see [Giv75]. Using equation (2.11), the steady state growth velocity in the limit $\alpha_1 \to \infty$ is given by $v = v_o - \omega_1(2\Omega^s\sigma^s/r)$. For $\omega_1 > 0$ this that the velocity would increase with increasing radius.

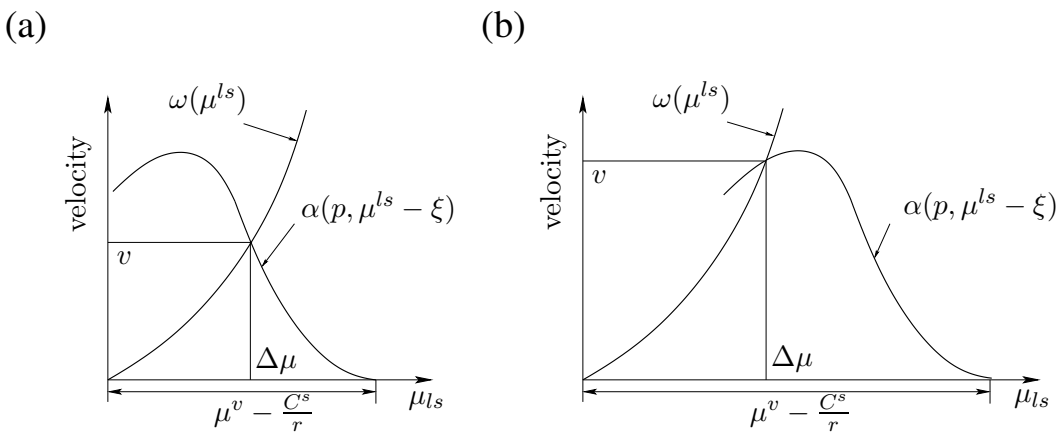

Figure 2.4: Two cases: (a) Case Nº 1, low pressure, small μ^v: $\alpha_1 < 0$, $\omega_1 > 0$, v increases with increasing radius. (b) Case Nº 2, high pressure, large μ^v: $\alpha_1 > 0$, $\omega_1 > \alpha_1 > 0$, v decreases with increasing radius

So both limiting cases, assuming $\alpha_1 < 0$ and $\omega_1 > 0$, would lead to an increase of the growth velocity with increasing radius. Hence the discussion which step is rate determining alone can not account for the complex behavior, shown in Fig. 2.2, where both a decrease and an increase of the growth velocity can be observed. The fact that both behaviors are observed has to do with the prefactor $\Gamma_v = (\omega_1\alpha_1)/(\omega_1 - \alpha_1)$ of the Gibbs-Thomson term in equation (2.11), which, depending on the signs and magnitudes of α_1 and ω_1, can be either positive or negative. Using this definition, the steady state growth velocity can be expressed as

$$v = v_o + \Gamma_v \frac{2\Omega^s\sigma^s}{r} \,. \tag{2.12}$$

With respect to the sign of Γ_v we can distinguish between two cases. The first case, $\alpha_1 < 0$ $\omega_1 > 0$, also shown schematically in Fig. 2.4(a), applies to nanowire growth at not too high

vapor pressures. The prefactor Γ_v is negative, thus the velocity increases with the radius, as indicated by the experimental results of Fig. 2.2(a) and Fig. 2.2(b). That the intersection point is indeed located on the right-hand side of the maximum of $\alpha(p, \mu^{ls} - \xi)$ can be deduced from the pressure dependence. The effect of a pressure increase on the growth velocity is twofold. One the one hand, a pressur increase, leads to an increase of the chemical potential of the vapor μ^v, which shifts the α-curve to the higher μ^{ls} values. If the intersection point, like shown in Fig. 2.4(a), is located on the right-hand side of the α-curve maximum, such a curve shift leads to an increase of the growth velocity. This effect should be even augmented by the direct pressure dependence of $\alpha(p, \mu^{ls} - \xi)$, which is caused by the pressure-dependent inpingement rate of precursor molecules. So we can expect an increase of the growth velocity with increasing pressure, which is consistent with the experimental results, presented in Fig. 2.2(a).

The second case, $\omega_1 > 0$ and $\omega_1 > \alpha_1 > 0$, applies to high growth pressure, and is shown schematically in Fig. 2.4(b). The prefactor Γ_v is positive in this case so that according to equation (2.12) the growth velocity should decrease with increasing radius, which can be seen in Fig. 2.2(c) or Fig. 2.2(d). Due to the high pressure, the α-curve is strongly shifted to the right, so that the intersection point can now be found on the left-hand side of the maximum. A pressure increase would shift the α-curve even further to the right, causing a further decrease of the growth velocity. Since the adsorption efficiency already started to degrade, the direct pressure dependence of $\alpha(p, \mu^{vl})$ should increase this effect, so that we can expect a decrease of the growth velocity with incresing pressure. The experimental data, presented in Fig. 2.2(c), exhibit exactly this anomalous kind of behavior.

To summarize briefly the above results, we can distinguish between two cases; the usual growth case, where the growth velocity increases with increasing pressure and increasing radius (see Fig. 2.4(a), Fig. 2.2(a),(b)); and the anomalous case, where both, a pressure and a radius increase lead to a decrease of the growth velocity (see Fig. 2.4(b), Fig. 2.2(c),(d)). Both cases can be conclusively explained in terms of our model.

Our model might also be applied to the case where the incorporation rate is independent of the supersaturation, i.e. $\alpha_1 \to 0$. As pointed out by Kodambaka et al. [Kod06] this might be the cause for the radius independence of the growth velocity, they observed in their experiments using disilane as precursor at very low pressures ($10^{-8} - 10^{-5}$ Torr). One can see from equation (2.11) that the radius dependence of the growth velocity indeed vanishes, if the incorporation rate is taken to be independent of the supersaturation ($\alpha_1 \to 0$).

One issue that has not been addressed so far is the maximum of the growth velocity that some of the experimental data sets, shown in Fig. 2.2(c) and Fig. 2.2(d), seem to exhibit at small radii. In order to understand this qualitatively, it is instructive to go one step beyond the linear approximation. We assume that the maximum of the α-curve is sufficiently smooth so that we can expand $\alpha(p, \mu^{ls} - \xi)$ to second order around the maximum located at $\Delta\mu_o$. In addition, we assume that a linear expansion gives a sufficiently accurate

description of $\omega(\mu^{ls})$ in the region close to the intersection point.

$$\omega(\mu^{ls}) = \omega_o + \omega_1 \cdot \left(\mu^{ls} - \Delta\mu_o\right) \tag{2.13}$$

$$\alpha(p, \mu^{ls} - \xi) = \alpha_o + \alpha_2 \cdot \left((\mu^{ls} - \Delta\mu_o) - (\xi - \xi_o)\right)^2 . \tag{2.14}$$

Using the steady state conditions $\mu^{ls} = \Delta\mu$, $\omega_o = \alpha_o$, and $\omega = \alpha = v$, we can eliminate $\Delta\mu - \Delta\mu_o$ and solve for the steady state growth velocity v

$$v(r) = v_o + \frac{\omega_1}{2\alpha_2}\left\{\omega_1 + 2\alpha_2\left(\frac{C^s}{r_o} - \frac{C^s}{r}\right) - \sqrt{\omega_1^2 + 4\alpha_2\omega_1\left(\frac{C^s}{r_o} - \frac{C^s}{r}\right)}\right\} . \tag{2.15}$$

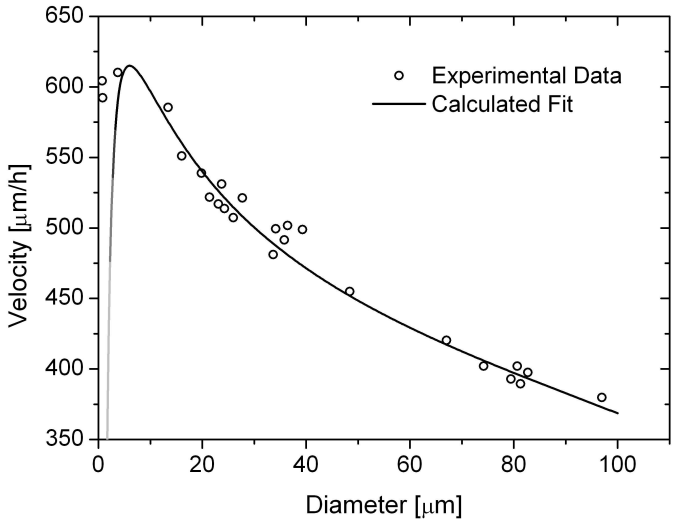

Figure 2.5: Dataset Nº 2 of Fig. 2.2(c) after Weyher [Wey78] and calculated fit using equation (2.15) and the following parameters: $C^s = 30\,\mathrm{J mol^{-1}}$ µm, $r_o = 3$ µm, $v_o = 615\,\mu\mathrm{m\,h^{-1}}$, $\omega_1 = 33.6\,\mu\mathrm{m\,h^{-1}\,mol\,J^{-1}}$, $\alpha_2 = -0.88\,\mu\mathrm{m\,h^{-1}\,mol^2\,J^{-2}}$, see also Fig. A.12.

In Fig. 2.5, the steady state growth velocity $v(r)$ is plotted together with the experimental dataset 2 of Fig. 2.2(c). Taking the material constants to be $\sigma = 1.24\,\mathrm{J\,m^{-2}}$ [Jac63] and $\Omega^s = 1.2 \times 10^{-5}\,\mathrm{m^3\,mol^{-1}}$ leads to $C^s = 30\,\mathrm{J mol^{-1}}$ µm. Assuming that according to Fig. 2.2(c) the maximal growth velocity of $v_o = 615\,\mu\mathrm{m\,h^{-1}}$ is located at $r_o = 3\,\mu$m, we can find best agreement with the experimental data for the following fit parameters: $\omega_1 = 33.6\,\mu\mathrm{m\,h^{-1}\,mol\,J^{-1}}$, $\alpha_2 = -0.88\,\mu\mathrm{m\,h^{-1}\,mol^2\,J^{-2}}$. Like the α-curve, the calculated steady state velocity also exhibits a maximum, which could be expected, since we are somehow probing the α-curve with the steeper ω-curve. For radii greater than r_o the calculated steady state growth velocity of Fig. 2.5 is in good agreement with experiment, which underscores the validity of our model. Only for radii smaller than r_o the calculated velocity curve shows a sharp decrease and does not reproduce the experimental data. This is because in deriving equation (2.15), we assumed that we can approximate the α-curve

in the vicinity of its maximum by a parabola. However, due to the $1/r$ dependence of the supersaturation, this approximation becomes invalid if the radius is consideraby smaller than r_o. This decreased validity of equation (2.15) is indicated in Fig. 2.5 by the fading out of the curve.

Furthermore note that our results cannot be directly applied to growth experiments, where, due to surface diffusion for example, the silicon supply is by itself strongly radius dependent [Sei04, Sch04, Joh05].

2.4 Conclusions of Chapter 2

To conclude, considering the silicon incorporation process at the droplet surface, the crystallization process at the liquid-solid interface, and the Gibbs-Thomson effect, we derived expressions for the radius dependence of the steady state growth velocity v. Our model showed, that the diameter dependence of this velocity v is not determined by material constants alone, as expected from the Gibbs-Thomson effect, but in addition also depends on the derivatives α_1 and ω_1 of the incorporation and crystallization velocities α and ω with respect to the supersaturation μ^{ls}. These derivatives α_1 and ω_1 give an additional prefactor to the Gibbs-Thomson term, which strongly influences the radius dependence of the steady state growth velocity. The seemingly contradictory experimental observations can be explained by a sign change of this prefactor, caused by a sign change of α_1. A sign change of α_1 does not only affect the radius, but also the pressure dependence of the growth velocity. Thus a consistent explanation could also be given to the phenomenon that an anomalous pressure dependence of the growth velocity coincides with an anomalous radius dependence.

Chapter 3

Expansion of the Nanowire Base and the Influence of the Line Tension

The previous chapter gave account of the diameter dependence of the growth velocity, or the length, of silicon nanowires. This chapter somehow treats the reverse subject: the diameter of silicon nanowires grown epitaxially via the vapor-liquid-solid (VLS) mechanism as a function of the nanowire length. It is found that the diameter, instead of being constant over the entire length of the nanowire, is larger at the nanowire base, where the nanowire is attached to the substrate. We will show that this expansion of the nanowire base is a direct consequence of the VLS growth mechanism and that it results from the balance of forces acting on the liquid catalyst droplet. Considering the equilibrium condition for the contact angle of the droplet, we will derive a model for epitaxial silicon nanowire growth via the VLS mechanism that can be used to numerically calculate the shape of this expansion [Sch05c]. In addition, our model also considers the line tension of the triple-phase line and its effect on the final nanowire shape.

3.1 Introduction

It has often been stated that the diameter of the nanowires grown via the VLS mechanism is determined by the size of the droplet. This is undoubtedly true, but it does not necessarily imply that the diameter of the nanowire is constant. In fact, the diameter of epitaxially grown silicon nanowires is larger close to where they are attached to the substrate [Wag65, Shc90, Neb96, Wak99]. One first guess would be that this larger diameter is simply created by an overgrowth of the nanowire. However, an overgrowth alone does not provide a sufficient explanation for the observed phenomenon, for two reasons. The first reason, also put forward by Givargizov [Giv87c], is that the phenomenon of a larger diameter of the nanowire base occurs independently of the growth temperature. An overgrowth requires the supply of silicon, either directly from the vapor and/or by surface diffusion. Both mechanisms are strongly temperature dependent. Thus the diameter enlargement of the nanowire base should be considerably reduced at lower temperatures,

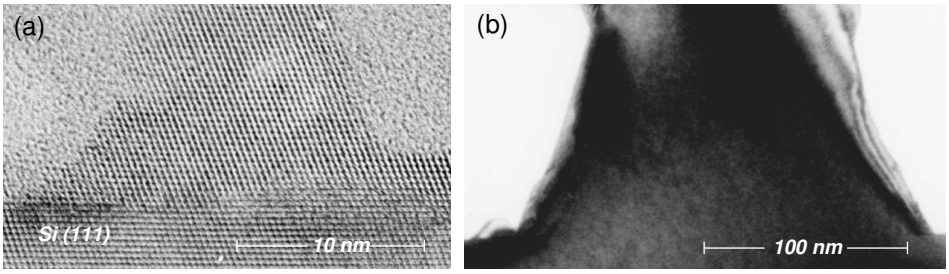

Figure 3.1: (a) HR-TEM image of the nanowire base. (b) TEM image of the nanowire base

which is not the case. The second reason is that the diameter enlargement of the nanowire base scales with the diameter of the nanowire. This can be seen in Fig. 3.1. Figure 3.1 (a) shows a high-resolution cross-section transmission electron micrograph of one thin silicon nanowire grown epitaxially on a (111) oriented silicon substrate. Within a distance of about twice the nanowire diameter, the diameter expands by almost a factor of two. A similar behavior can be seen Fig. 3.1(b), which shows a transmission electron micrograph of the base of a nanowire with much larger diameter. Although both nanowires are grown under similar growth conditions, the expansion of the nanowire base is of totally different magnitude in absolute numbers, but comparable, if expressed in units of the nanowire diameter. If in contrast, the diameter increase at the nanowire base were only due to an overgrowth of the nanowire, one would expect the absolute magnitude of the expansion to be more or less diameter-independent. These arguments show that the larger base diameter can not be explained by an overgrowth of the nanowire alone. Nevertheless, surface diffusion and vapor-solid growth do have a certain influence on the shape of the nanowire expansion [Wag67]. A faceting of the nanowire base expansion, for example, is often observed, especially at elevated temperatures [Wey78, Tho66].

3.2 Surface Thermodynamics

Before actually deriving our model, let us first take a look at the initial conditions of silicon nanowire growth. We assume that the silicon nanowires are grown vertically on a flat silicon surface, that gold is used as the catalyst material, and that growth takes place via the VLS mechanism. Nanowire growth starts from a Au/Si alloy droplet, sessile on the silicon surface, so that the initial conditions for growth are determined by the properties of this Au/Si alloy droplet. A scanning electron micrograph of Au/Si droplets on a flat silicon surface is shown in Fig. 3.2(a). One can see that the sessile droplet is relatively flat, the contact angle, though temperature dependent, being about 45° [Res03]. The contact angle of a sessile droplet on a flat surface (see Fig. 3.2(b)) is determined by the balance of forces, as schematically shown in Fig. 3.2(c). Here σ_l, σ_{ls}, and σ_s are the surface tension of the droplet surface, the liquid-solid interface tension, and the silicon surface tension, respectively. The droplet has a contact area of radius r_0 and a contact angle β_0. The curvature radius R of the droplet can be expressed as $R = r_0/\sin(\beta_0)$. The only way

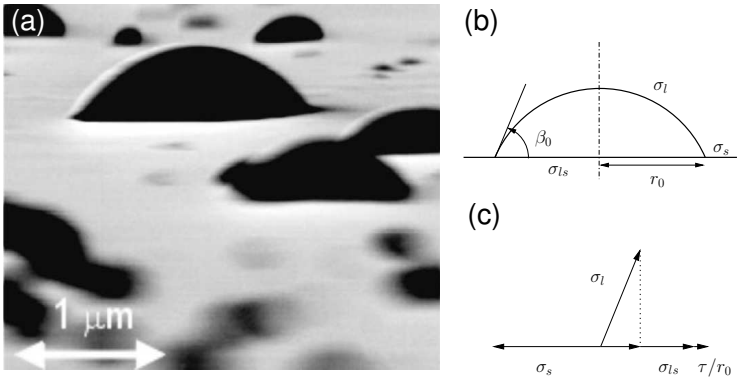

Figure 3.2: (a) Scanning electron micrograph [Res03] of Au/Si eutectic droplets on Si at 400 °C. (b) Schematic of a Au/Si-eutectic droplet sessile. (c) Surface forces and their horizontal components; r_0=interface radius, β_0=contact angle, σ_l=liquid surface tension, σ_{ls}=liquid-solid interface tension, σ_s=solid surface tension, τ=line tension.

the Au/Si alloy droplet, as it is shown in Fig. 3.2(b), can equilibrate is by increasing or reducing its radius r_0. In equilibrium, the droplet is expected neither to expand, nor to shrink, which means that the horizontal components of the surface forces created by the surface tensions, and the line tension have to cancel out. This is schematically depicted in Fig. 3.2(c). This condition of a vanishing horizontal force component relates the contact angle β_0 to the surface tensions and the line tension τ, leading to the modified Young's equation [Row02a]

$$\sigma_l \cos(\beta_0) = \sigma_s - \sigma_{ls} - \frac{\tau}{r_0} \,. \tag{3.1}$$

It is called modified, because a line tension contribution has been added to Young's equation, as suggested by Pethica [Pet61] and Widom [Wid95]. The idea of a line tension was first brought up about hundred years ago by J. W. Gibbs [Gib61]. He pointed out that the contact line, where three phases meet, can be treated alike a dividing surface between two phases, and that correspondingly a specific line energy must be assigned to this contact line. A surface tension is defined as the excess free energy per unit area of the dividing plane separating two phases. Analogously, the line tension is defined as the excess free energy per unit length of the dividing line separating three separate phases. The only place, where in our case three phases meet, is the outer rim of the droplet. Here the liquid, the solid, and the vapor phase define the triple phase line.

If the problem of a droplet on a flat surface is to be described in the most general way, a line tension contribution has to be taken into account. However, as the line tension is proportional to r_0^{-1}, i.e. to the curvature of the triple phase line, it is usually neglected if macroscopic systems are considered. The absolute value of the line tension is estimated to be between $1{\times}10^{-11}$ J m^{-1} and $1{\times}10^{-9}$ J m^{-1} [Row02b]. In contrast to the surface tension, which can only take positive values, the line tension can either be positive or negative. The reason is that a negative surface tension would give a non-physical solution. An increase of the surface area would reduce the energy, such that the equilibrium solution of the problem

would literally explode. This is not the case for a negative line tension, because an increase of the length of the triple-phase line is accompanied by an increase of the surface area. For small line tension values, the positive surface tensions will over-compensate the negative line tension contribution, so that the solution itself remains physical.

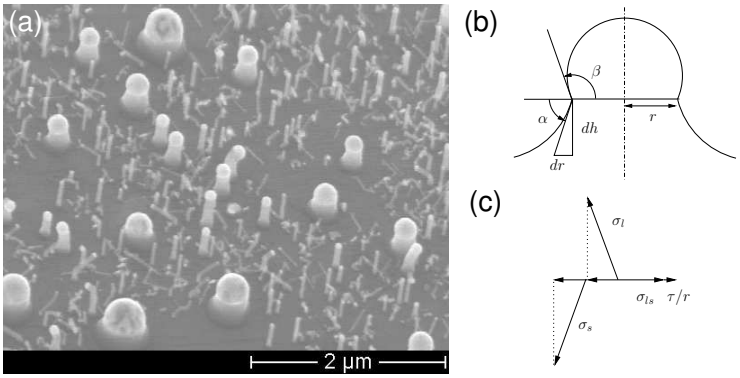

Figure 3.3: (a) Scanning electron micrograph of nanowires in the initial stage of growth. (b) Schematic of the initial stage of nanowire growth. (c) Surface forces and their horizontal component; r=interface radius, β=contact angle, σ_l=liquid surface tension, σ_{ls}=liquid-solid interface tension, σ_s=solid surface tension, τ=line tension.

In the initial stage of VLS silicon nanowire growth, the shape of the catalyst droplet changes. A SEM image of silicon nanowires in their initial stage of growth is shown in Fig.3.3(a). It can readily be seen that the droplets, sitting on the short and tapered nanowire stumps, are much more spherical then the ones of Fig. 3.2(a). In Fig. 3.3(b) a nanowire in its initial growth stage is schematically depicted. Together with the inclination angle α of the nanowire flank, also the force-balance for the droplet changes, as the contribution of the silicon surface tension to the force balance relation is now proportional to $\cos(\alpha)$, see Fig. 3.3(c). Equation (3.1) thus transforms into

$$\sigma_l \cos(\beta) = \sigma_s \cos(\alpha) - \sigma_{ls} - \frac{\tau}{r} \,. \tag{3.2}$$

This is the so-called Neumann quadrilateral relation [Che96], which relates the contact angle β to the surface tensions, the line tension τ and the inclination angle α. In the limit $\alpha \rightarrow 0$ equation (3.2) of course becomes equal to equation (3.1). In our case, where the nanowires are grown on a flat substrate, α equals zero at the beginning. As growth starts, the angle α has to increase. By considering (3.2) it becomes immediately clear that an increase of α is accompanied by an increase of β, which means that the droplet becomes more spherical. Yet, this causes a decrease of the contact area and a decrease of the nanowire radius r. Consequently, the radius of the nanowire becomes smaller as it grows; or in other words, the nanowire shows an expansion at its base.

3.3 Quasi-static Growth Model

In order to give a mathematical description of this development of the droplet, we have to make some simplifying assumptions. We assume that the nanowires have a circular cross section and that the volume of the Au/Si alloy droplet is constant during growth. This neglects the loss of gold by dissolution, evaporation, or surface diffusion. In addition, the shape of the droplet is taken to be a segment of a sphere. The volume V of the Au/Si-eutectic droplet can then be expressed in terms of the contact angle β and the radius r.

$$V = \frac{\pi}{3}\left(\frac{r}{\sin(\beta)}\right)^3 (1-\cos(\beta))^2\,(2+\cos(\beta_0))\ . \tag{3.3}$$

Solving for r gives the radius of the contact area as a function of the contact angle β and the volume V,

$$r(\beta) = \left(\frac{3\,V}{\pi}\right)^{1/3} \frac{(1+\cos(\beta))^{1/2}}{(1-\cos(\beta))^{1/6}\,(2+\cos(\beta))^{1/3}}\ . \tag{3.4}$$

Additionally, we can make use of the fact that the inclination angle α of the nanowire flank, as indicated in Fig. 3.3(b), can also be expressed as

$$\tan(\alpha) = -\frac{dh(r)}{dr}\ . \tag{3.5}$$

The minus sign in (3.5) arises since a decrease of the radius leads to an increase of $\tan(\alpha)$. This differential equation can directly be solved by integration, leading to an expression for the nanowire height as a function of the inclination angle

$$h(\alpha') = -\int_0^{\alpha'} \tan(\alpha)\left(\frac{dr}{d\alpha}\right) d\alpha\ . \tag{3.6}$$

The derivative in the integrand above is easily found by using (3.2) and (3.4). Of course, the above expression for $h(\alpha)$ implicitly assumes that the physical process of growth proceeds as long as the equilibrium conditions for the droplet allow it. This means that the supply of silicon for the growth of the silicon nanowire is ensured, but that the growth velocity is small enough that the droplet can maintain its equilibrium shape. In a way, our growth model is a quasi-static model, since we do not employ kinetic aspects or time dependent quantities. It is as much an analysis of the droplet shape as a model for nanowire growth. The advantage of this approach is that it minimizes the number of unknowns.

The only unknowns, necessary to model the shape of the silicon nanowire, are the values of the surface tensions and the line tension. Suppose σ_l, the surface tension of the droplet, is approximately given as $0.85\ \mathrm{Jm}^{-2}$ [Nai75] and the specific surface energy of the (111) silicon surface $\sigma_s \approx 1.24\ \mathrm{Jm}^{-2}$ [Jac63], then knowledge of the contact angle $\beta_0 \approx 43°$ [Res03] of a macroscopic droplet (the line tension is effectively zero) leads to a liquid-solid interface tension $\sigma_{ls} \approx 0.62\ \mathrm{Jm}^{-2}$. Both the surface tensions and the line tension are taken to be isotropic. Yet, an extension of the model to allow for anisotropy effects seems to be possible. Unfortunately, reliable data on the value of the line tension τ are not available. Hence the line tension τ is left as a free parameter.

3.4 Results and Discussion

To keep the following considerations as concise as possible, a set of dimension-less variables shall be introduced here, viz a dimension-less surface tension, $\sigma_s' \equiv \sigma_s/\sigma_l$, a dimension-less interface tension, $\sigma_{ls}' \equiv \sigma_{ls}/\sigma_l$, and a dimension-less line tension, $\tau' \equiv \tau/(r_0\sigma_l)$. Note that the dimension-less line tension scales inversely with the initial contact radius of the droplet, leading to a vanishing line tension contribution for macroscopic droplets. The

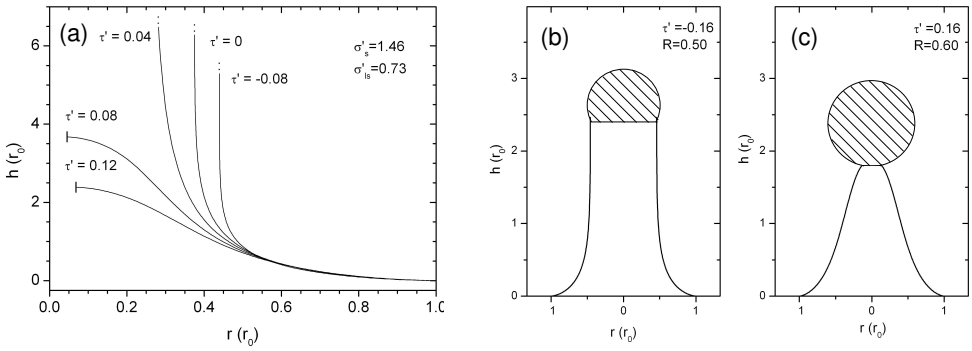

Figure 3.4: (a) Silicon nanowire shape for various line tension values τ', see also Fig. A.13; (b-c) Calculated nanowire shapes for $\sigma_{ls}' = 0.73$ and $\sigma_s' = 1.46$: (b) normal nanowire growth, $\tau' = -0.16$; (c) hillock growth, $\tau' = +0.16$. The gray shaded areas represent the Au/Si-eutectic droplets having the radius R.

aforementioned surface tension values give $\sigma_s' = 1.46$ and $\sigma_{ls}' = 0.73$. Using these values, together with equations (3.2) and (3.4), a numerical evaluation of the integral in (3.6) then gives the height h as a function of the radius r. This function, i.e. the shape of the right flank of a silicon nanowire, is depicted for some values of τ' in Fig. 3.4(a), where both the height and the radius are expressed in units of r_0. One can see in Fig. 3.4(a) that there are two different growth modes present. Real nanowire growth takes place for line tension values being moderately positive, zero, or negative. The radius of the nanowire shrinks within a finite height from r_0, the initial droplet radius, to a radius close to the final radius r_{fin} of the nanowire. In Fig. 3.4(a) the shape of the right flank of a real nanowire is drawn for three different line tension values; $\tau' = 0.04$, $\tau' = 0$, and $\tau' = -0.08$. One can see that the transition from the initial stage to a growth with an almost constant radius $r \approx r_{fin}$ gets sharper the more negative the line tension becomes. The other growth mode, shown in Fig. 3.4(a) for $\tau' = 0.08$ and $\tau' = 0.12$, corresponds to the growth of hillock-like structures of finite height.

In order to give a more clear impression of the two growth modes, both are depicted in Fig. 3.4(b-c). The nanowire growth mode is shown in Fig. 3.4(b); the hillock growth mode is displayed in Fig. 3.4(c). Note that in Fig. 3.4(b) and Fig. 3.4(c) both contours correspond to the calculated shapes. The schematically indicated Au/Si alloy droplets on top of the nanostructure have been added using the calculated value for the droplet radius

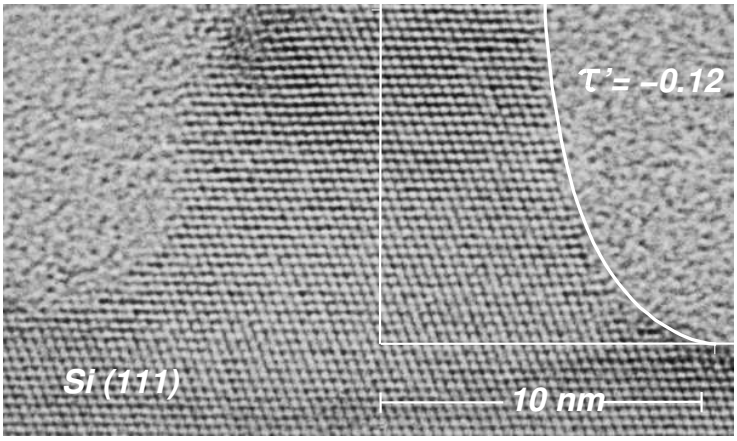

Figure 3.5: High resolution transmission electron micrograph of an epitaxially grown silicon nanowire. White line: calculated shape for $\tau' = -0.12$, $\sigma'_{ls} = 0.73$, and $\sigma'_s = 1.46$.

R. In order to compare the calculated nanowire shapes to experimental results, a high resolution transmission electron micrograph (JEM-4010) of the base of a silicon nanowire is shown in Fig. 3.5. The nanowire in Fig. 3.5 has been produced by chemical vapor deposition in ultra high vacuum environment via the VLS growth mechanism using gold as catalyst and diluted silane (5% in argon) as precursor gas. The gold was in situ deposited as a film of 0.2 nm thickness onto a hydrogen-terminated (111)-oriented silicon wafer and subsequently annealed at 300 °C for 30 minutes. Nanowire growth took place at a temperature of around 400 °C at a silane partial pressure around 10 Pa. The transmission electron micrograph of Fig. 3.5 also clearly shows the epitaxial relation between the (111)-oriented substrate and the nanowire. The white curve on the right flank of the nanowire is the calculated shape of the nanowire base for $\sigma'_s = 1.46$, $\sigma'_{ls} = 0.73$, and $\tau' = -0.12$. It is in perfect agreement with the experimentally observed shape. Taking r_0 to be around 10 nm, the value of $\tau' = -0.12$ leads to an estimate for the line tension $\tau \approx -1 \cdot 10^{-9}\text{Jm}^{-1}$. However, it must be emphasized here that this is only a crude estimate for the line tension and that the errors of this estimate are extremely high. Nevertheless, it shows that the value of the line tension can in principle be determined that way.

Coming back to the model, we have seen in Fig. 3.4(a-b) that there are two growth modes present. One corresponds to real nanowire growth (Fig. 3.4b) and the other one leads to the growth of hillock-like structures (Fig. 3.4c). The transition from the nanowire to the hillock growth mode takes place if the line tension exceeds a certain positive upper limit τ'_{up}. This can be understood intuitively by considering that a positive line tension means that the energy of the system can be reduced by a shrinkage of the liquid-solid interface area. If the value of the line tension is too large, the impetus for a shrinking of the interface area becomes so strong that regular nanowire growth with constant radius becomes impossible. Instead, a further shrinkage of the contact area is preferred, which then leads only to the growth of the hillock-like structures, shown for example in Fig. 3.4c. Note that the inclination angle α goes to zero as the height approaches its final value,

whereas the diminishing of the radius stops at a small but non-zero value. This is denoted in Fig. 3.4(a) by a vertical bar at the end of the curve. That the radius does not go to zero is reasonable, since a small contact area to where the Au/Si-eutectic droplet is attached, has to be left. It should be mentioned here that a system with a droplet, which is connected by such a small contact area is mechanically not very stable, and that it is not unlikely that the droplet may become disconnected from its base by minor mechanical forces.

The mathematical reason for one or the other growth mode to be realized, lies in the divergence of the integral in (3.6), or better in the divergence of $\tan(\alpha)$ in the integrand, as $\alpha \to \pi/2$. This is equivalent to the condition that $\cos(\alpha) = 0$ for $r = r_{fin}$, where $\cos(\alpha)$ is constrained by (3.2). If the line tension is positive and exceeds a certain limit τ'_{up}, the divergence of the integral disappears. The condition $\cos(\alpha) = 0$ can not be fulfilled any more, the integral remains finite, and growth stops at a finite height. The interesting question is now at which line tension value τ'_{up} does this transition take place. A short calculation gives the approximate solution

$$\tau'_{up} \approx \frac{2(1-\sigma'_{ls})^{3/2}}{3^{3/2}(1+\sigma'_s-\sigma'_{ls})^{1/2}} \,. \tag{3.7}$$

Taking the silicon values $\sigma'_s = 1.46$ and $\sigma'_{ls} = 0.73$ gives a $\tau'_{up} \approx 0.04$, which is in agreement with the results shown in Fig. 3.4(a). For a nanowire having a radius of 10 nm this would correspond to a line tension $\tau \approx 3 \cdot 10^{-10}\mathrm{Jm}^{-1}$; a relatively small value. It seems possible that such a small line tension value can be exceeded, with the consequence that a normal nanowire growth would be suppressed.

Especially for the growth of doped silicon nanowires by addition of dopant atoms to the Au/Si-eutectic droplet, the transition of one growth mode to the other might be relevant. Since the dopants are known to be surface active substances, they presumably also influence the value of the line tension. A change of shape of silicon nanowires upon the addition of dopant gases was indeed observed by Givargizov [Giv75], who reports on the periodic instability of silicon nanowires. He found that this periodic instability diminishes upon the introduction of arsine or phosphine during nanowire growth. This might possibly also explain our observation that silicon nanowires, although usually grown without difficulties on lowly doped silicon wafers, did not grow properly on highly doped silicon wafers (both p and n-type, resistivity of the order $10^{-3}\Omega$cm). The dopants, boron and arsenic, might have induced an increase of the line tension τ' over the upper limit, causing the transition to the hillock growth mode. Indeed, only short, strongly tapered nanowires could be found on the wafer surface.

Although our discussion so far concentrated on the case of gold as catalyst, our model is not principally restricted to this. Yet, different catalysts imply different surface, interface, and line tension values. Therefore, the influence of a variation of these parameters on the shape of the nanowires is of interest. The nanowires are characterized by their final radius r_{fin}, i.e. the radius at infinite height.

In Fig. 3.6(a) this characteristic parameter r_{fin} in units of r_0 is plotted as a function of the line tension τ' for various values of σ'_s. The dimension-less interface tension $\sigma_{ls} = 0.73$ is kept constant at the value of the gold-silicon system. One can see that for each curve both

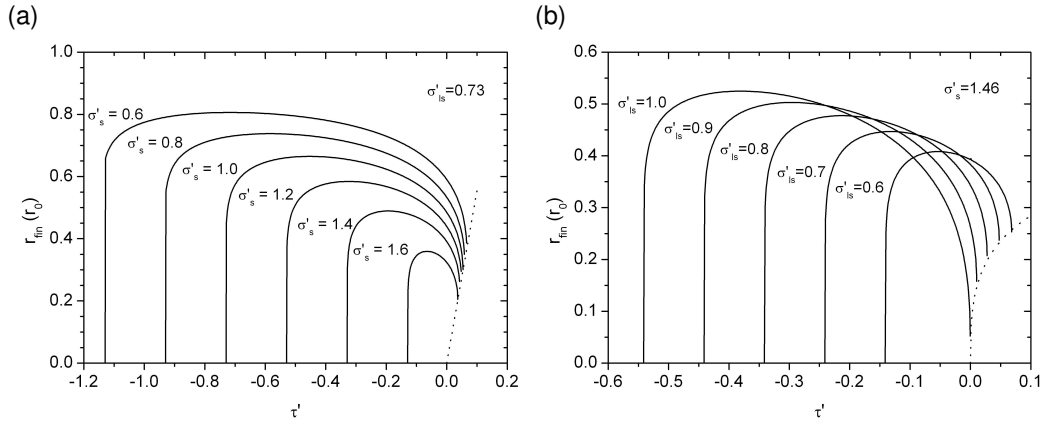

Figure 3.6: (a) Final nanowire radius r_{fin} as a function of the line tension τ' for $\sigma'_{ls} = 0.73$ and various σ'_s values, see also Fig. A.14. (b) Final nanowire radius r_{fin} as a function of the line tension τ' for $\sigma'_s = 1.46$ and various σ'_{ls} values, see also Fig. A.15.

an upper and a lower line tension boundary exists, within which a positive and finite final nanowire radius r_{fin} can be found. The value of r_{fin} is zero at the lower boundary and increases with increasing line tension till it reaches a maximum value. A further increase of the line tension leads to a decrease of r_{fin}, which ends at the upper line tension boundary τ'_{up}. The lower boundary τ'_{lo} is located at the negative line tension $\tau'_{lo} = \sigma'_s - \sigma'_{ls} - 1$. The fact that the final radius r_{fin} (in units of the initial radius r_0) becomes zero, means that the expansion at the base becomes wider and wider. A line tension value below the lower limit, $\tau'_{lo} = \sigma'_s - \sigma'_{ls} - 1$, would cause a complete spreading of the initial droplet over the substrate, that is $r_0 \to \infty$. The upper boundary τ'_{up} is the more interesting one, because it is smaller in magnitude, and this increases the probability that this boundary might be also experimentally relevant. Interestingly, the final nanowire radius r_{fin} does not become zero at the upper boundary. It can be shown that to a good approximation all of the r_{fin} values at the upper boundary lie on a straight line going through $\tau' = 0$ and having a slope $(3/2)(1-\sigma'_{ls})^{-1}$. This straight line is depicted in Fig. 3.6(a) as a dashed line. Line tension values beyond this dashed line lead to the hillock growth mode, discussed before.

The effect of a variation of σ'_{ls}, the dimensionless liquid-solid interface tension, is considered in Fig. 3.6(b). Here, the final nanowire radius r_{fin} is plotted for various σ'_{ls} with the surface tension σ'_s kept constant. One can see that the final radius r_{fin} of the nanowire is increasing for increasing σ'_{ls}, but that the general behavior remains the same. For all values a lower and an upper line tension boundary exists. Similar to the situation shown in Fig. 3.6(a), the values of r_{fin} at the upper boundary are approximately located on a smooth curve, depicted in Fig. 3.6(b) as a dashed line, which is given by $(3/2)((4\tau')^{1/3} - \tau')(2 + \sigma'_s - \tau')^{-1}$. So we have to conclude that neither a variation of σ'_s nor of σ'_{ls} does substantially affect the general behavior. An upper boundary close to $\tau' = 0$ exists, for which nanowire growth is suppressed if the line tension exceeds the boundary.

3.5 Conclusions of Chapter 3

In conclusion we have shown that by considering the equilibrium condition for the contact angle of the droplet, i.e. the Neumann quadrilateral relation, a quasi-static growth model was derived. The model explains the origin of the diameter expansion of the base of the nanowire, which has been observed experimentally. By comparing the calculated shape of this expansion with experimental results, an estimate for the line tension was obtained. Furthermore, the model predicts that proper nanowires can only be synthesized for a certain range of line tension values. Analytic expressions for the upper and lower boundaries limiting this range have been given. In addition, the effect of a variation of the interface and surface tension values on the nanowire growth has been discussed.

Chapter 4

Diameter Dependence of the Growth Direction

The crystallographic growth direction is a parameter of paramount importance for the integration of epitaxially grown silicon nanowires into possible future devices, since an arbitrary growth direction renders a processing of the nanowires difficult, if not impossible. We will show in this section that the growth direction is diameter-dependent. Although the influence of different factors on the growth direction is not fully understood yet, we propose a model for the diameter dependence of growth direction. In our model, the different scaling properties of specific surface and interface energies cause the change in the growth direction [Sch05a].

4.1 Introduction

It is known since the nineteen sixties that silicon nanowires grown by chemical vapor deposition with gold as catalyst and diameters greater than 100 nm tend to grow in the $<111>$ direction [Wag64a]. In addition to the $<111>$ direction, also the $<110>$ [Giv71, Cui01a], the $<112>$ [Giv75, Oza98], and even the $<100>$ direction [Lew02, Sha04] has been observed for silicon nanowires. Frequently, $<111>$, $<110>$, and $<112>$ oriented nanowires are found in our experiments. Furthermore, the experimental results presented in this chapter demonstrate that the growth direction of epitaxially grown silicon nanowires changes with the nanowire diameter from $<111>$ to $<110>$, similarly as it had earlier been observed for non-epitaxial silicon nanowires [Wu04a].

We investigated the growth direction of silicon nanowires, grown epitaxially on a (100) oriented silicon wafer (p-doped with boron, $5 - 20\,\Omega\,\mathrm{cm}$). As described before, the wafer is cleaned by a two-step wet chemical cleaning procedure (RCA), and dipped afterwards into diluted hydrofluoric acid to obtain a clean hydrogen-terminated silicon surface. After hydrophobically pre-bonding pairs of wafers, the wafer pairs are immediately transferred into the UHV system. As catalyst for the VLS growth of the silicon nanowires we deposited a 0.3 nm thick layer of gold onto the hydrogen-terminated surface of the silicon, which is

afterwards annealed in situ at 400 °C for ten minutes. After the annealing, nanowire growth is initiated at this temperature by switching on the precursor gas, diluted silane (40 sccm of 5% silane in argon). After a few minutes a total pressure of about 2 mbar is reached in the growth chamber. Pressure and silane flow are kept constant for six minutes, during which nanowire growth takes place.

4.2 Results and Discussion

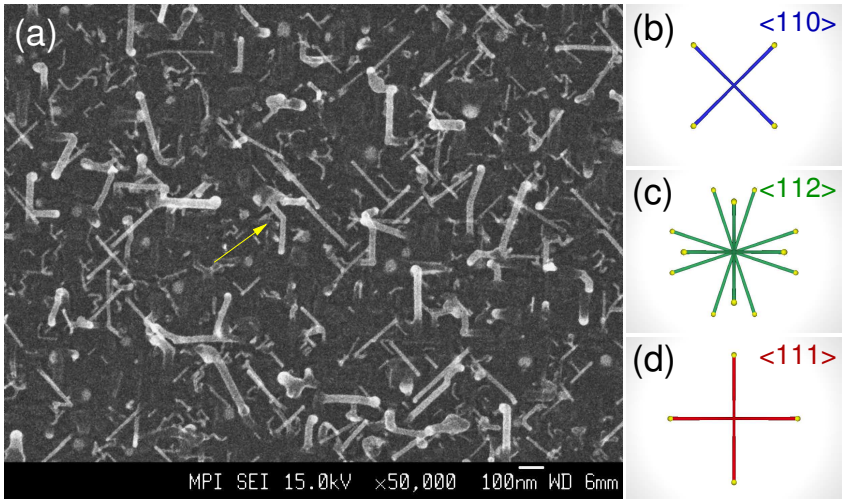

Figure 4.1: (a) Top view scanning electron micrograph of nanowires grown on a silicon (100) substrate. (b) Schematic top view image of <110> oriented nanowires on a (100) substrate of the same azimuthal orientation as in (a). (c) Schematic top view image of <112> oriented nanowires on a (100) substrate of the same azimuthal orientation as in (a). (d) Schematic top view image of <111> oriented nanowires on a (100) substrate of the same orientation as in (a).

Figure 4.1 (a) shows a typical top view scanning electron micrograph (JEOL JSM 6340 F) of a sample processed in the aforementioned way. Clearly, the SEM image exhibits three different kinds of nanowires. First, the ones pointing at $\pm 18^\circ$ with respect to the horizontal or vertical image axis of Fig. 4.1(a). As depicted schematically in Fig. 4.1(c), these nanowires are unambiguously <112> oriented. The second group that can be identified are the <110> oriented nanowires. These are growing at $\pm 45^\circ$ with respect to the horizontal image axis (see Fig. 4.1(b)). Furthermore, one can immediately recognize that their diameter is relatively small. As for the third kind, the ones observed horizontally or vertically in the projection plane, the situation is more complicated. Considering the schematic drawings shown in Fig.4.1(c) and Fig.4.1(d) it is apparent that these could either be <211> or <111> oriented. So in this case we get a mixed distribution. Suppose the number density is identical for the different possible <112> directions, the pure <111> distribution can be deduced by subtracting the <112> contribution obtained in the beginning. For a better understanding of the spatial orientation of the nanowires, a schematic 3D side view

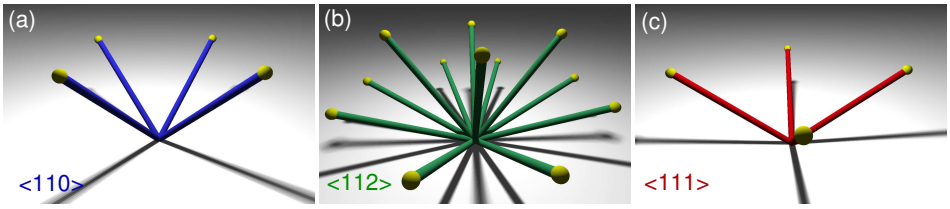

Figure 4.2: (a) Schematic side view of $<110>$ oriented nanowires grown on a (100) substrate. (b) Schematic side view of $<112>$ oriented nanowires grown on a (100) substrate. (c) Schematic side view of $<111>$ oriented nanowires grown on a (100) substrate. The viewing direction is $[\bar{1}\bar{1}\bar{1}]$ in all three images.

of the different growth directions is shown in Fig. 4.2. Figure 4.2 (a) and Fig. 4.2(c) show the four possible $<110>$ or $<111>$ growth directions, respectively. In Fig. 4.2(b) the twelve possible $<112>$ growth directions are displayed.

The resulting size distributions of the $<110>$, $<112>$, and $<111>$ oriented nanowires obtained by analyzing top view SEM images, are depicted in Fig. 4.3. Here it can be seen that for diameters smaller than 20 nm the $<110>$ direction is preferred. However, for diameters larger than 30 nm the $<111>$ direction becomes dominant. Especially by considering the relative proportion of the different directions, shown in the inset of Fig. 3, it becomes apparent that a transition between the $<111>$ and the $<110>$ orientation takes place at a crossover diameter $d_c = 2\,r_c$ of approximately 20 nm. In the diameter range around this crossover diameter also the $<112>$ orientation is present, but since it mainly appears in this intermediate range it will not be discussed in detail.

These size distributions agree surprisingly well with the results of Wu et al. [Wu04a] for non-epitaxial silicon nanowire growth, which is interesting from a nucleation point of view. Their nanowires, grown on amorphous SiO_2, experienced totally different nucleation conditions. We therefore assume that the nanowire nucleation cannot be the cause for the diameter dependence of the nanowire growth direction. This assumption is underscored by a nanowire, marked in Fig. 4.1(a) with a yellow arrow, that changes its growth direction from $<110>$ to $<111>$, or $<112>$, respectively. We will see later on that this direction change is consistent with a minimization of the overall interface energy between droplet and nanowire.

It should be remarked here, that there are indications that under certain conditions, the nanowire nucleation has a non-neglectable influence on the growth direction of the nanowires. Krishnamachari et al. [Kri04] observed that the crystallographic orientation of InP nanowires on InP substrate is strongly affected by the pretreatment of the Au catalyst particles. However, since the Au particles in case of InP nanowire growth are most likely to be solid [Dic05], the nucleation of InP nanowires presumably differs considerably from the nucleation of silicon nanowires.

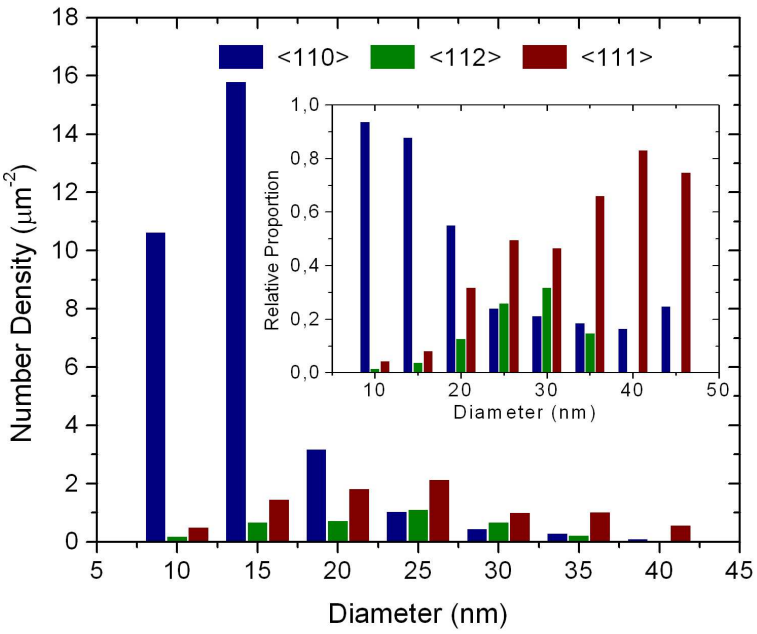

Figure 4.3: Number density versus diameter for different growth directions. Inset: relative proportion of the different growth directions, see also Fig. A.16.

4.3 Theoretical Model

A possible explanation for this diameter dependence of the growth direction will be presented in the following. Considering silicon nanowire growth via the vapor-liquid-solid mechanism, it takes place at the liquid-solid interface. Therefore, it seems obvious that also the growth direction is determined by properties of the liquid-solid interface. In a thermodynamical model, interfaces are usually assumed to be atomically abrupt [Row02a]. In reality, this is not the case. Simulations show that on both sides of a Au/Si-Si interface a certain transition region extending over a few atomic layers, can be found [Kuo04]. Consequently, a description of the liquid-solid interface between the Au/Si alloy droplet and the silicon nanowire has to include all the contributions that arise in this transition region. This means that in our case we have to consider six different contributions: The bulk energy of silicon, the bulk energy of the Au/Si-eutectic droplet, the interface tension of the liquid-solid interface, the line tension of the triple phase line (vapor-Au/Si-Si), the surface tension of the droplet, and the surface tension of the silicon nanowire. But not all of these six terms contribute to our growth direction problem.

Since we are interested in the energy difference between two different growth directions, we can concentrate on the contributions that are growth direction dependent. Suppose, the bulk energy of silicon, the bulk energy of the Au/Si-eutectic alloy, and the surface

tension of the Au/Si-eutectic droplet are direction independent, these contributions cancel out. In addition, we disregard the contribution of the line tension. In generally it is expected that the value of the line tension is somewhere between $1{\times}10^{-11}\,\mathrm{J\,m^{-1}}$ and $1{\times}10^{-9}\,\mathrm{J\,m^{-1}}$ [Row02b]. However, there are theoretical [Get98] and experimental [Dre96] results indicating that the value of the line tension is more likely of the order of $1\times10^{-11}\,\mathrm{J\,m^{-1}}$ and that therefore the contribution of the line tension can be neglected. Consequently, there are

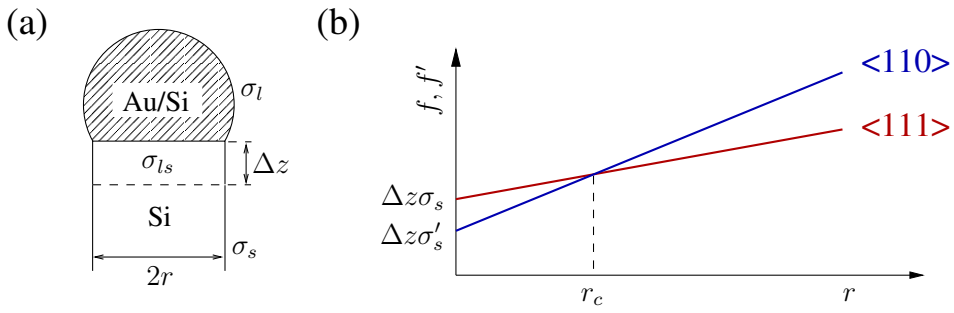

Figure 4.4: Schematic of the free energy per circumference as a function of the radius of both <110> and <111> oriented nanowires.

two terms remaining that depend on the growth direction. First, the interface energy itself, given by the product of the interface area A with the corresponding liquid-solid interface tension σ_{ls}. And second, the silicon surface tension of the edge of the interface. This term is proportional to the circumference L and to the interface thickness Δz on the silicon side (see Fig. 4.4(a)). Hence the energy F of a (111)-oriented interface can now be expressed in terms of the surface and interface tension:

$$F = \Delta z \sigma_s L + \sigma_{ls} A \,. \tag{4.1}$$

Concerning the geometry of the nanowires, we assume that <111> oriented ones have a regular hexagonal cross section with r being the distance from the center to one corner. Since <110> oriented nanowires have surface planes of different orientation the hexagonal cross section of the <110> nanowires is not regular. So in this case we define the radius r of the nanowire as the corner-to-center distance of a regular hexagon having the same circumference as the nanowire in question. The liquid-solid interface is assumed to be flat and perpendicular to the growth direction. Dividing equation (4.1) by L and introducing the geometrical parameter $a = A\,L^{-1}r^{-1}$, which is independent of the radius of the nanowire, the free energy per circumference $f = F/L$ of a <111> oriented nanowire can be expressed as

$$f = \Delta z \sigma_s + a \sigma_{ls}\, r \,. \tag{4.2}$$

This means that f as a function of r is given by a straight line with a y-axis intercept $\Delta z\sigma_s$ and a slope that is proportional to the interface tension of the liquid-solid interface. Keeping in mind the definition of r, a similar expression holds for f', the interface energy

per circumference of a <110> oriented nanowire:

$$f' = \Delta z \sigma'_s + a' \sigma'_{ls}\, r \;, \tag{4.3}$$

where a', σ'_{ls}, and σ'_s are the geometrical parameter, the interface tension and the surface energy of a <110> oriented nanowire. For reason of simplicity, it is assumed here that Δz takes the same value for both orientations. In case that $\sigma_s > \sigma'_s$ and $a'\sigma'_{ls} > a\sigma_{ls}$ the functions f and f' are crossing at a crossover radius r_c, given by

$$r_c = \Delta z \, \frac{\sigma_s - \sigma'_s}{a'\sigma'_{ls} - a\,\sigma_{ls}} \;. \tag{4.4}$$

This is depicted schematically in Fig. 4.4(b), where f and f' are shown as a function of the radius r. It becomes immediately clear that minimizing the energy with respect to the growth direction results in <110> oriented nanowires for radii smaller than r_c, whereas for radii larger than r_c, the <111> direction is energetically more favorable. The reason is that for large diameters the direction with the lowest liquid-solid interface energy is dominant, while for small diameters the surface energy of the silicon nanowire determines the preferential direction of growth. In order to verify this result, estimates for the interface and surface tensions have to be found.

Let us first consider the interface and surface properties of <111> oriented nanowires: The geometrical parameter $a = AL^{-1}r^{-1}$ of the hexagonally shaped (111)-oriented liquid-solid interface is 0.43 (a circular interface would give $a = 0.5$). The interface tension can be calculated using Young's equation (equation (3.1) with $\tau = 0$) provided that the contact angle, the surface tension of the gold-silicon eutectic droplet, and the surface energy of silicon are known. A droplet surface tension of 0.85 J m^{-2} [Nai75], a silicon (111) surface energy of approximately 1.25 J m^{-2} [Zha03, Jac63], and a contact angle of 43° [Res03] then yield an interface tension $\sigma_{ls} = 0.62\,\mathrm{J\,m^{-2}}$. Concerning the surface tension of <111> oriented nanowires we assume that the nanowire is of hexagonal cross section having six $\{110\}$ surface planes. The surface tension can be found by assuming that the surface energy of a certain plane is roughly proportional to the corresponding density of dangling bonds [Giv87a]. This estimate results in a surface tension, which is $\sqrt{3/2}$ larger than the surface tension of a $\{111\}$ plane, giving $\sigma_s = 1.53\,\mathrm{J\,m^{-2}}$. The same argument can be used to find an estimate for the interface tension σ'_{ls} of the liquid-solid interface of a <110> oriented nanowire, which then gives $\sigma'_{ls} = 0.76\,\mathrm{J\,m^{-2}}$. It is assumed that the interface is flat and perpendicular to the growth direction, since our TEM investigations showed no evidence for a V-shaped interface morphology, in contrast to what has been observed by Wu et al. [Wu04a]. Interestingly, the increase of the interface area by such a V-shaped morphology would amount to the same factor $\sqrt{3/2}$ by which the $\{110\}$ interface tension is larger than the $\{111\}$ interface tension.

To evaluate the surface tension σ'_s of the silicon surface of a <110> oriented nanowire, one has to take into account that two of the six surface planes are $\{100\}$ and four are $\{111\}$ planes [Ma03]. The relative area proportion (1.59) of the $\{111\}$ planes to the $\{100\}$ planes can be used together with the Wulff theorem to calculate $\sigma'_s = 1.28\,\mathrm{J\,m^{-2}}$. This means that

<111> orientation	<110> orientation
$a = 0.43$	$a' = 0.39$
$\sigma_{ls} = 0.62\,\mathrm{J\,m^{-2}}$	$\sigma'_{ls} = 0.76\,\mathrm{J\,m^{-2}}$
$\sigma_s = 1.53\,\mathrm{J\,m^{-2}}$	$\sigma'_s = 1.28\,\mathrm{J\,m^{-2}}$

Table 4.1: Summary of parameters determining the critical radius r_c

the surface energy σ'_s of a <110> oriented nanowire is only slightly larger than the surface energy of a silicon $\{111\}$ plane ($1.25\,\mathrm{J\,m^{-2}}$). From the geometry of the nanowire cross section given by Ma et al. [Ma03], a geometrical parameter $a' = 0.39$ can be deduced. A summary of all these parameters is shown in Table 4.1.

The parameter Δz, the "thickness" of the interface, is estimated to be $\Delta z \approx 1$ nm. Together with the estimates for the surface and interface tensions, equation (4.4) leads to a crossover radius $r_c \approx 10$ nm. This value fits very well to the corresponding crossover diameter of 20 nm based on the experimental results shown in Fig. 4.3. It should be emphasized here that the crossover radius strongly depends on the relative magnitude of the interface and surface tensions so that small changes in the surface tension might alter the value for the crossover radius substantially. The <112> direction has not been considered in detail, but we expect that our model could be extended straightforward, provided the required parameters were available.

4.4 Conclusions of Chapter 4

To conclude, we have shown that epitaxially grown silicon nanowires of diameters larger than 40 nm prefer the <111> direction whereas wires with diameters less than 20 nm are mostly <110> oriented. This change of the growth direction has been explained by considering the free energy of the silicon nanowire, which is influenced by both the surface tension and the interface tension. Our model provides an estimate for the crossover diameter of 20 nm, in agreement with experimental data.

Chapter 5

Electrical Characterization of Silicon Nanowires

One of the intrinsic advantages of epitaxially grown silicon nanowires compared to non-epitaxial ones is that the nanowires are already equipped with one good electrical connection located at the lower end, where the nanowire is attached to the substrate. This is especially useful for two-terminal measurements, which largely depend on the quality of the electrical contacts. A second, well-defined electrical connection can be established by contacting the gold catalyst particle at the nanowire tip. This is also the configuration we chose for the electrical characterization of silicon nanowires, presented in this chapter. Following a brief theoretical introduction to the physics of metal-semiconductor contacts, and a more detailed discussion of the influence of interface traps and interface charges on the charge carrier density in the nanowire, temperature-dependent two-terminal current-voltage measurements on both n-doped and p-doped silicon nanowires will be presented and discussed.

5.1 Theory

Generating good metal-semiconductor contacts is an art by itself. This is, because in most cases in which a metal is brought into contact with a semiconductor, so an energetic barrier arises at the metal-semiconductor interface. Walter Schottky [Sch39] first pointed out that this barrier is caused a space-charge layer in the vicinity of the interface. This finding set the basis for investigations on rectifying metal-semiconductor contacts, often referred to as Schottky contacts. In the following subsection, the basic results will be summarized briefly.

5.1.1 Metal-Semiconductor Contacts

Disregarding the influence of interface states, the electrical properties of a metal-semiconductor contact are determined by the work function ϕ_m of the metal and the electron affinity χ of the semiconductor. The work function ϕ_m of the metal is defined as the

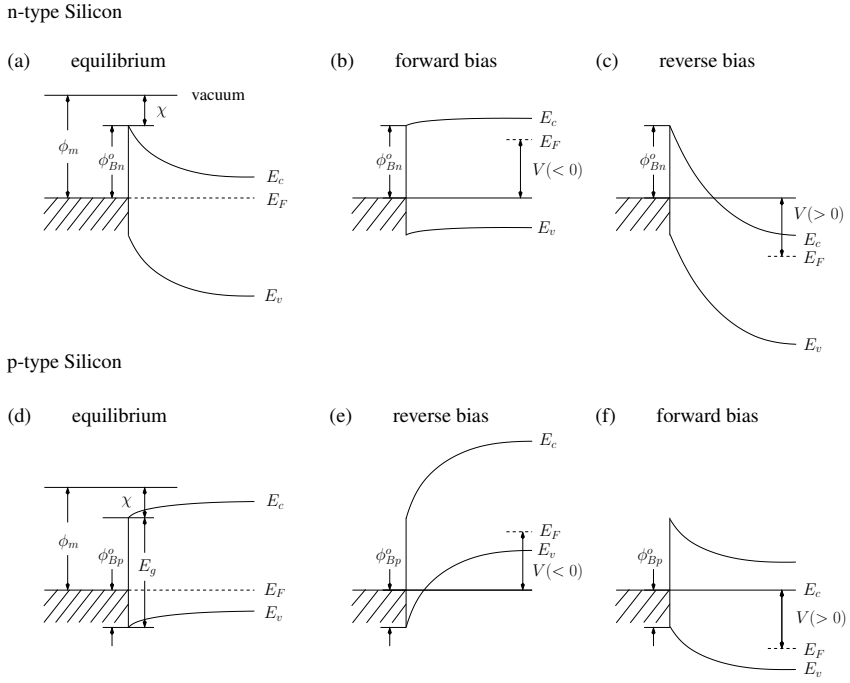

Figure 5.1: Schematic band-diagrams of an ideal metal-semiconductor contact under different bias conditions, after [Sze81c]. (a-c) n-type semiconductor: (a) $V = 0$, (b) $V < 0$, (c) $V > 0$. (b-d) p-type semiconductor: (d) $V = 0$, (e) $V < 0$, (f) $V > 0$.

energy difference between the vacuum level and the Fermi level. The electron affinity χ is the energy difference between the vacuum level and the bottom of the conduction band of the bulk semiconductor. In our case, considering the contact properties of the gold catalyst particle with respect to the silicon nanowire, the metal work function, $\phi_{Au} = 4.70\,\text{eV}$, is larger than the electron affinity of the semiconductor, $\chi_{Si} = 4.05\,\text{eV}$ [Cow65]. Thus we can confine ourselves to the discussion of so-called depletion contacts, which are present if $\phi_m > \chi$. The energetic properties of such depletion contacts are schematically depicted in Fig. 5.1 for both n-type and p-type semiconductors under different bias conditions.

If no voltage is applied and the metal and the n-type semiconductor are in thermal equilibrium, the Fermi levels of the metal and the semiconductor, E_F, have to level out. In order to equilibrate the two Fermi levels, charges accumulate at the metal-semiconductor interface. In case Fig. 5.1(a), these are positive charges in the semiconductor and negative charges in the metal. This charge accumulation in the so-called space charge region can be equivalently described by a band-bending of the semiconductor in the vicinity of the interface. This band bending, on the other hand, signifies a barrier for the charge carriers - the so-called Schottky barrier. According to Fig. 5.1(a), the barrier height ϕ^o_{Bn} of an ideal metal to n-type semiconductor contact can be expressed as

$$\phi^o_{Bn} = \phi_m - \chi \qquad \text{[Sze81c]}. \tag{5.1}$$

In case of a metal contact to a p-type semiconductor (see Fig. 5.1(d)), the barrier height

ϕ^o_{Bp} is given by

$$\phi^o_{Bp} = E_g - \phi_m + \chi \qquad \text{[Sze81c]}, \tag{5.2}$$

where E_g is the bandgap of the semiconductor. Thus for a given metal semiconductor combination, the sum of ϕ^o_{Bn} and ϕ^o_{Bp} should equal the bandgap.

The most prominent property of a metal-semiconductor contact is its rectifying ability. Figure 5.1 (b) and Fig. 5.1(c) schematically show the response of a metal to n-type semiconductor contact under different bias conditions. If the metal is held at constant potential and a negative voltage is applied to the n-type semiconductor, the Schottky barrier is reduced and the Schottky diode is said to be forward biased (see Fig. 5.1(b)). A sufficient forward bias entirely removes the Schottky barrier, so that electrons in the conduction band can flow without hindrance from the semiconductor to the metal. When, like in Fig. 5.1(c), a positive voltage is applied to the semiconductor, the Schottky barrier is blocking the electron current from the metal to the semiconductor, which corresponds to reverse bias conditions.

Considering a metal to p-type semiconductor contact, as shown in Fig. 5.1(d-f), the voltage dependence is reversed. Now the Schottky diode is forward biased for negative voltages and reverse biased for positive voltages. This property can be used to determine the type of majority charge carrier from the rectifying behavior of the Schottky contact.

We have seen so far that the properties of a metal-semiconductor contact are determined by the space-charge layer in the semiconductor. Due to the boundary conditions at the metal surface, the charges in the space charge layer will induce image charges in the metal. The interaction with these image charges effectively lowers the barrier height by an amount $\Delta\phi$. Thus the effective barrier height ϕ_B of a metal contact to an n-type or p-type semiconductor (subscript n and p dropped) is given by

$$\phi_B = \phi^o_B - \Delta\phi \qquad \text{[Sze81c]}. \tag{5.3}$$

This effect, the image charge-induced lowering of the Schottky barrier, is usually referred to as the Schottky effect. It is schematically depicted in Fig. 5.2(a).

Exploiting the full depletion approximation, that is taking the charge density N_{ch} within the space-charge region equal to the density of ionized dopants, and additionally assuming that the dopant atoms are fully ionized, the charge density $N_{ch} = N_D - N_A$, with N_D being the donor, and N_A being the acceptor density. If a voltage V is applied, the Schottky barrier lowering can be expressed as a function of the sum of the voltage V and the built-in potential V_{Bi}

$$\Delta\phi = \left(\frac{q}{\epsilon_s}\right)^{3/4} \left(\frac{N_{ch}}{8\pi^2}\left(V_{Bi} + V \pm \frac{kT}{q}\right)\right)^{1/4} \qquad \text{[Sze81c]}, \tag{5.4}$$

where the plus or minus sign refers to p-type or n-type semiconductors, and ϵ_s is the dielectric constant of the semiconductor. According to Fig. 5.2(a) the built-in potential of an n-type semiconductor, $V_{Bi} > 0$, is defined as the energy difference between the initial barrier maximum and the conduction band edge E_c. In case of a p-type semiconductor, the built in potential, $V_{Bi} < 0$, is given by the energy difference between the barrier maximum

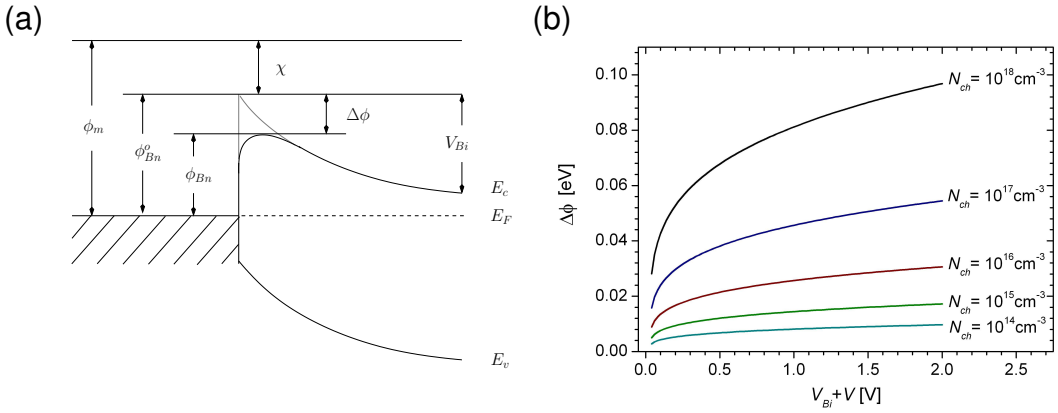

Figure 5.2: (a) Schematic of the Schottky barrier lowering for a metal contact to n-type silicon, after [Sze81c]. (b) Schottky barrier lowering $\Delta\phi$ as a function of $V_{Bi} + V$ at room temperature, see also Fig. A.17.

and the valence band. Figure 5.2 (b) shows the Schottky barrier lowering $\Delta\phi$ for different space charge densities N_{ch} as a function of $V_{Bi} + V$. One can see that the Schottky barrier lowering $\Delta\phi$ is a rather small effect, compared to usual barrier heights. Nevertheless, the Schottky effect is a main cause for the voltage dependence of the reverse current [Sze81d].

Up to now, we assumed that the barrier height is entirely determined by the metal work function ϕ_m and the electron affinity χ of the semiconductor. This is only valid as a first approximation. Experimental investigations [Mey47] revealed that under certain circumstances the barrier height can become more or less independent of the metal work function. As pointed out by Bardeen [Bar47] this apparent contradiction to the Schottky model can be resolved by considering the influence of interface states on the contact behavior. If a certain density of interface states is present, a double layer formed from interface charges and compensating space charges builds up at the metal-semiconductor interface. This double layer causes a potential drop proportional to the interface charge. Thus, the height of the Schottky barrier additionally depends on the density of interface states. For a high density of interface states, the barrier height is mainly determined by the interface state density and consequently becomes effectively independent of the metal work function. This is sometimes referred to as the Fermi level pinning at the interface. Interestingly, it is observed for different semiconductors that, as a consequence of the Fermi level pinning, the barrier height ϕ_{Bn} of a metal to n-type semiconductor contact is approximately $2/3\ E_g$, and that a contact to a p-type semiconductor has a barrier height ϕ_{Bp} of approximately $1/3\ E_g$ [Sch98a].

As already discussed, the current-voltage characteristic of a Schottky metal-semiconductor contact usually shows rectifying behavior. If the barrier width is large enough as to neglect tunneling currents through the barrier, the total current flow across an ideal Schottky contact is determined by the thermionic emission and diffusion of charge carriers over the barrier. It can be derived [Sze81c] that the current-voltage characteristics of metal

contacts to n-type and p-type semiconductors are in a good approximation given by

$$I_n = AA^*T^2 \exp\left(\frac{-\phi_{Bn}}{kT}\right)\left(1 - \exp\left(\frac{-qV}{kT}\right)\right) , \tag{5.5}$$

$$I_p = AA^*T^2 \exp\left(\frac{-\phi_{Bp}}{kT}\right)\left(\exp\left(\frac{qV}{kT}\right) - 1\right) . \tag{5.6}$$

Here A denotes the actual device area, A^* is the effective Richardson constant, and k and T have their usual meaning. Considering contacts to silicon nanowires of not too small a radius, we can assume that the effective Richardson constant A^* approximately equals that of bulk silicon, viz $112\,\mathrm{A\,cm^{-2}\,K^{-2}}$ for n-type and $32\,\mathrm{A\,cm^{-2}\,K^{-2}}$ for p-type silicon, respectively [And70]. Equations (5.5) and (5.6) can be simplified by defining the saturation current I_s comprising all the voltage-independent terms.

$$I_s = AA^*T^2 \exp\left(\frac{-\phi_B}{kT}\right) \qquad \text{[Sze81c]}, \tag{5.7}$$

where we dropped the subscript n or p, respectively, since the definition holds similarly for both types of contacts. In order to describe also non-ideal Schottky-contacts, an ideality factor n can be introduced in equations (5.5) and (5.6) in the following way [Sch98a]:

$$I_n = I_s \exp\left(\frac{-qV}{nkT}\right)\left(\exp\left(\frac{qV}{kT}\right) - 1\right) , \tag{5.8}$$

$$I_p = I_s \exp\left(\frac{qV}{nkT}\right)\left(1 - \exp\left(\frac{-qV}{kT}\right)\right) . \tag{5.9}$$

An ideality factor of $n = 1$ corresponds to an ideal Schottky diode with a pure thermionic charge transport across the barrier. The ideality factor n is expected to take values between 1.0 and 1.5, approximately. Higher ideality factors indicate the presence of other charge carrier transport mechanisms, in addition to thermionic emission and diffusion. The equations (5.8) and (5.9) set the basis for the analyses of the measurements presented in the following sections.

5.1.2 Silicon/Silicon Dioxide Interface

Since silicon easily oxidizes, silicon nanowires brought into air are usually covered by a silicon dioxide shell. Similar to the effect of interface charges on the space charge region of a metal-semiconductor contact, interface charges at the Si/SiO_2 interface will influence the charge carrier density of the semiconductor [Sho48]. Due to their high surface to volume ratio, this is of paramount importance for the properties of the nanowires, as has been recently shown by van Weert et al. [vW06] for InP nanowires. According to the most commonly used nomenclature [Dea80], we can distinguish between charges that are located deep inside the oxide and charges that are located at or in close vicinity of the interface. To the first category belong the oxide trapped charges and the mobile ionic charges having charge densities Q_{ot} and Q_m, respectively.

Since the charges directly at the Si/SiO_2 interface are most important for the electric properties [Nic82a], we will concentrate in the following discussion on the influence of the

interface charges. The interface charge density is given by the sum of two contributions: the fixed oxide charge density Q_f, and the interface trap charge density Q_{it}. The fixed oxide charges, being usually positive do not interact via a charge transfer with the underlying silicon. Hence Q_f does not depend on the position of the Fermi level. Electron-spin-resonance studies show that the trapped oxide charges may at least partly be equivalent to so-called E' resonance centers, which are trivalent silicons, bonded to three oxygens [Sil61, Wee56, Gri80, Len84a]. The fixed oxide charge density of the Si/SiO_2 interface can be strongly reduced by annealing the sample in a hydrogen-rich atmosphere at temperatures around $500\,^{\circ}C$.

The interface trap charges, on the contrary, do exchange charges with the underlying semiconductor. The interface trap charge density Q_{it} arises by charging specific interface states, having a level density $D_{it}[\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}]$. Depending on the position of the Fermi level at the surface, Q_{it} can be either positive or negative. The nature of these interface states is closely related to so-called P_b resonance centers, which were first observed by Nishi et al. [Nis66, Nis71, Nis72] in electron-spin-resonance studies. They could also identify the P_b center as a trivalent silicon at the Si/SiO_2 interface[Nis72], and it could be shown later on that this trivalent silicon is bonded to three underlying silicon atoms [Cap79, Poi81]. Extensive electron-spin-resonance studies on irradiated silicon/oxide capacitors showed that these P_b centers are the main cause for the presence of interface states of irradiated samples [Len82, Len83, Len84b, Len84a, Kim88]. That this also holds to be true for un-irradiated samples was first shown by Caplan et al. [Cap79] and Johnson et al. [Joh83]. Consequently, the characteristic of the interface traps is mainly determined by the properties of the P_b centers.

Concerning the electrical properties of the P_b centers, Lenahan and Dressendorfer found that the P_b centers are amphoteric, which means that they can both accept and donate electrons [Len84a]. In the lower half of the bandgap the P_b center is donor-like ($P_b \rightarrow e^- + P_b^+$). Suppose the Fermi level lies in the lower half of the band-gap, then the P_b centers below the Fermi-level are neutral, whereas the P_b centers between Fermi-level and the bandgap middle are positively charged. The P_b centers in the upper half of the band gap are acceptor-like ($P_b + e^- \rightarrow P_b^-$). If the Fermi level is located in the upper half of the band gap, the P_b centers between the Fermi level and midgap are negatively charged, while the ones above the Fermi level are neutral.

In addition to spin-resonance measurements, the interface trap level density has also been obtained by capacitance [Nic82b], and photovoltage measurements [Mun84, Mun86], deep-level transient spectroscopy [Joh83], measurements of the subthreshold slope [Lyu93], irradiation and annealing studies [McW86, Fle92, Fle93], and simulations [Lau80]. The outcome is that the density of Si/SiO_2 interface trap states is U-shaped around midgap and that the value at midgap can approximately vary between $D_{it} = 1\times10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-2}$ and $D_{it} = 1\times10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-2}$, depending on the oxidation and annealing conditions. The easiest way to reduce the density of interface traps seems to be a short annealing of the sample at temperatures around $1000\,^{\circ}C$. Figure 5.3 (a) shows the interface trap level density for both (100) and (111) oriented interfaces. One can see that the interface trap level density

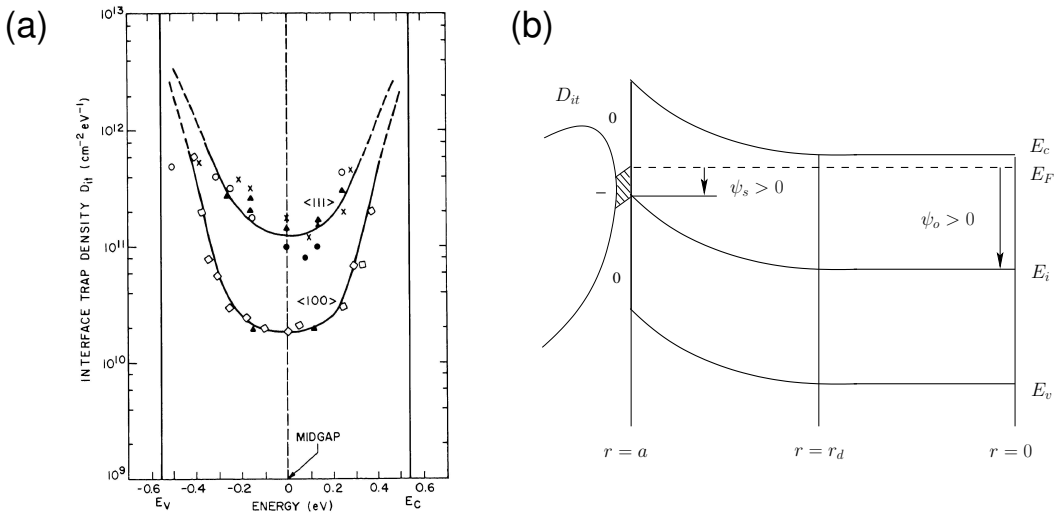

Figure 5.3: (a) Density of interface traps for silicon (100) and (111) [Sze81e] after [Whi72], see also Fig. A.18. (b) Schematic of the Si/SiO_2 interface.

of a (100) interface is roughly a factor five smaller than that of a (111) oriented interface, which can partly be explained by the higher density of dangling bonds of a (111) surface. Furthermore, it is apparent that within a certain range of about $\pm 0.25\,\text{eV}$ around midgap, the trap level density D_{it} is approximately constant.

In the following, we want to derive a model for the effective charge carrier density in a nanowire as a function of the interface trapped charge density Q_{it} and the fixed oxide charge density Q_f. To reduce the complexity of the problem, we want to model the electric properties of the nanowire by considering a circular slice of silicon covered with an oxide layer, additionally assuming radial symmetry. Despite its simplicity, this model provides some worthwhile insights.

Figure 5.3 (b) schematically depicts the band diagram of a circular slice of n-type silicon as a function of the radius, in the presence of a certain interface trap level density D_{it}. The Fermi level E_F at the surface of the circular slice of radius a is located above the midgap level E_i. This corresponds to a positive surface potential ψ_s. As discussed before, the interface traps between the Fermi level and midgap will accept an electron and become negatively charged (see the shaded region in Fig. 5.3(b)). Neglecting the fixed oxide charges for now, this leads to a negative interface charge density. To create this negative interface charge, electrons have to be removed from the silicon, causing an electron depletion layer at the nanowire surface. This can be equivalently described by an upward bending of the conduction and valence band in the depletion layer. As shown in Fig. 5.3(b), the depletion layer extends from an inner radius r_d to the nanowire surface at $r = a$.

If the electrostatic potential $\psi(r)$ is defined with respect to the Fermi level E_f in a way that it equals the midgap level E_i, and the donors and acceptors of density N_D and N_A, respectively, are taken to be fully ionized, we can write the charge density in the

semiconductor as

$$\rho(r) = q\Big(p_o \exp(-\beta\psi(r)) - n_o \exp(\beta\psi(r)) + N_D - N_A\Big) \qquad \text{[Sze81b]}, \tag{5.10}$$

with $\beta = q/kT$. The parameters n_o and p_o in the above equation are given by

$$n_o = N_c \exp\big(-\frac{E_g}{2\,kT}\big)\,, \tag{5.11}$$

$$p_o = N_v \exp\big(-\frac{E_g}{2\,kT}\big)\,, \tag{5.12}$$

where N_c and N_v are the density of states in the conduction and valence band, respectively. In our model we will adopt the full depletion approximation. This means that we assume an abrupt transition between the interface charge-induced depletion layer and the non-depleted semiconductor material. Inside of the depletion layer, the charge density is equal to the number density of dopant atoms times the elemental charge q.

$$\rho = \begin{cases} 0 & 0 \le r < r_d \\ q(N_D - N_A) & r_d \le r \le a \end{cases} \tag{5.13}$$

The electrostatic potential $\psi(r)$ can be obtained by solving the Poisson equation in polar coordinates.

$$\psi(r) = \begin{cases} \psi_o & 0 \le r < r_d \\ \psi_o - \frac{\rho}{4\epsilon_s}(r^2 - r_d^2) & r_d \le r \le a \end{cases} \tag{5.14}$$

According to the above equation, the potential at the silicon surface $\psi_s = \psi(a)$ is

$$\psi_s = \psi_o - \frac{\rho}{4\epsilon_s}(a^2 - r_d^2)\,. \tag{5.15}$$

The potential ψ_o is the potential in the middle of the nanowire, i.e at $r = 0$. If the nanowire is not fully depleted, that is if the inner radius of the depletion region r_d is greater than zero, the charge density within $r \le r_d$ vanishes. The value of the potential ψ_o can be obtained by solving equation (5.10) with $\rho = 0$ for $\psi_o = \psi(0)$.

$$\psi_o = \beta^{-1} \ln\left\{\frac{N_D - N_A}{2n_o}\Big(1 + \big(1 - \frac{2n_o p_o}{(N_D - N_A)^2}\big)^{1/2}\Big)\right\} \qquad \text{[Nic82a]}. \tag{5.16}$$

Let us come back to the Si/SiO_2 interface and its properties. According to our definition, the interface charge density is given by the sum of Q_f and Q_{it}. As the name implies, the fixed oxide charge density is constant and independent of the position of the Fermi level. The interface trapped charges are assumed to have the same characteristic as the P_b centers; that is they are donor-like in the lower-half and acceptor-like in the upper half of the bandgap. In addition, we assume that the interface traps are neutral, if the Fermi level is in midgap position. If we approximate the Fermi distribution by a step function, and assume that the interface trap level density is constant around midgap, the interface trap charge density Q_{it} can be expressed as

$$Q_{it} = -q^2 D_{it} \psi_s \qquad \text{[Mun86]}. \tag{5.17}$$

Charge neutrality provides another condition. Demanding that the nanowire slice is neutral, the space charge in the depletion layer has to equal the interface charge, which gives

$$\pi(a^2 - r_d^2)\rho + 2\pi a(Q_f + Q_{it}) = 0\,. \tag{5.18}$$

Using equation (5.17), we can solve the above equation for the depletion radius,

$$r_d = \sqrt{a^2 + \frac{2aQ_f - 2aq^2 D_{it}\psi_o}{\rho(1 + \frac{aq^2}{2\,\epsilon_s})D_{it}}}\,. \tag{5.19}$$

So we arrived at an expression for the inner radius of the depletion region. One can see that for a specific set of parameters Q_f, D_{it}, a, and ψ_o the inner radius of the depletion layer can become zero. This defines a critical nanowire radius

$$a_{crit} = \frac{\epsilon_s}{q^2 D_{it}}\left(-1 + \left(1 + \frac{4q^2 D_{it}}{\rho\,\epsilon_s}(q^2 D_{it}\psi_o - Q_f)\right)^{1/2}\right)\,. \tag{5.20}$$

If the nanowire radius a is larger than a_{crit}, we face the situation that the nanowire is depleted at its surface, but still conductive in its center, like depicted in Fig. 5.3(b). However, if the nanowire radius a is smaller than a_{crit} the nanowire is fully depleted. Figure 5.4 (a) shows the critical radius of an n-doped nanowire for different interface trap level densities D_{it} and zero fixed oxide charges ($Q_f = 0$) as a function of the donor concentration N_D. The critical radius a_{crit} decreases with increasing doping concentration and decreasing D_{it}. This could be expected, since both, an increase of the doping, and a reduction of the interface trap level density reduces the width of the depletion layer. We can deduce from Fig. 5.4(a) that the doping of a silicon nanowire of $50\,\text{nm}$ in diameter, having a medium trap level density of $D_{it} = 1\times10^{11}\,\text{eV}^{-1}\,\text{cm}^{-2}$ and zero Q_f, has to be larger than $2\times10^{17}\,\text{cm}^{-3}$ to prevent the nanowire from being fully depleted. By expanding the square root of equation (5.20) to first order we can obtain an approximate expression for a_{crit}, which is sufficiently accurate in most cases.

$$a_{crit} \approx \frac{2}{\rho}\left(q^2 D_{it}\psi_o - Q_f\right)\,, \tag{5.21}$$

where ρ is $q(N_D - N_A)$ and ψ_o has to be determined by using equation (5.16). In order to discuss the influence of the interface charges on the charge carrier concentration, we have to distinguish two cases. The first case corresponds to $a > a_{crit}$, i.e. the nanowire is not fully depleted. Considering an n-doped nanowire, we can evaluate the effective electron concentration $n_{eff>}$ of the nanowire by combining equation (5.11) and equation (5.14) and averaging over the nanowire area. The potential in the nanowire center, ψ_o, is given by equation (5.16). (The greater sign in the subscript of $n_{eff>}$ is meant as a reminder that $a > a_{crit}$).

$$\begin{aligned} n_{eff>} &= \frac{1}{a^2\pi}\int_0^a n_o \exp(\beta\psi(r))2\pi r dr \\ &= \frac{2n_o}{a^2}\left\{\int_0^{r_d}\exp(\beta\psi_o)r dr + \int_{r_d}^{a}\exp\left(\beta\psi_o + \frac{\beta\rho}{4\epsilon_s}(r_d^2 - r^2)\right)r dr\right\} \\ &= n_o\exp(\beta\psi_o)\left\{\frac{r_d^2}{a^2} + \frac{4\epsilon_s}{\beta\rho a^2}\left(1 - \exp\left(\frac{\beta\rho}{4\epsilon_s}(r_d^2 - a^2)\right)\right)\right\}\,, \end{aligned} \tag{5.22}$$

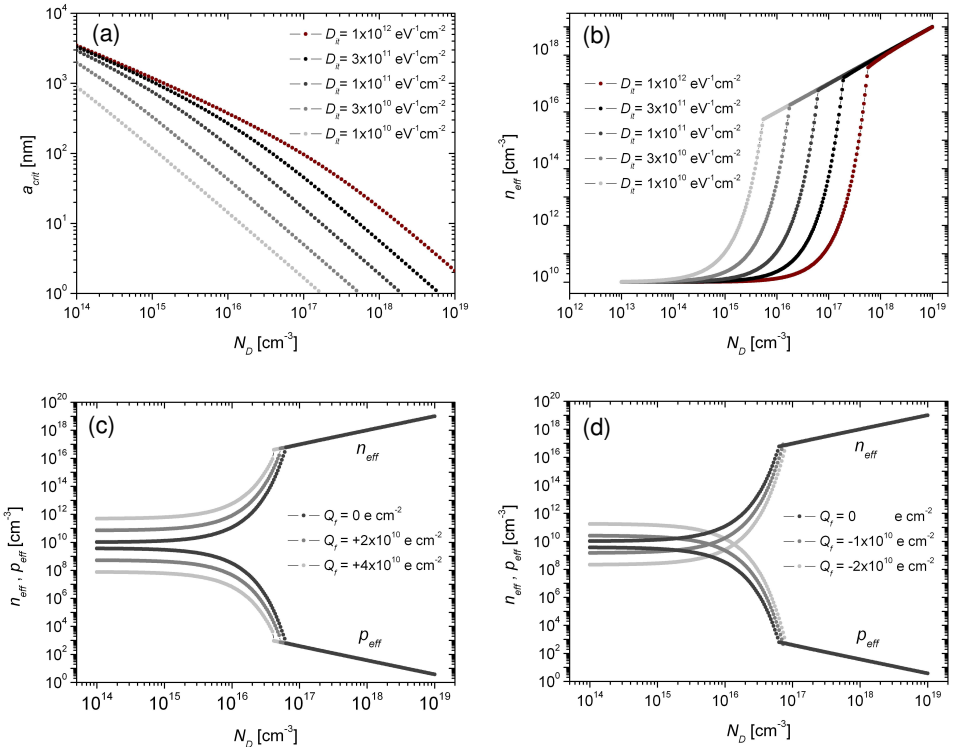

Figure 5.4: (a) Critical radius a_{crit} for different interface trap level densities D_{it} as a function of the donor concentration N_D; $Q_f = 0$, see also Fig. A.19. (b) Effective electron densities n_{eff} for different values of D_{it}, assuming $Q_f = 0$ and $a = 25\,\text{nm}$, see also Fig. A.20. (c) Effective electron and hole density, n_{eff} and p_{eff}, as a function of N_D for $a = 25\,\text{nm}$, $D_{it} = 1\times10^{11}\,\text{eV}^{-1}\,\text{cm}^{-2}$ and different values of $Q_f \geq 0$, see also Fig. A.21. (d) n_{eff} and p_{eff} as a function of N_D for $a = 25\,\text{nm}$, $D_{it} = 1\times10^{11}\,\text{eV}^{-1}\,\text{cm}^{-2}$ and different values of $Q_f \leq 0$, see also Fig. A.22.

The second case corresponds to the situation where the wire is fully depleted ($a < a_{crit}$). The electrostatic potential can then be expressed as

$$\psi(r) = \psi_s + \frac{\rho}{4\epsilon_s}(a^2 - r^2)\,, \tag{5.23}$$

where the surface potential is determined by the charge neutrality condition

$$\psi_s = \frac{a\rho + 2Q_f}{2q^2 D_{it}} \tag{5.24}$$

The effective electron density $n_{eff<}$ for the fully depleted case ($a < a_{crit}$) can be obtained by averaging the electron density over the nanowire area

$$\begin{aligned} n_{eff<} &= \frac{1}{a^2\pi}\int_0^a n_o \exp(\beta\psi(r))2\pi r dr \\ &= n_o \exp(\beta\psi_s)\frac{4\epsilon_s}{\beta\rho a^2}\Big(\exp\big(\frac{\beta\rho a^2}{4\epsilon_s}\big) - 1\Big)\,. \end{aligned} \tag{5.25}$$

Combining equation (5.22) and (5.25), we can evaluate the effective electron density n_{eff} for an arbitrary combination of N_D, Q_f and D_{it}. Figure 5.4 (b) shows n_{eff} for different interface trap level densities D_{it}, zero Q_f, and a radius a of 25 nm as a function of the donor density N_D. The characteristic feature of the curves is a sharp transition between a region of high and a region of low effective electron density. Clearly this transition is located at the N_D value, where the wire starts to be fully depleted. Similarly to Fig. 5.4(a), the onset of full depletion is shifted on the N_D axis depending on the density of interface trap levels. The smaller the D_{it} value is, the smaller the doping concentration can be, without causing a full depletion of the nanowire. Since the fixed oxide charge was set to zero, the effective electron concentration approaches the intrinsic value of 1.5×10^{10} cm^{-3} in the limit of low doping concentrations.

In order to give an impression of the effect of fixed oxide charges, Fig. 5.4(c) shows the effective electron density n_{eff} and the effective hole density p_{eff} as a function of N_D, assuming a medium interface trap level density $D_{it} = 1\times10^{11}$ eV^{-1} cm^{-2} and a nanowire radius of 25 nm. The fixed oxide charge is taken to be positive. In the low N_D region, where the nanowire is fully depleted, the effective electron density is basically determined by the position of the surface potential. Equation (5.24) implies that positive fixed oxide charge will lead to an increase of the surface potential, which corresponds to an increase of the electron concentration, and a concomitant decrease of the hole concentration. This can be seen Fig. 5.4(c). In the limit of low doping concentrations, n_{eff} approaches a value that is greater than the intrinsic electron concentration. For negative fixed oxide charges, the effect is reversed. As depicted in Fig. 5.4(d), a negative fixed oxide charges density will lead to an effective electron concentration that is smaller, and an effective hole density that is greater than the intrinsic one. The nanowire is than said to be inverted.

To summarize the above results briefly, we have seen that especially the interface trap level density D_{it} has a considerable influence on the effective charge carrier density, which is clearly a consequence of the high surface to volume ratio of the nanowires. We have derived an expression for a critical nanowire radius a_{crit}, depending on the interface trap level density D_{it}, the fixed oxide charge density Q_f, and the dopant density. If the radius is smaller than the critical radius a_{crit} the nanowire will be fully depleted, whereas for a radius greater than a_{crit} only an outer shell of the nanowire will be depleted.

5.2 Array of n-Doped Nanowires

Single nanowire measurements are technologically challenging, both from a sample fabrication and a measurement point of view. Therefore we concentrate on contacting arrays of nanowires with macroscopic contacts defined by standard optical lithography. The detailed experimental procedure is described below. Temperature-dependent measurements of epitaxial n-doped nanowires are presented and discussed in detail.

5.2.1 Experimental

The n-doped silicon nanowire samples were prepared in the following way. As substrate, phosphorus doped ($7-13\,\Omega$ cm), (111)-oriented 100 mm silicon wafers were used. Before transferring the wafers into the ultra-high vacuum (UHV) system, the wafers were cleaned by a two-step wet chemical cleaning and a short HF dip. Details on the wafer preparation are given in Section 1.1.

As a catalyst for the VLS nanowire growth, a gold layer of 0.5 nm thickness was in situ deposited onto the hydrogen-terminated silicon wafer, using an electron beam evaporation source (Tectra). In order to break up the gold film, the wafer was annealed at $450\,^{\circ}$C for 20 minutes. Afterwards the temperature was lowered to $300\,^{\circ}$C, well below the eutectic point. At this temperature, a small amount of antimony was deposited onto the substrate by an e^{-}-beam evaporation source. The antimony is assumed to be dissolved in the droplet and to be incorporated little by little into the silicon nanowire during growth. Antimony is known to have an electronic level in silicon located 0.039 eV below the conduction band [Sze81b], thus causing an n-type doping of the silicon nanowires.

Upon the antimony deposition, the temperature was raised to the growth temperature of $450\,^{\circ}$C. The silicon nanowires were grown at a constant pressure of 1.8 mbar (5% silane, 95% argon) and at constant gas flow of 40 sccm, within about 7 minutes. An image of the as-grown silicon nanowires is shown in Fig. 5.5(a). The nanowires have an average diameter of approximately 50 nm and a length of about 500 nm.

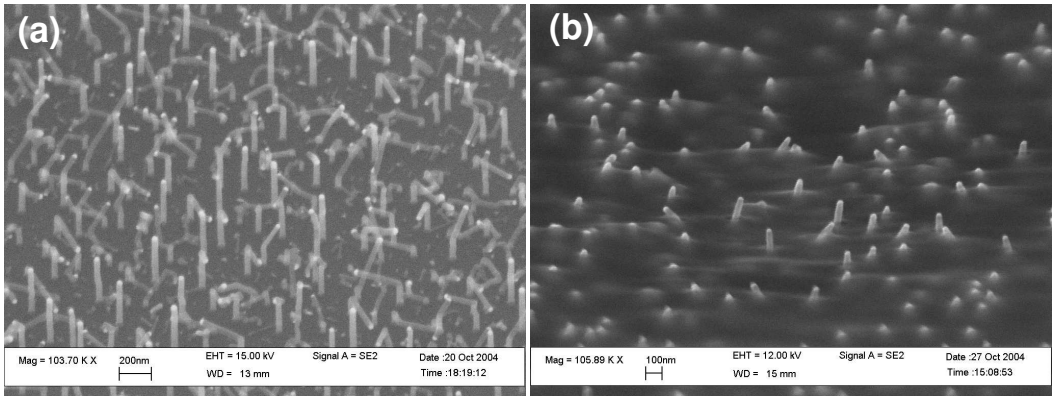

Figure 5.5: n-doped silicon nanowires (a) as-grown; (b) embedded and etched.

After silicon nanowire growth, 2 nm of dysprosium were deposited in situ onto the backside of the wafer in order to achieve good electrical contact to the substrate. The resulting epitaxially grown silicon nanowires were then embedded into a layer of spin-on-glass (Futurrex IC1-200) which was baked out at $400\,^{\circ}$C. The spin-on-glass was etched down, using a commercial reactive ion etching system (Oxford, Plasmalab: 49 sccm CHF_3, 1 sccm O_2, 15mbar, 100 W), to uncover the gold tips from the SiO_2, see Fig. 5.5(b). The top contacts, having an area of $6\times10^5\,\mu m^2$, were defined by standard optical lithography techniques, followed by a deposition of 100 nm of aluminum.

5.2.2 Results and Discussion

All temperature-dependent electrical measurements were performed in a vacuum probe station using an Agilent 4155C semiconductor parameter analyzer. The sample was clamped inside the probe station onto a heatable/coolable chuck with a piece of indium foil between the metalized sample backside and the chuck. Purpose of the indium foil was to improve the thermal contact between the sample and the chuck. The lithographically defined contact pads, on top of the sample, were contacted by a probe needle. Measurements were carried out at temperatures between 290 K and 130 K, with the temperature controlled by a proportional-integral-differential (PID) controller. Figure 5.6 (a) shows the temperature-

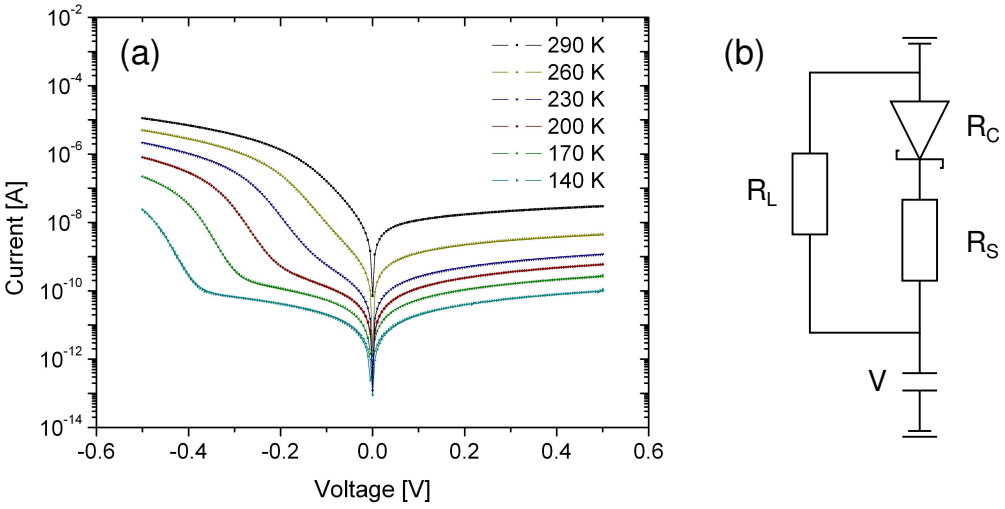

Figure 5.6: (a) Temperature-dependent current-voltage measurement of an array of n-doped silicon nanowires, see also Fig. A.23. (b) Corresponding equivalent circuit.

dependent current-voltage characteristics of an array of n-doped silicon nanowires. The measurements reveal a pronounced rectifying behavior with a forward current at -0.5 V that is approximately three orders of magnitude larger than the reverse current at $+0.5$ V. This behavior can be attributed to the characteristic of a Au/n-Si Schottky contact. As shown in Fig. 5.1, a Au/n-Si Schottky contact with the voltage applied to the semiconductor and the metal held at constant potential is forward biased for negative and reverse biased for positive voltages (see Fig. 5.1). This is consistent with the measurement and a first indication that the observed rectifying behavior is indeed caused by the Au/n-Si contact.

A closer inspection of the measurement reveals that three different regions can be identified for negative voltages; and to each region a different element of the equivalent circuit, shown in Fig. 5.6(b), can be assigned. The first region to consider is where the curves have a more or less constant slope, which indicates an exponential current-voltage dependence. This exponential increase can be attributed to the characteristic of the Au/n-Si Schottky diode. In Fig. 5.6(b) this contact is symbolized by a Schottky diode having

voltage-dependent resistance R_c corresponding to equation (5.8). The second region can be found for elevated temperatures and strongly negative bias voltages. Under these conditions, the current starts to saturate. This means that the IV-characteristic is now dominated by a series resistance R_s, also shown in the equivalent circuit of Fig. 5.6(b). One can see that the level of saturation of the current, for example at -0.5 V, decreases with temperature. Therefore, we can infer that the series resistance is temperature-dependent and increases with decreasing temperature. The third feature of Fig. 5.6 is that the exponential current-voltage dependence, caused by the Schottky diode, flattens out at low temperatures and moderate forward bias, producing a kink in the current-voltage curves. This behavior can be explained by a leakage current path that bypasses the Schottky contact. In the equivalent circuit, shown in Fig. 5.6(b), this leakage current is accounted for by a parallel resistance R_l. Also this parallel resistance is temperature-dependent. It increases with decreasing temperature. Hence the equivalent circuit with which we intend to simulate the set of temperature-dependent measurements consists of the Au/n-Si Schottky diode and two temperature-dependent resistances, R_l and R_s.

Let us first concentrate on the Schottky contact, which is characterized by three unknown parameters, the actual device area A, the ideality factor n, and the barrier height ϕ_{Bn}. As stated in equation (5.8), the current-voltage characteristic of a Schottky contact to an n-type semiconductor can be approximated as

$$I_n = I_s \exp\left(\frac{-qV}{nkT}\right)\left(\exp\left(\frac{qV}{kT}\right) - 1\right) \qquad \text{[Sch98a].} \tag{5.26}$$

Thus a logarithmic plot of $I_n/(\exp\left(\frac{qV}{kT}\right) - 1)$ versus voltage should give a straight line with a slope that is inversely proportional to the ideality factor and a y-axis intercept that is equal to I_s. Such a plot, for five different temperatures between 260 K and 300 K, is shown in Fig. 5.7(a). It is easily seen that the data are in excellent agreement with the expected linear behavior.

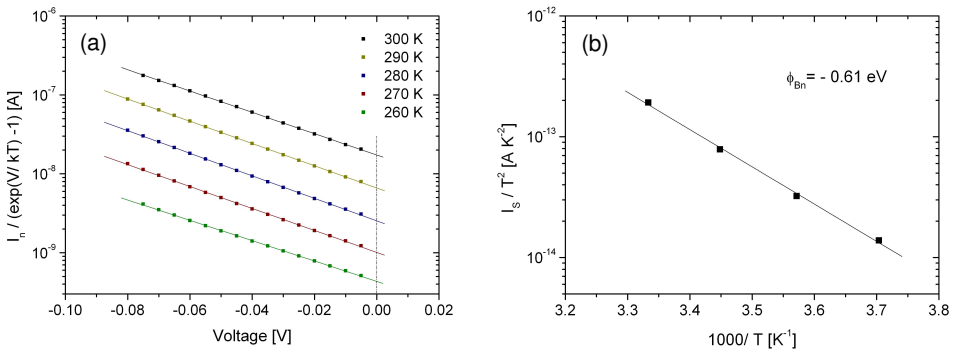

Figure 5.7: (a) $I_n/(\exp\left(\frac{qV}{kT}\right) - 1)$ versus voltage for determination of n and I_s, see also Fig. A.24. (b) Richardson plot for determination of the Schottky barrier height, see also Fig. A.25.

By linearly fitting the data of Fig. 5.7(a) an ideality factor $n = 1.2$ can be found from

the slope of the linear fit, which is a relatively good value. Usually, it is expected that the ideality factor takes values between $n = 1$ and $n = 1.5$, where an ideality factor of one represents an ideal Schottky diode. The y-axis intercept of the linear fit gives the saturation current I_s, defined as

$$I_s = AA^*T^2 \exp\left(\frac{-\phi_{Bn}}{kT}\right) \qquad \text{[Sch98a]}. \tag{5.27}$$

Considering this definition, it becomes clear that a logarithmic plot of I_s/T^2 versus the inverse temperature has a slope that is proportional to the Schottky barrier height and a y-axis intercept that is equal to AA^*. This represents the standard procedure to determine the barrier height, sometimes referred to as a Richardson plot. In Fig. 5.7(b) such a Richardson plot using the I_s values of Fig. 5.7(a) is shown. The slope of the linear fit corresponds to a barrier height of $\phi_{Bn} = 0.61$ eV, which is smaller than the 0.8 eV, reported in literature [Cro64, Cow65] for a Au/n-Si contact. There are several reasons for this. One is that we measure a parallel arrangement of about 10^6 Schottky contacts. Due to the parallel switching, the measured barrier height will be dominated by the smallest values among the varying barrier heights of the nanowire contacts. This at least partially explains the deviation. Another possible reason why the measured barrier height is slightly smaller than expected, might be the influence of interface states at the metal-semiconductor interface. The interface states, and with them the measured barrier height, are sensitive to the experimental procedure by which the contact has been produced. An annealing of the metal-semiconductor contact, for example, can change the barrier height considerably [Sze81d]. A third possible cause for the deviation might be the small contact size. Usually, metal-semiconductor contacts are dealt as a one-dimensional problem, i.e. neglecting effects at the contact edges. In our case the contact diameter is of the order of 50 nm, so that an influence of Si/SiO_2 interface charges located in the vicinity of the contact edge can probably not be excluded [AB78]. Considering all these effects, we think that the measured barrier height is in fair agreement with the value reported in literature.

From the y-axis intercept of Fig. 5.7(b) we can obtain the product $AA^* = 3.5 \times 10^{-3}\,\mathrm{A\,K^{-2}}$. If the Richardson constant A^* is taken to equal that of n-type bulk silicon, $A^* = 112\,\mathrm{A\,cm^{-2}\,K^{-2}}$ [And70], we can deduce a Au/n-Si contact area of $3.1 \times 10^{-5}\,\mathrm{cm^2}$. The area of a single nanowire (diameter 50 nm) is approximately $2 \times 10^{-11}\,\mathrm{cm^2}$, which corresponds to roughly 1.6×10^6 nanowires contacted in parallel. The total area of the contact pad is $6 \times 10^5\,\mu\mathrm{m}^2$, which means that according to the measurement, the density of contacted nanowires is approximately $3\,\mu\mathrm{m}^{-2}$. Three contacted nanowires per square micrometer roughly agrees with the scanning electron micrograph, shown in Fig. 5.5.

Let us now focus on the leakage current, which cuts off the Schottky-diode like behavior for temperatures below 230 K and currents smaller than $\approx 10^{-9}$ A, as shown in Fig. 5.6(a). The current-voltage characteristics for different temperatures are plotted in Fig. 5.8(a) on a linear scale. They show a linear behavior, so that the resistance can directly be extracted from the slope. This resistance can be interpreted as a leak-resistance R_l of the equivalent circuit shown in Fig. 5.6(b). The such obtained values of R_l are plotted in Fig. 5.8(b) as a function of the inverse temperature. The leak resistance R_l exhibits a slight

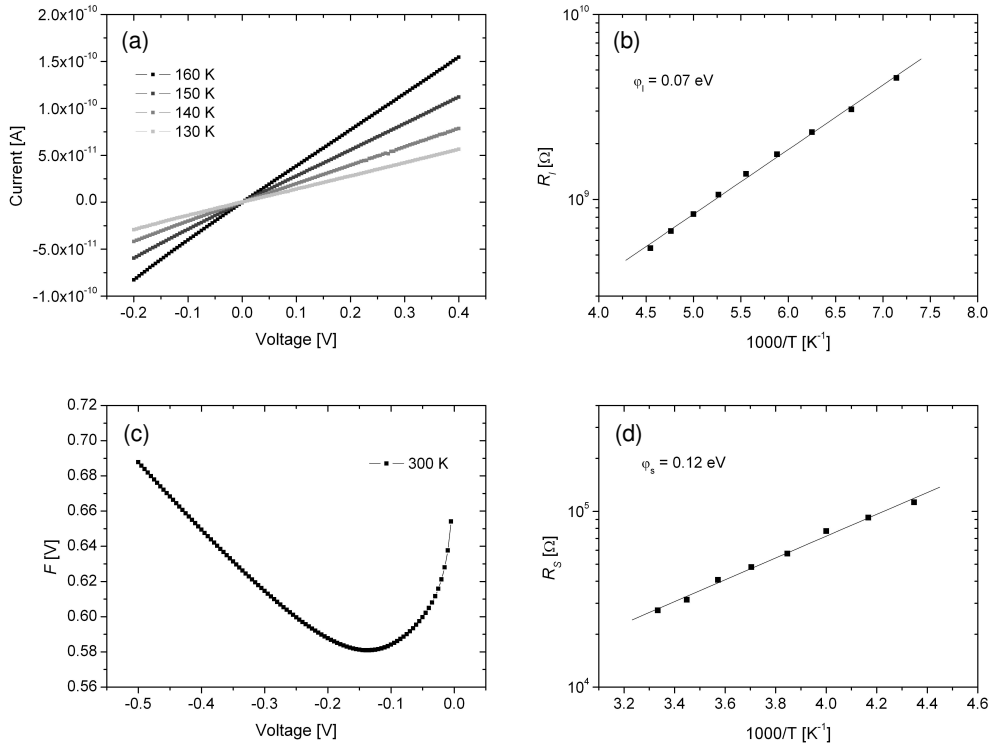

Figure 5.8: (a) Current-voltage characteristics for low temperatures on a linear scale, see also Fig. A.26. (b) Temperature dependence of the leak-resistance R_l, see also Fig. A.27. (c) Norde Plot of the forward current, see also Fig. A.28. (d) Temperature dependence of the series resistance R_s, see also Fig. A.29.

temperature dependence, which in a good approximation can be taken to be exponential. The slope of the linear fit of Fig. 5.8(b) leads to an activation energy of $\varphi_l = 0.07\,\mathrm{eV}$. Hence, the leak-resistance can be approximated as $R_l = 1.5 \times 10^7 \exp(0.07\,\mathrm{eV}/kT)\,\Omega$, which corresponds to $2 \times 10^8\,\Omega$ at 300 K.

We have seen in Fig. 5.6(a) that for large forward currents, the current is driven into saturation, which indicates the existence of a series-resistance R_s. However, to determine the magnitude of this series resistance, including its temperature dependence, is a little more subtle, since the nanowire current-voltage characteristic, even for large forward bias voltages, shows a mixture of an ohmic behavior due to R_s and a diode-like behavior due to the Schottky contact. To circumvent this obstacle, Norde developed a method [Nor79] to determine the series resistance of Schottky diodes, called Norde plot after him. According to equation (5.8), the current-voltage characteristic of a Schottky diode at large forward (negative) bias, using $(\exp(qV/kT) - 1) \approx -1$, is approximately given by

$$I_n = -AA^*T^2 \exp\left(\frac{-\phi_{Bn}}{kT}\right) \exp\left(\frac{-qV}{nkT}\right). \tag{5.28}$$

In the presence of a series resistance R_s, the voltage drop over the Schottky contact is

reduced by an amount $R_s I_n$, thus the current I_n can be expressed as

$$I_n = -AA^*T^2 \exp\left(\frac{-\phi_{Bn}}{kT}\right) \exp\left(\frac{-q(V - R_s I_n)}{nkT}\right) . \tag{5.29}$$

One can now define the so-called Norde-function $F(V, I_n)$ as

$$\begin{aligned} F(V, I_n) &= -\frac{V}{2} - \frac{kT}{q} \ln\left|\frac{I_n}{AA^*T^2}\right| \\ &= \left(\frac{1}{n} - \frac{1}{2}\right)V + \frac{\phi_{Bn}}{q} - \frac{R_s I_n}{n} \qquad \text{[Sch98b]}. \end{aligned} \tag{5.30}$$

The term $V/2$ enters here with a minus, since the diode is forward biased for negative voltages. As long as the ideality factor n is smaller than two, this function $F(V, I_n)$ exhibits a minimum F_{min} at a voltage V_{min}. These values can be used to determine the series resistance. As an example, the Norde function at 300 K is shown in Fig. 5.8(c). From the extremum condition $\partial F(V, I_n)/\partial V = 0$ it can be easily derived using equations (5.29) and (5.30) that

$$R_s = \left(\frac{n-2}{I_{min}}\right)\frac{kT}{q} \qquad \text{[Sch98b]}, \tag{5.31}$$

$$F_{min} = \frac{\phi_{Bn}}{q} + \left(\frac{2-n}{2n}\right)V_{min} + \left(\frac{2-n}{n}\right)\frac{kT}{q} \qquad \text{[Sch98b]}, \tag{5.32}$$

where I_{min} denotes the current I_n that corresponds to the voltage V_{min}. Using equation (5.31) and the measured ideality factor of $n = 1.2$, the series resistance of an array of n-doped nanowires can be determined for various temperatures.

In Fig. 5.8(d), the resulting R_s values are plotted as a function of inverse temperature. One can see that the data points are located close to a straight line, so that we can assume an exponential temperature dependence. Linearly fitting the data, Fig. 5.8(d) gives an activation energy of $0.12\,\text{eV}$. Thus the series resistance can be approximated as $R_s \approx 3 \times 10^2 \exp(0.12\,\text{eV}/kT)$, which corresponds to series resistance of $3 \times 10^4\,\Omega$ at room temperature. Assuming an average length of the nanowires of roughly $500\,\text{nm}$ and taking the mobility of bulk silicon ($1 \times 10^3\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$) leads to an effective electron density $n_{eff} \approx 3{\times}10^{11}\,\text{cm}^{-3}$. So the nanowires, although doped, seem to have an electron density insignificantly higher than that of intrinsic silicon. However, such a low effective electron density can be explained by considering the effect of interface traps, as shown in Fig.5.4(b). A high interface trap level density of $1 \times 10^{12}\,\text{eV}^{-1}\,\text{cm}^{-2}$ - we did not try to reduce the interface trap density of the nanowires by any means - would cause a full depletion of the nanowires, given that the doping concentration N_D is less than about $2 \times 10^{17}\,\text{cm}^{-3}$. Probably the doping of the wires was below this threshold.

Equation (5.32) can also be used to determine the barrier height ϕ_{Bn} and to cross-check in this way the barrier height value of $\phi_{Bn} = 0.61\,\text{eV}$ we obtained from the Richardson plot shown in Fig. 5.7(b). The resulting values of the barrier height, determined at different temperatures, have a mean value of $0.62 \pm 0.01\,\text{eV}$.

$$
\begin{aligned}
A &= 3.2\times10^{-5}\,\mathrm{cm}^2 \\
\phi_{Bn} &= 0.61\,\mathrm{eV} \\
n &= 1.2 \\
R_s &= 3.0\times10^{2}\exp(0.12\,\mathrm{eV}/kT)\,\Omega \\
R_l &= 1.5\times10^{7}\exp(0.07\,\mathrm{eV}/kT)\,\Omega
\end{aligned}
$$

Table 5.1: Parameters deduced from the current-voltage characteristics of an array of n-doped nanowires.

All parameters we obtained so far by analyzing the current-voltage behavior are summarized in Table 5.1. Together with the proposed equivalent circuit of Fig. 5.6(b), these values were used to simulate the current-voltage characteristic of the array of n-doped nanowires. For comparison, the measured and simulated data are plotted in Fig. 5.9(a) and Fig. 5.9(b), respectively. One can see that the parameters we derived from the measure-

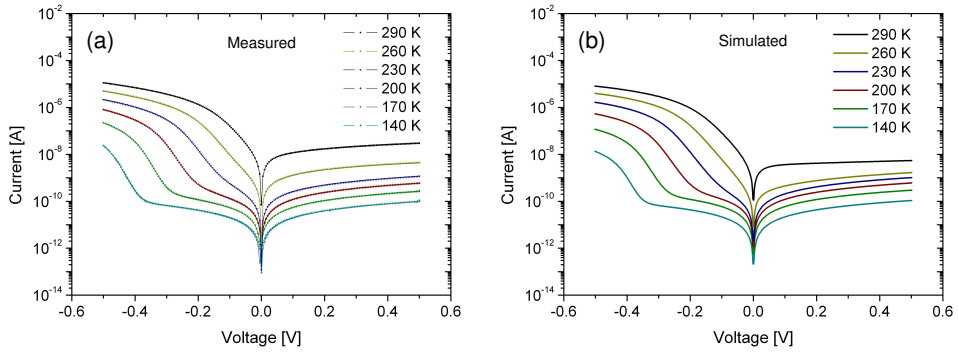

Figure 5.9: (a) Measured temperature-dependent current-voltage characteristic of an array of n-doped silicon nanowires, see also Fig. A.23. (b) Simulation of the measurement using the parameters extracted from (a), see also Fig. A.30.

ment indeed give a good qualitative description of the current-voltage behavior. The most apparent disagreement regards the reverse current at temperatures close to room temperature. This is because at elevated temperature, the reverse current behavior is dominated by the characteristic of the Schottky contact, which we modelled by using equation (5.8). However, this formula for an ideal Schottky contact disregards the Schottky effect, i.e. the voltage induced lowering of the barrier height, and other effects that alter the voltage dependence of the reverse current. Instead, equation (5.8) predicts an approximately constant reverse current for voltages $V > 5\,kT/q$.

5.3 Array of p-Doped Nanowires

5.3.1 Experimental

The procedure for producing samples of p-doped nanowires is closely related to the way the n-doped nanowires are prepared. As substrate, a hydrogen terminated boron-doped ($> 5\,\Omega\,$cm) wafer was used, onto which a layer of gold of $0.5\,$nm thickness was in situ evaporated in the UHV system. The wafer was subsequently annealed at $450\,^{\circ}$C for 20 minutes. The temperature was then lowered to $300\,^{\circ}$C, and at this temperature, a small amount of boron was evaporated onto the sample by a thermal evaporation source in order to achieve a p-doping of the nanowires. After deposition, the temperature was increased to the growth temperature of $450\,^{\circ}$C. The silicon nanowires were grown using diluted silane (5% in argon) as precursor gas at a flow of 40 sccm and a pressure of 1.9 mbar. After ten minutes the silane supply was switched off and the growth chamber was evacuated. The resulting nanowires, having a typical diameter of 50 nm, are shown in Fig. 5.10. About one half are grown without kinks in the $<111>$ direction perpendicular to the surface. These have lengths of about 500 nm.

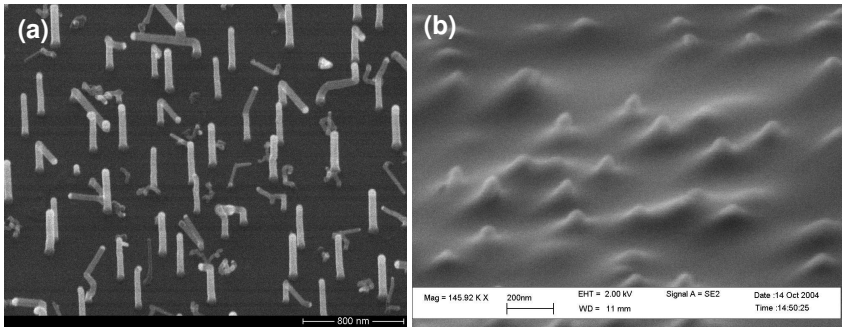

Figure 5.10: p-doped silicon nanowires: (a) as-grown; (b) embedded and etched.

To achieve a good electrical contact to the substrate, 2 nm of platinum were deposited in-situ by an electron beam evaporation source onto the backside of the silicon wafer. The silicon nanowires were then embedded into three layers of spin-on-glass (Futturex IC1-200, 3000 turns/min). To uncover the gold tips of the nanowires, the sample was etched in a reactive ion etch system (Oxford, Plasmalab: 49 sccm CHF_3, 1 sccm O_2, 15 mbar) for 5 minutes. The result is shown in Fig. 5.10(b). Contacts pads (0.4×0.5 mm^2) were defined by optical lithography followed by a deposition of 150 nm of platinum to achieve a good top contact to the gold tips of the nanowires.

5.3.2 Results and Discussion

Fig. 5.11(a) shows the temperature-dependent current-voltage characteristics of an array of p-doped silicon nanowires on a logarithmic scale. For temperatures smaller than $200\,$K the current-voltage characteristics exhibit a pronounced rectifying behavior with the forward current being about two orders of magnitude larger than the reverse current. This

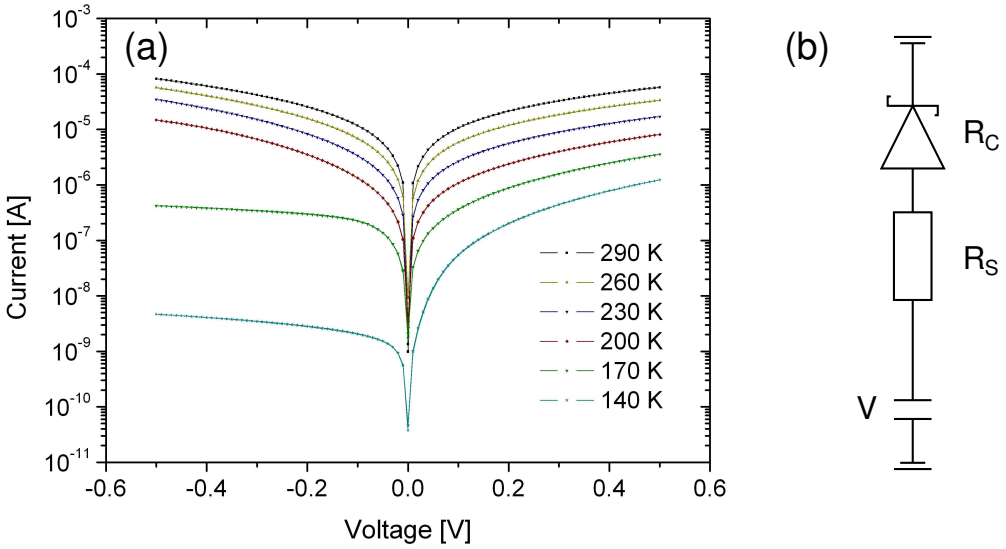

Figure 5.11: (a) Temperature-dependent current-voltage measurement of an array of p-doped silicon nanowires, see also Fig. A.31. (b) Corresponding equivalent circuit.

can be attributed to the diode like behavior of a Au/p-Si Schottky contact. Note that, as shown in Fig. 5.1, the Schottky diode is forward biased for positive voltage. This is indicative of a hole current flowing across the metal-semiconductor contact. As shown in the equivalent circuit of Fig. 5.11(b), a contact resistance R_c is assigned to the Schottky contact. For temperatures larger or equal 200 K the diode-like behavior disappears and instead the current-voltage behavior becomes more or less ohmic. This indicates the existence of a series resistance R_s. So in this case the equivalent circuit shown in Fig. 5.11(b) only consists of two elements, the Schottky contact of resistance R_c and the series resistance R_s. The task now is to determine the parameters defining these two elements. Let us first concentrate on the Schottky contact.

As apparent from Fig. 5.11(a), a region of constant slope, i.e. of an exponential current increase is absent in forward direction, so that the usual Richardson plot procedure to determine ϕ_{Bp}, n, and AA^* cannot be applied here. We therefore have to make use of the Norde plot procedure, which is more tedious, but nevertheless worthwhile. In our case, the procedure is additionally complicated by the fact that we neither know the ideality factor n, nor the effective device area A, parameters that are required as an input for the standard Norde plot method [Nor79]. Therefore a modified version has to be used.

Like in the case of the standard Norde plot method, the approximated form of the Schottky-contact formula (5.9), valid in forward direction for voltages greater than a few kT/q, serves as a starting point for our considerations. Including the effect of the series

resistance, this gives

$$I_p = AA^*T^2 \exp\left(\frac{-\phi_{Bp}}{kT}\right) \exp\left(\frac{q}{nkT}(V - I_p R_s)\right) . \tag{5.33}$$

Considering this relation, we can define the modified generalized Norde function $G(V, I_p, \gamma)$ as

$$\begin{aligned} G(V, I_p, \gamma) &= \frac{V}{\gamma} - \frac{kT}{q} \ln\left|\frac{I_p}{T^2}\right| \\ &= \left(\frac{1}{\gamma} - \frac{1}{n}\right)V + \frac{\phi_{Bp}}{q} + \frac{I_p R_s}{n} - \frac{kT}{q} \ln(AA^*) . \end{aligned} \tag{5.34}$$

This function $G(V, I_p, \gamma)$ is said to be generalized, because the term $V/2$ of equation (5.30) is replaced by the expression V/γ [Boh86], introducing the additional parameter γ. It is modified, inasmuch the current I_p in the logarithm is not divided by AA^*T^2, like in equation (5.30), but only by T^2 [Sch98b]. As long as the parameter γ is chosen to be larger than the ideality factor n, the function $G(V, I_p, \gamma)$ exhibits a minimum G_{min} at a voltage V_{min}. Using the extremum condition together with equations (5.33) and (5.34), the following two relations are easily derived:

$$R_s = \left(\frac{\gamma - n}{I_{min}}\right)\frac{kT}{q} , \tag{5.35}$$

$$G_{min} = \left(\frac{n - \gamma}{\gamma\, n}\right)V_{min} + \frac{\phi_{Bp}}{q} + \frac{kT}{q}\left(\frac{\gamma - n}{n}\right) - \frac{kT}{q} \ln(AA^*) . \tag{5.36}$$

The procedure is like before, we determine the minimum of the Norde function $G(V, I_p, \gamma)$ which gives us the values of G_{min}, V_{min}, and I_{min}. If in addition the ideality factor n would be known, the series resistance R_s could be inferred using equation (5.35). Since this is not the case, we propose the following method, based on equation (5.35) rewritten as

$$\gamma = n + \frac{q}{kT} R_s I_{min} . \tag{5.37}$$

Thus if I_{min} is determined for several different values of the parameter γ, we can deduce R_s from the slope of a plot of γ versus I_{min}; the ideality factor n can then be inferred from the y-axis intercept. As an example, Fig. 5.12(a) shows a plot of γ versus I_{min} for a temperature of 120 K. Linearly fitting the data, we can obtain the ideality factor, $n = 1.54$, and the series resistance, $R_s = 1.5 \times 10^{-6}\,\Omega$. Repeating this procedure for the measured data at temperatures between 110 K and 150 K, yields an average n-factor of $n = 1.5 \pm 0.1$.

The second task is now to determine the barrier height ϕ_{Bp} and AA^*. For this we define a temperature-dependent function $H(T, \gamma)$ using equation (5.36)

$$\begin{aligned} H(T, \gamma) &= q\, G_{min} + \left(\frac{\gamma - n}{\gamma\, n}\right) q V_{min} + \left(\frac{n - \gamma}{n}\right) kT \\ &= \phi_{Bp} - kT \ln(AA^*) . \end{aligned} \tag{5.38}$$

This function $H(T, \gamma)$ can directly be obtained for all the different γ values. A plot of $H(T, \gamma)$ versus temperature should give a straight line from which AA^* and ϕ_{Bp} can

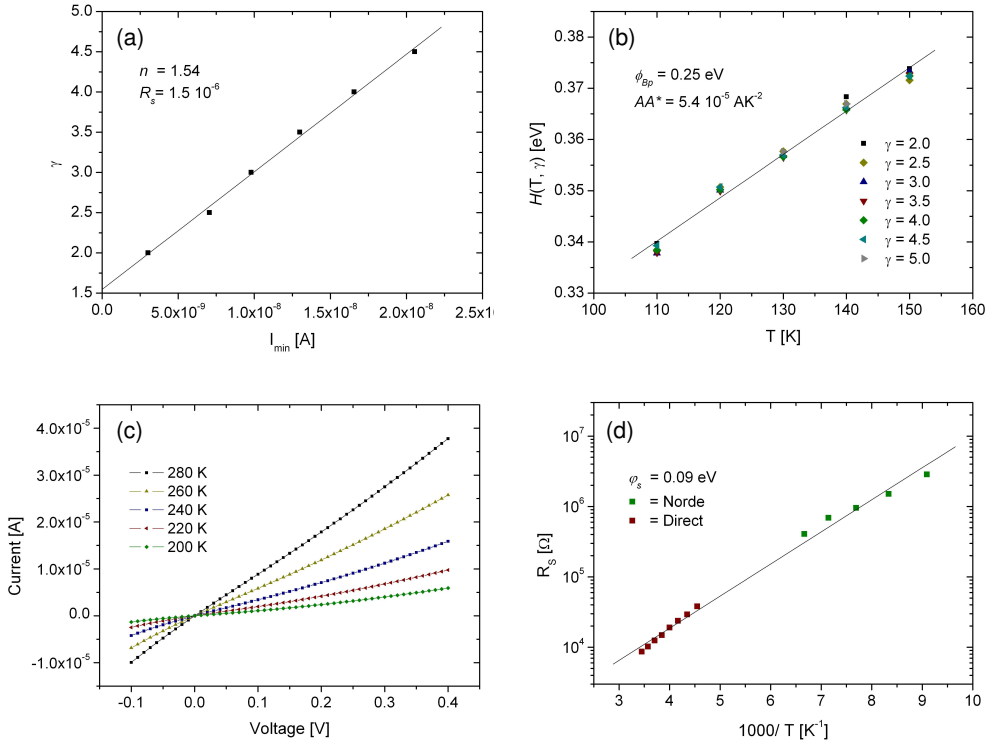

Figure 5.12: (a) γ as a function of I_{min}, see also Fig. A.32. (b) $H(T, \gamma)$ as a function of the inverse temperature, see also Fig. A.33. (c) Linear current-voltage relation at elevated temperatures, see also Fig. A.34. (d) Arrhenius plot of the series resistance, see also Fig. A.35.

be derived considering the slope and the y-axis intercept, respectively. This is shown in Fig. 5.12(b). The measured barrier height of $\phi_{Bp} = 0.25\,\text{eV}$ is a bit too small compared to the literature value of $0.34\,\text{eV}$ [Sze81d]. As mentioned before, due to the parallel switching of the nanowires, the contacts having the smallest barrier height determine the measured value of the barrier height. This might to some degree account for the deviation. Another possible reason could be that the barrier height is altered by the special way the Au/p-Si contacts were treated. However, a measured barrier height of $\phi_{Bp} = 0.25\,\text{eV}$ is close enough to the value reported in literature that we can take it as being consistent.

From the slope of the linear fit shown Fig. 5.12(b) we can obtain the product AA^* of the effective device area and the Richardson constant. Assuming a Richardson constant A^*, equal to the one of p-type silicon, $A^* = 32\,\text{A}\,\text{cm}^{-2}\,\text{K}^{-2}$ [And70], leads to an effective device area of $1.8 \times 10^{-6}\,\text{cm}^2$. This area, together with an average nanowire diameter of $50\,\text{nm}$, corresponds to approximately 1×10^5 nanowires contacted in parallel. Considering the size of the contact pad of 0.4 mm $\times$0.5 mm, we end up with a nanowire density of $0.5\,\mu\text{m}^{-2}$, which is roughly consistent with what could be expected from the scanning electron micrographs of the sample (see Fig. 5.10(b)).

Let us now focus on the series resistance. We have seen so far that for low tempera-

tures, the series resistance data can be obtained from a generalized modified Norde plot. In addition, we can also directly deduce the series resistance for temperatures $\geq 220\,\mathrm{K}$, since the current-voltage characteristic is almost linear, as shown in Fig. 5.12(c). An approximation for the temperature dependence of the series resistance is found by combining both data sets. In Fig. 5.12(d), R_s is plotted versus the inverse temperature. One can see that in a crude approximation we can assume that the series resistance depends exponentially on temperature, i.e. $R_s = 2.8\times10^2 \exp(0.09\,\mathrm{eV}/kT)\,\Omega$, which corresponds to a series resistance of roughly $1\times10^4\,\Omega$ at room temperature. Assuming an average length of the nanowires of roughly $500\,\mathrm{nm}$ and taking the hole mobility of bulk silicon ($4\times10^2\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) leads to an effective hole density of $p_{eff} \approx 5\times10^{13}\,\mathrm{cm^{-3}}$. Similar to the n-doped wires this small value for the effective hole density can be explained taking the influence of interface traps into account. Assuming a interface trap level density of $1\times10^{12}\,\mathrm{eV^{-1}\,cm^{-2}}$ we can find from Fig. 5.4(b) that the doping concentration was probably less than $2\times10^{17}\,\mathrm{cm^{-3}}$. The parameters we obtained so far are summarized in Table 5.2.

$$
\begin{aligned}
A &= 1.8\times10^{-6}\,\mathrm{cm^2} \\
\phi_{Bp} &= 0.25\,\mathrm{eV} \\
n &= 1.5 \\
R_s &= 2.8\times10^2 \exp(0.09\,\mathrm{eV}/kT)\,\Omega
\end{aligned}
$$

Table 5.2: Parameters deduced from the current-voltage characteristics of an array of p-doped nanowires.

In order to test the consistency of the extracted parameters with the measurement, the current-voltage characteristic was simulated based on the proposed equivalent circuit shown in Fig. 5.11(b). For an easier comparison, both the measured and the simulated current-voltage characteristic are shown in Fig. 5.13(a) and Fig. 5.13(b), respectively. It can be seen that the parameters of Table 5.2, determining the Au/p-Si Schottky diode and the series resistance R_s, indeed provide a good qualitative description. The most apparent deviation occurs for the reverse bias current at low temperatures. This is due to the fact that the Schottky effect and other mechanisms leading to a more pronounced voltage dependence of the reverse current have not been considered.

5.4 Conclusions of Chapter 5

The measurements of both n-doped and p-doped silicon nanowires can be consistently explained by taking the contact properties and the influence of interface states into account. The rectification direction of the Au/Si Schottky contact indicated that indeed a hole cur-

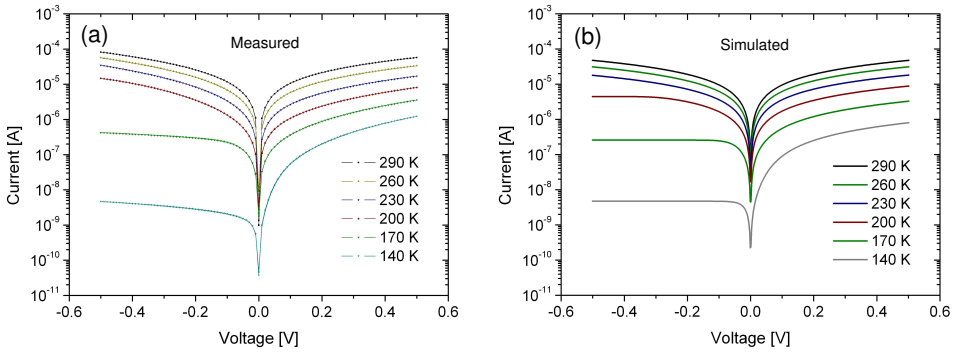

Figure 5.13: (a) Measured temperature-dependent current-voltage characteristic of an array of p-doped silicon nanowires, see also Fig. A.31. (b) Simulation of the measurement using the parameters extracted from (a), see also Fig. A.36.

rent is flowing in the p-doped nanowires, and an electron current in the n-doped nanowires. The measured Schottky barrier heights agree with the values reported in literature, if the effect of the parallel switching of the nanowires and edge effects at the metal-semiconductor contact edge are considered. The ideality factors are more or less in the expected range. Also the device areas we could derive from the contact characteristics, are consistent with the estimated contact area. The most puzzling outcome concerns the series resistance, which we could obtain by a Norde plot analysis of the measurements. This series resistance seems to be too high, if only the nominal doping of the nanowires is taken into account. However, a more detailed analysis, also considering the influence of interface traps at the Si/SiO_2 interface could resolve this apparent contradiction. It seems that our doping method produced a dopant density that is below the critical limit, necessary to prevent the nanowires from being fully depleted. For an interface trap level density of $D_{it} = 1 \times 10^{12}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-3}$ and a nanowire diameter of $50\,\mathrm{nm}$ the critical doping limit is about $10^{17}\,\mathrm{cm}^{-3}$. We believe that the dopant densities in our nanowires are lower than this threshold value and that the nanowires are therefore fully depleted, which explains their high resistance.

Chapter 6

Vertical Surround-Gate Field-Effect Transistor

The first step towards a technical realization of a nanowire logic element is the design and manufacturing of a nanowire transistor. In this respect, epitaxially grown silicon nanowires offer two advantages. First, the problem of handling and positioning nanometer-sized objects that arises in the conventional pick-and-place approach, where devices are fabricated by manipulating horizontally lying vapor-liquid-solid (VLS) grown nanowires [Cui01b, Wha03], is circumvented. And second, the vertical orientation of the nanowires permits to wrap the transistor gate around the nanowire. Such a wrapped-around gate allows better electrostatic gate control of the conducting channel and offers the potential to reduce the gate voltage [Wan04].

In this chapter, following a theoretical introduction, a generic process for fabricating a vertical surround-gate field-effect transistor (VS-FET) based on epitaxially grown nanowires is described. A first electrical characterization proving the feasibility of the process developed and the basic functionality of this device is presented and discussed.

6.1 Theory and Simulation

Figure 6.1(a) shows a schematic cross section through a conventional p-type MOSFET. In such a device, an inversion channel can be created close to the gate by applying a negative gate voltage. This forms a conducting channel that electrically connects the p-doped regions under the source and drain contacts. Using this concept, a silicon nanowire VS-FET would ideally require a nanowire that is n-doped in the region of the gate, and p-doped elsewhere. Unfortunately, such a p-n-p structure with abrupt transitions appears difficult to realize if the nanowires are grown by means of the vapor-liquid-solid mechanism [Wag64a] using gold as catalyst. The difficulty here is that the catalyst droplet might act as a reservoir for the therein dissolved dopant atoms. Consequently, only graded transitions could be obtained when switching from one dopant to the other. Instead, we used a structure consisting of an n-doped silicon nanowire grown on a p-type substrate, see Fig. 6.1(b). If the

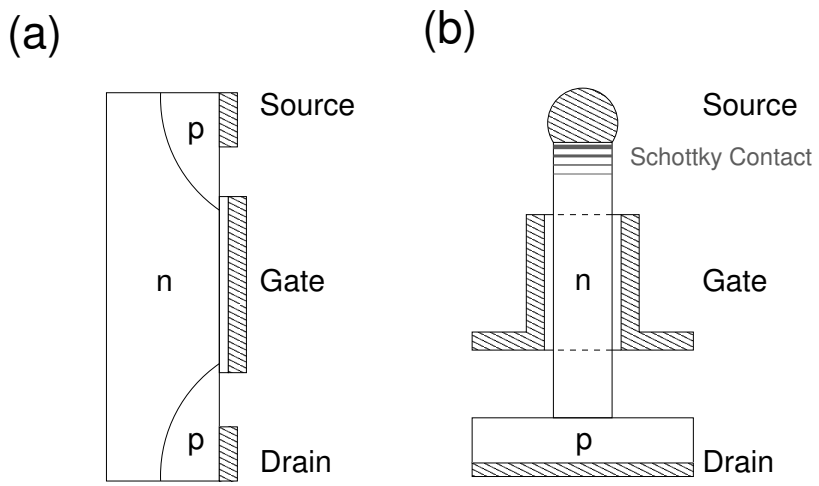

Figure 6.1: Schematics of (a) a conventional p-channel MOSFET, (b) a silicon nanowire vertical surround-gate field-effect transistor.

gate-drain and gate-source distances are not too large, it is nevertheless possible to create an inversion channel along the entire length of the nanowire. In the proposed configuration, the p-n-junction at the source contact, shown in Fig. 6.1(a), is replaced by a Au/n-Si Schottky contact at the nanowire tip.

6.1.1 MOS Capacitor

Before discussing the properties of a vertical nanowire surround-gate field-effect transistor, let us first consider the effect of applying a gate voltage on the effective charge carrier concentration in the nanowire. The electrical measurements presented in the last chapter revealed that with our method of doping the nanowires, the nanowires are usually fully depleted. Thus we can use equation (5.25) to describe the effective electron density n_{eff} of the nanowire.

$$n_{eff} = n_o \exp(\beta\psi_s)\frac{4\epsilon_s}{\beta\rho a^2}\Big(\exp\big(\frac{\beta\rho a^2}{4\epsilon_s}\big) - 1\Big)\,, \tag{6.1}$$

where $\beta = q/kT$, and ρ, ϵ_s, and a are the charge density, the dielectric constant, and the radius of the nanowire, respectively. If $\rho \ll 4\epsilon_s/(\beta a^2)$ we can expand the exponential in (6.1) in a Taylor series expansion to first order. The above condition is satisfied if the dopant density in a wire of radius $a = 25$ nm is smaller than $1{\times}10^{17}$ cm^{-3}. A Taylor series expansion to first order gives

$$n_{eff} = n_o \exp(\beta\psi_s)\,, \tag{6.2}$$

where n_o is defined in equation (5.11). Clearly, in this approximation, the effective electron concentration n_{eff} is determined by the value of the surface potential. Using equation (5.12) we can write the charge density in the wire as

$$\rho = q\Big(p_o \exp(-\beta\psi_s) - n_o \exp(\beta\psi_s) + N_D - N_A\Big)\,. \tag{6.3}$$

Compared to the previous chapter, where we approximated that $\rho = q(N_D - N_A)$, this approximation goes one step further. It is implicitly assumed that the charge density is constant within the nanowire - a reasonable approximation for small radii.

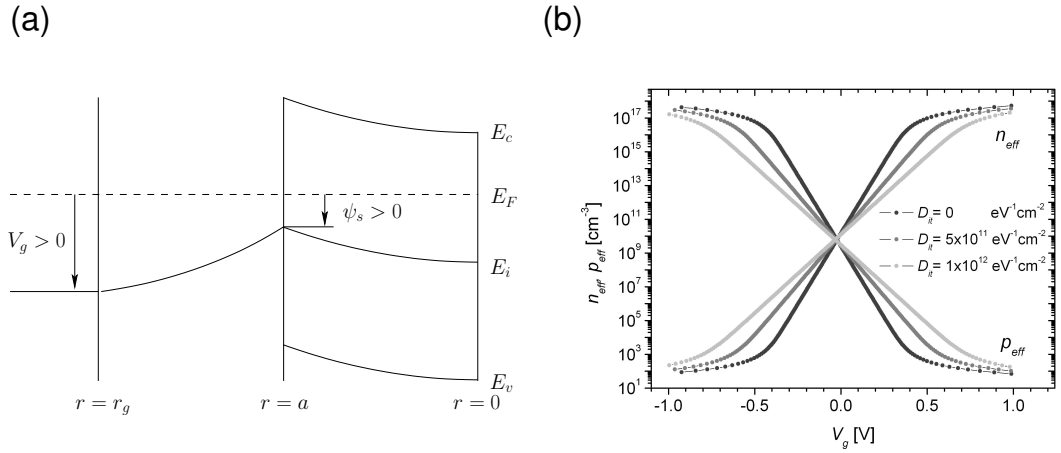

Figure 6.2: (a) Schematic of the electrostatic potential and the bandstructure of a circular MOS capacitor. (b) Effective electron and hole density of an n-doped ($N_D = 1 \times 10^{16}\,\mathrm{cm}^{-3}$) circular surround-gate MOS capacitor for different interface trap level densities D_{it} as a function of the gate voltage V_g, see also Fig. A.37.

To simplify the electrostatic problem, we only consider the two-dimensional problem of a circular slice of silicon of radius a covered with SiO_2 of thickness $(r_g - a)$, surrounded by a circular gate of radius r_g. The electrostatic situation for the VS-FET is schematically depicted in Fig. 6.2(a). Furthermore, we neglect the work function difference between the gate metal and silicon, we neglect charges inside the oxide layer ($Q_{ot} = Q_m = 0$), and consider only the effect of fixed oxide charges, Q_f, and trapped interface charges, Q_{it}, on the effective charge carrier density. The boundary conditions for the problem are determined by the gate voltage, as shown in Fig. 6.2(a). Under these conditions, the electrostatic potential is given by

$$\psi(r) = \begin{cases} \psi_s - \frac{\rho}{4\epsilon_s}(r^2 - a^2) & 0 \le r < a \\ \psi_s - \frac{a^2}{2\epsilon_{ox}} \ln(\frac{r}{a})\big(\rho + \frac{2}{a}(Q_f + Q_{it})\big) & a \le r < r_g \end{cases} . \tag{6.4}$$

Using equation (5.17) and the boundary condition $\psi(r_g) = V_g$ we arrive at an expression that directly relates the gate voltage to the surface potential ψ_s

$$V_g = \psi_s - \frac{a^2}{2\epsilon_{ox}} \ln(\frac{r_g}{a}) \Big\{ q\Big(p_o \exp(-\beta\psi_s) - n_o \exp(\beta\psi_s) + N_D - N_A\Big) + \\ + \frac{2}{a}\Big(Q_f - q^2 D_{it}\psi_s\Big) \Big\} , \tag{6.5}$$

or equivalently to the effective electron concentration, using equation (6.2),

$$V_g = \frac{kT}{q}\ln(\frac{n_{eff}}{n_o}) - \frac{a^2}{2\epsilon_{ox}}\ln(\frac{r_g}{a})\ \left\{ q\Big(\frac{p_o n_o}{n_{eff}} - n_{eff} + N_D - N_A\Big) + \right.$$
$$\left. + \frac{2}{a}\Big(Q_f - kTqD_{it}\ln(\frac{n_{eff}}{n_o})\Big)\right\}. \qquad (6.6)$$

Clearly, the only effect of fixed oxide charges, Q_f, is to shift the gate voltage. In Fig. 6.2(b), the effective electron and hole concentrations of a lowly n-doped nanowire ($N_D = 1 \times 10^{16}\,\mathrm{cm}^{-3}$) of 25 nm in radius, as a function of the gate voltage V_g, is plotted for different interface trap level densities D_{it}. The gate is located at $r_g = 35\,\mathrm{nm}$, corresponding to an oxide thickness of 10 nm. One can see in Fig. 6.2(b) that a positive gate voltage leads to the accumulation of electrons in the nanowire, whereas a negative gate voltage results in a charge carrier inversion. An inversion in the nanowire is what we need for our surround-gate silicon nanowire FET. The presence of interface traps reduces the response of the device with respect to the applied gate voltage, but does not alter the overall behavior considerably.

However, for our approach of fabricating vertical surround-gate FETs, using n-doped nanowires grown on a p-doped substrate, an additional complication arises from the fact that the width of the surround-gate is much smaller then the length of the nanowire. One can expect that in order to create an inversion along the entire nanowire, higher gate voltages have to be applied than shown in Fig.6.2(b). To get a better impression of the nanowire response to the application of a gate voltage, simulated band structures and charge carrier densities are presented in the following.

6.1.2 VS-FET Simulation

The simulation was performed using the WIAS-TeSCA program [WT03], designed for 2D device simulation, but also able to solve radially symmetric 3D problems. The geometry we defined for our VS-FET problem is a circular nanowire, 50 nm in diameter and 400 nm in length, which is covered by 15 nm of SiO_2. The n-doped nanowire ($N_D = 1{\times}10^{16}\,\mathrm{cm}^{-3}$) is attached to a 500 nm thick p-doped substrate ($N_A = 1 \times 10^{11}\,\mathrm{cm}^{-3}$). The aluminum gate has a width of 80 nm and is located 200 nm above the substrate. The drain contact to the substrate is assumed to be ohmic, whereas the source contact was modelled as a Schottky contact. Unfortunately, the program does not offer the possibility of introducing a constant Si/SiO_2 interface trap level density, wherefore the effect of depletion caused by the Si/SiO_2 interface is not properly reproduced. Nevertheless, the simulation provides some insight regarding the way the inversion region spreads along the nanowire. Figure 6.3 shows on the left the simulated charge carrier density for three different gate voltages, and on the right the corresponding band structures. The source-drain bias is set to zero. For zero gate voltage, charge carrier density and band structure are shown in Fig. 6.3(a) and Fig. 6.3(b). The junction between the nanowire and the substrate is located at $x = 0$; with the substrate extending to negative and the nanowire extending to positive x-values. One can see in Fig. 6.3(a) that the crossing of the charge carrier curves, i.e. the point at which

the Fermi level is in the midgap position (see Fig. 6.3(a)), is shifted into the substrate by about $150\,\text{nm}$. This is due to the lower doping of the substrate compared to the nanowire. The nanowire itself shows the expected electron concentration of $1 \times 10^{16}\,\text{cm}^{-3}$. Only in the region $x > 250\,\text{nm}$, close to the Schottky contact at the tip, the electron density is reduced.

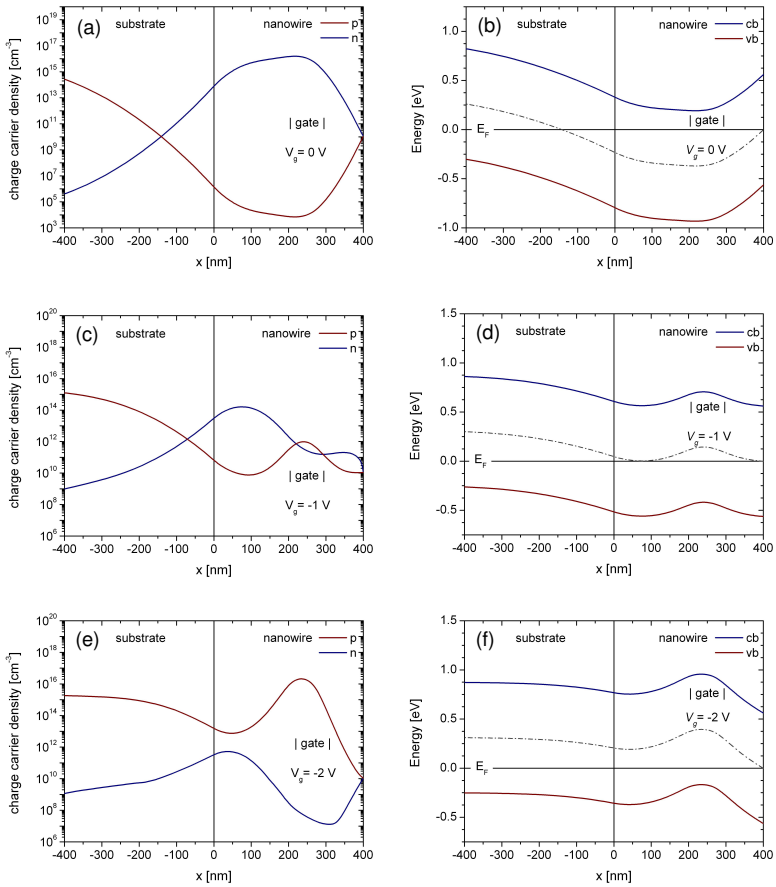

Figure 6.3: $V_{DS} = 0\,\text{V}$. (a) Charge carrier density for $V_g = 0\,\text{V}$, see also Fig. A.38. (b) Bandstructure for $V_g = 0\,\text{V}$, see also Fig. A.39. (c) Charge carrier density for $V_g = -1\,\text{V}$, see also Fig. A.40. (d) Bandstructure for $V_g = -1\,\text{V}$, see also Fig. A.41. (e) Charge carrier density for $V_g = -2\,\text{V}$, see also Fig. A.42. (f) Bandstructure for $V_g = -2\,\text{V}$, see also Fig. A.43.

By applying a sufficiently negative gate voltage $V_g = -1\,\text{V}$, shown in Fig. 6.3(c-d), an inversion region in the nanowire is created directly under the gate. This can best be seen in Fig. 6.3(c), where in the region of the gate the hole concentration exceeds the electron concentration. However, a gate voltage of $-1\,\text{V}$ is insufficient to create an inversion along the entire nanowire. Both the region between gate and substrate ($0\,\text{nm} > x > 200\,\text{nm}$) and the region between gate and nanowire tip ($280\,\text{nm} < x < 400\,\text{nm}$) are not inverted, which would hinder the flow of a hole current through the nanowire. This changes if we increase the gate voltage further to $V_g = -2\,\text{V}$, as shown in Fig. 6.3(e-f). Now the entire

nanowire is inverted and a hole current can flow through the wire. In order to give also

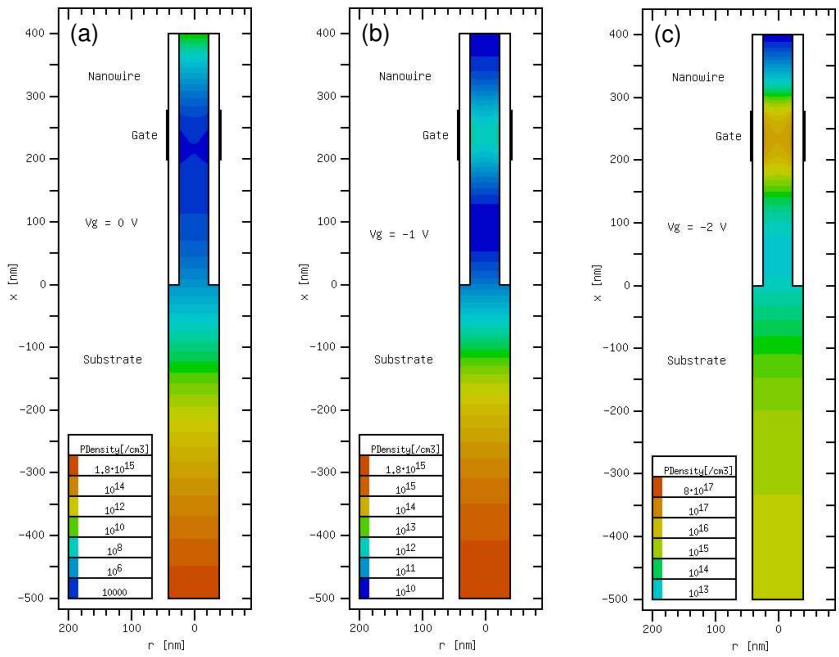

Figure 6.4: $V_{DS} = 0\,\mathrm{V}$. (a) Charge carrier density for $V_g = 0\,\mathrm{V}$, see also Fig. A.44. (b) Charge carrier density for $V_g = -1\,\mathrm{V}$, see also Fig. A.45. (c) Charge carrier density for $V_g = -2\,\mathrm{V}$, see also Fig. A.46.

an impression of the radial distribution of the charge carriers, the charge carrier density is shown in Fig. 6.4(a)-(c) for $V_g = 0\,\mathrm{V}$,$V_g = -1\,\mathrm{V}$, and $V_g = -2\,\mathrm{V}$, respectively. Hardly any radius dependence can be seen, which justifies our previous assumption of a constant charge density within the nanowire. Nevertheless, Fig. 6.4(a-c) nicely shows how upon the application of a gate voltage, the nanowire becomes inverted. Note that the color coding changes from Fig. 6.4(a) to Fig. 6.4(c).

6.2 Experimental

6.2.1 Nanowire Growth

The silicon nanowires were produced by chemical vapor deposition (CVD) in ultra high vacuum (UHV) environment. For this purpose, (111) oriented boron-doped ($> 5\,\Omega$cm) 100 mm silicon wafers were cleaned (RCA cleaning), dipped into diluted hydrofluoric acid, and immediately transferred into the UHV system. A thin layer of gold was in situ deposited onto the hydrogen-terminated silicon wafer in stripes of a few hundred micrometers in width by means of a shadow mask. A radiative heater was used to anneal the wafer at 450°C for 30 min to break up the gold film and create the Au/Si alloy droplets necessary for nanowire growth. The temperature was then lowered to 320°C and a small amount

of antimony was deposited onto the Au/Si droplets by an e-beam evaporation source in order to inject the dopant into the droplets. The temperature was then raised again to 450°C, and the UHV chamber flooded with diluted silane (5 % in argon) until a pressure of 1.9 mbar was reached. Under constant pressure, nanowire growth proceeded for a total of twelve minutes. The resulting nanowires have diameters of around 40 nm and an aspect ratio of approximately ten. The p-type silicon substrate was metalized with platinum and aluminum to create a backside electrical contact to the substrate.

6.2.2 VS-FET Manufacturing

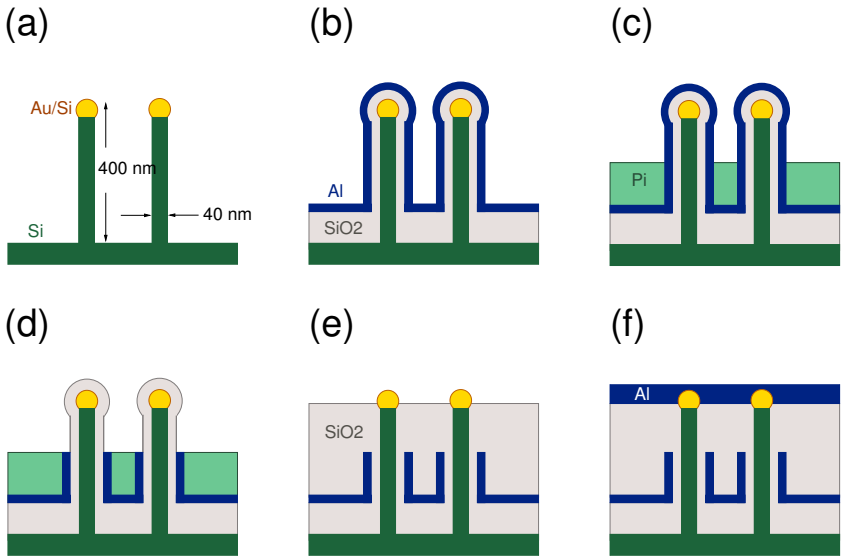

Figure 6.5: Nanowire VS-FET process flow. (a) Vertically grown silicon nanowires. (b) After deposition of SiO_2 layers and Al gate metal. (c) After polyimide deposition and polyimide RIE etching. (d) After Al wet chemical etching. (e) After polyimide removal, SiO_2 deposition and SiO_2 RIE etching. (f) After deposition of Al as source metal.

The first step of the VS-FET processing is the deposition of the SiO_2 gate insulator. Therefore, the silicon nanowires are encapsulated with a uniform, approximately 10 nm thick, CVD-grown SiO_2 layer as gate dielectric. In the second step, a spin-on-glass (Futurrex IC1-200) is deposited by spin-coating and thermally cured at 400°C for 30 min under nitrogen. This second SiO_2 layer ensures a better electrical insulation of the metal gate from the silicon substrate, the drain contact, so that leakage currents are avoided. As gate metal, an aluminum layer is deposited by e-beam evaporation to cover the SiO_2-encapsulated silicon nanowire with a uniform thickness of 30 nm. A schematic of the sample after these processing steps is shown in Fig. 6.5(b).

Afterwards the sample was spin-coated with a layer of polyimide (HD Microsystems), which was thermally cured at 350°C for 30 minutes. The polyimide layer serves as an etchstop for the subsequent wet-chemical etching step that removes the upper part of the

gate metalization (see Fig. 6.5(d)). To define the gate length, the polyimide was etched down in a reactive ion etching (RIE) system (Oxford Plasmalab) until the nanowire tips extended about 150 nm above the polyimide surface, see Fig.6.5(c). After the wet-chemical etching, the sacrificial polyimide layer was entirely removed by an O_2 plasma treatment.

In the next step, the silicon nanowires are completely embedded in SiO_2 by spin-coating a sufficiently thick layer of spin-on-glass on top of the sample followed by thermal curing. RIE is used to free the Au/Si caps of the nanowire tips from the SiO_2 deposited (see Fig. 6.5(e)). Finally, a 100-nm-thick layer of aluminum or titanium is deposited to contact the Au/Si nanowire tips and thus establish the source contact. An advantage of this process is that the fabrication of the VS-FET does not include any chemical-mechanical polishing step. In addition, the process flow developed is generic and can therefore be used with any other nanowire/substrate combination.

6.3 Results and Discussion

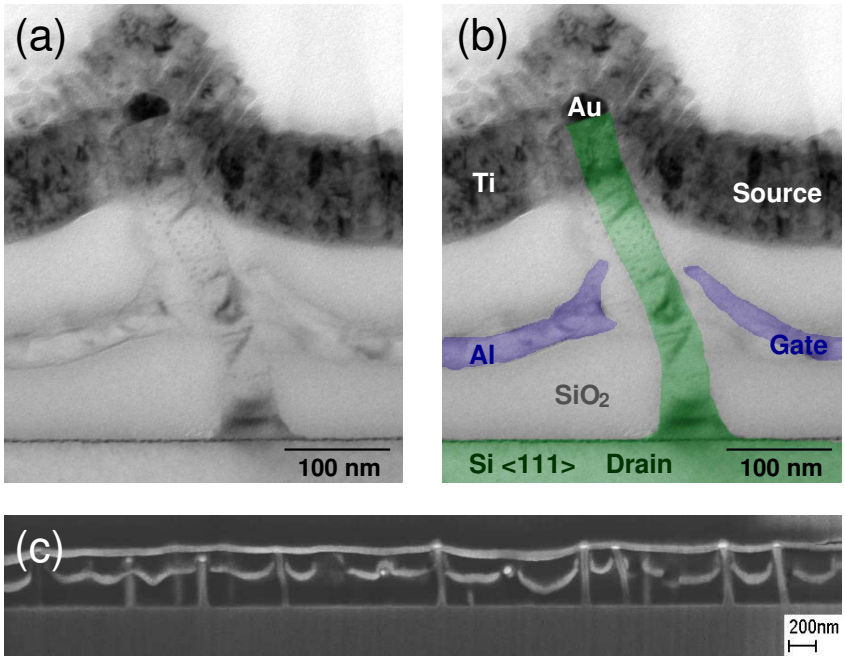

Figure 6.6: (a) TEM image of a silicon nanowire VS-FET (exclusively produced for TEM study). (b) Colored TEM image; green: silicon, blue: aluminum. (c) SEM image of a sample cross section made by FIB. Gate and source metal is aluminum.

A transmission electron micrograph (TEM; Philips CM20) of the resulting VS-FET is shown in Fig. 6.6(a-b). Because of the low contrast of aluminum compared with silicon or SiO_2, this TEM-image is reproduced in Fig. 6.6(b) with aluminum and silicon colored in blue and green, respectively. One can clearly see the nanowire, epitaxially grown on the silicon surface, with the gate surrounding the nanowire approximately at mid-height.

The bending of the nanowire is probably due to stress during spin-on-glass coating and/or polyimide curing. By optimizing the layer deposition and curing procedure, the bending of the nanowires could be strongly reduced, as shown in the cross section scanning electron micrograph of Fig. 6.6(c). This sample was fabricated using aluminum for both source and gate.

For the electrical measurements, the nanowires were grown on the substrate in stripe-shaped regions of a few hundred micrometers in width. The gate and source contacts were defined using optical lithography and lift-off techniques. Figure 6.7 (a) shows a colored top-view optical micrograph of the contacts. The active area where nanowires are contacted is on the order of 10^{-1} mm^2 and is defined by the width of the source contact and the width of the stripe. The average distance between individual nanowires is about 1 μm, which translates to an estimated 10^4 to 10^5 silicon nanowires contacted in parallel by the source and drain contact. A schematic 3D picture (Fig. 6.7(b)) illustrates the vertical position of the different layers. To contact the gate electrically, it is necessary to remove the SiO_2 layer that covers the gate contact. This was done in an anisotropic RIE step, using the metal source contact as etching mask. Electrical measurements were performed using

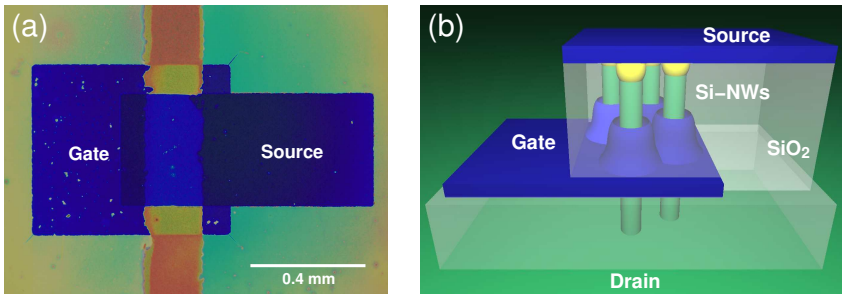

Figure 6.7: (a) False-colored top-view optical micrograph of the contact arrangement. The red and yellow stripe is the region where nanowires are grown. The grayish-green areas to the left and right are regions without nanowires. The blue areas are the Al source and gate contact. (b) Schematic 3D side view of the contact arrangement.

an Agilent 4155C parameter analyzer. The output characteristics of a silicon nanowire VS-FET device (10^4 to 10^5 silicon nanowires contacted in parallel), processed with the method described is shown in Fig. 6.8(a) for gate voltages V_G between $+3$ and -4 V. For positive drain-source voltages V_{DS}, the drain-source current I_{DS} strongly depends on V_G. With increasing negative V_G, the drain-source current increases, whereas with increasing positive V_G it is reduced. For negative V_{DS}, the gate-voltage dependence of I_{DS} is similar but less pronounced. Such a behavior is characteristic of hole transport and is indicative of a gate-driven formation of an inversion layer of holes in the vicinity of the gate. In the case of inversion, the holes in the inversion channel can inundate the n-doped nanowire. Thus, for negative V_G, our Si-nanowire VS-FET seems to function as a normal p-channel MOSFET. The nanowire VS-FET is normally on, and turns off only if a positive gate voltage is applied. This indicates a shift of the threshold voltage that can be attributed to trapped and/or interfacial charges. Considering the characteristic of a p-channel MOSFET,

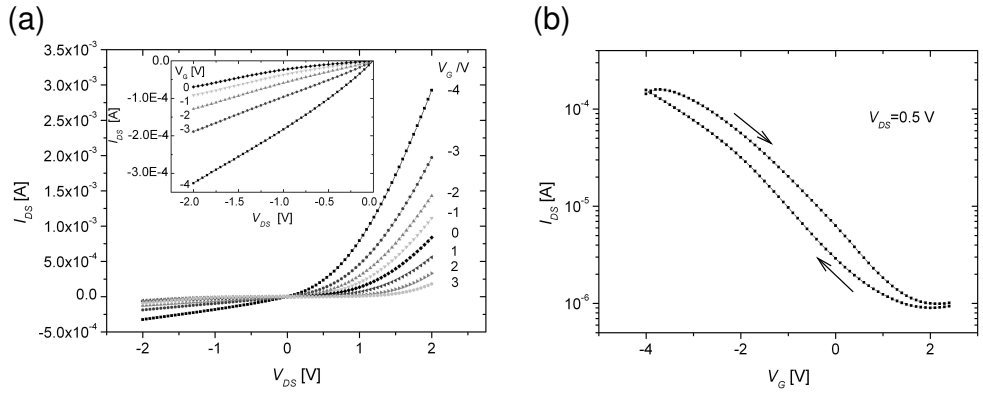

Figure 6.8: (a) Output characteristics of an array of VS-FETs for different gate voltages, see also Fig. A.47. (b) Drain-source current I_{DS} vs. gate voltage V_G, $V_{DS} = 0.5$ V, see also Fig. A.48.

one would expect a linear behavior of I_{DS} at low V_{DS} in the third quadrant, followed by a saturation of I_{DS} as V_{DS} increases. The inset of Fig. 6.8(a) shows a closeup of the third quadrant: For small V_G, the increase of I_{DS} at low V_{DS} is nonlinear, indicating a series resistance that might be attributed to an incomplete formation of the inversion channel close to the interface of the p-type substrate and the n-type nanowires. Therefore, no extraction of a charge carrier mobility in the linear regime can be performed. Moreover, for the VS-FET no saturation of I_{DS} can be observed, as is the case for other NW FETs [Ng04, Cui00]. Furthermore, the inset of Fig. 6.8(a) shows that the On/Off ratio at $V_{DS} = -0.5$ V is approximately six. In Fig. 6.8(b) the drain-source current I_{DS} at $V_{DS} = 0.5$ V is plotted versus V_G. Considering the number of nanowires contacted in parallel, it is most remarkable that the current changes by more than two orders of magnitude if the gate voltage is decreased from 2 to -4 V. As discussed above, this effect can be explained by the creation of an inversion channel in the nanowire. The small slope of the curve in Fig. 6.8(b) is probably caused be the short gate length compared to the necessary length of the inversion channel. Also the interface states located at the Si/SiO_2 interface might be responsible for the reduced slope. Besides, the existence of charged traps at the Si/SiO_2 interface could possibly also explain the hysteresis observed in Fig. 6.8(b).

6.4 Conclusions of Chapter 6

In conclusion, we have presented a generic process flow to fabricate silicon nanowire vertical surround-gate field-effect transistors (VS-FET). The intrinsic advantage of the process developed is that no chemical mechanical polishing steps, which are difficult to control at this length scale, are required. In the demonstrated device, n-doped silicon nanowires, grown epitaxially on a p-doped substrate, were used as active material. The array of VS-FETs exhibited a gate-voltage-dependent current increase by more than two orders of magnitude.

Summary

The scope of this last part of the thesis is to summarize and discuss the results, described in detail in the chapters before. As indicated by the title of the thesis, "Silicon Nanowires: Synthesis, Fundamental Issues, and a First Device" the results presented in the five chapters therein are dedicated to three more or less independent topics, which we tried to order into what appeared to us the most logical way, i.e. starting with experimental results on the synthesis of silicon nanowires in Chapter 1, continuing with fundamental growth related issues in Chapter 2 to 4, and ending finally with the electrical properties in Chapter 5 and the fabrication of a potential electronic silicon nanowire device in Chapter 6.

It should be additionally remarked here that although especially Chapters 2, 4 and 5 treated general silicon nanowire issues, we tried to focus on homo-epitaxially grown silicon nanowires. At least from our point of view, these offer the greatest opportunities with regard to future silicon nanowire devices. Especially concerning sensors and electronic applications, epitaxial silicon nanowires offer the decisive advantage that the nanowires are both mechanically and electrically well-connected to the substrate material. Moreover, especially the positioning of the silicon nanowires on the substrate is far easier in case of epitaxially grown nanowires.

For these reasons we concentrated on the epitaxial growth of silicon nanowires, which is described in detail in Chapter 1. We used a chemical vapor deposition process with silane as precursor gas and, in most cases, gold as catalyst at low synthesis temperatures between $400\,^{\circ}\mathrm{C}$ and $500\,^{\circ}\mathrm{C}$. At these temperatures, the catalyst forms a liquid alloy, and growth can be described by the vapor-liquid-solid (VLS) mechanism. Higher synthesis temperatures than $500\,^{\circ}\mathrm{C}$ are not desirable from an application point of view as they may prevent some types of pre-growth processing of the substrate used. Controlled growth of single-crystalline silicon nanowires with radii between $15\,\mathrm{nm}$ and $100\,\mathrm{nm}$ could be achieved that way, with at most about 70% of the nanowires straight and perpendicular on the substrate. Although this is as good or even superior to what has been achieved by other groups concerning the low temperature synthesis of silicon nanowires, it is clear that a yield of 70% is by far not sufficient for serious applications. So there is still a strong need for an improvement of the synthesis quality in general. But even if perfect gold-catalyzed silicon nanowires could be produced, their use as parts of electronic devices is questionable, as gold is usually deemed as being incompatible with existing electronics fabrication technology. Thus from this point of view, the replacement of gold by an alternative catalyst material is of considerable interest. We tested six different metals - Pd, Fe, Dy, Bi, In,

and Al. It was found that aluminum is indeed a very promising alternative to gold, leading to the growth of single-crystalline epitaxial silicon nanowires. Recent results indicate that well-oriented almost non-tapered epitaxial silicon nanowires can be synthesized with aluminum as catalyst [Wan]. The maximum yield of perfectly oriented nanowires produced that way turns out to be even higher than for the gold-catalyzed nanowires. The fact that so far only little is reported in literature on the use of aluminum as a catalyst for silicon nanowire growth is probably due to the fact that aluminum oxidizes too easily under non ultra-high vacuum conditions.

Although the method we used to synthesize most of our silicon nanowires - the VLS mechanism - has been discovered about forty years ago, its implications for the nanowire morphology are not fully understood yet. Three fundamental morphology related issues of the VLS growth of silicon nanowires are treated in Chapters 2 to 4. Chapter 2 focusses on the diameter dependence of the growth velocity of silicon nanowires synthesized via the VLS mechanism. This is insofar an important issue as the length of the nanowires is usually adjusted via the growth time, which requires an understanding of the factors that determine the growth velocity. Concerning the chemical vapor deposition of silicon nanowires it is generally accepted that two sub-processes may influence the nanowire growth velocity. These are the incorporation of silicon at the surface of the liquid catalyst droplet and the crystallization of the silicon nanowire at the catalyst-nanowire interface. However, despite or better because of good arguments in favor of either of these sub-processes it was discussed for a long time, whether in general the incorporation or the crystallization process effectively determines the growth velocity. However, considering different apparently contradictory experimental observations we found that this growth velocity riddle can only be solved if the assumption of a single rate-determining step is rejected. By taking the interplay of both processes, the incorporation and the crystallization process, at steady state conditions into account, we derive in Chapter 2 a model for the radius dependence of the growth velocity. In terms of our model the apparently contradictory experimental observations could be reconciled and consistently explained. Furthermore it was found that the radius dependence of the growth velocity, caused by the Gibbs-Thomson effect, is strongly affected by the applied growth conditions - an insight that might be used to optimize the growth conditions.

Chapter 3 dealt with a subject characteristic for the epitaxial growth of silicon nanowires, namely the expansion of the nanowire diameter close to where the nanowire is attached to the substrate. Although at first glance this seems to be a detail of minor importance, it is relevant for a potential post-growth processing of the nanowires, since the diameter expansion at the nanowire base will necessarily affect the shape of layers deposited onto the nanowires. We could show that the origin of the diameter expansion is directly related to the equilibrium mechanics of the liquid catalyst droplet in the initial stage of growth. Considering the influence of surface tensions and additionally assuming a possible line tension contribution, we were able to model the shape of the diameter expansion with surprising accuracy. An additional outcome of our model was that depending on sign and magnitude of the line tension, the usual nanowire growth mode may be inhibited. Instead of

nanowires, hillock-like structures of finite height may develop, if the line tension exceeds a certain limit. This line tension criterion could possibly be the cause for the growth of hillock-like structures we found on highly doped silicon substrates.

The focus of Chapter 4 is on the crystallographic growth direction of silicon nanowires, a subject of utmost importance, especially for epitaxially grown silicon nanowires. The experimental results we presented in Chapter 4 clearly indicated that the growth direction of silicon nanowires grown with gold as catalyst is diameter-dependent and that furthermore the preferential growth direction changes from <111> to <110> at a diameter of about 30 nm. The same phenomenon has also been observed by Wu et al. [Wu04a] analyzing silicon nanowires grown on oxidized silicon substrates. Since the nucleation conditions are totally different we concluded that the diameter dependence of the growth direction is more an energetic and not so much a nucleation phenomenon. To explain the origin of this direction change, we proposed a model that takes surface tension of the silicon nanowire and interface tension of the catalyst-nanowire interface into account. According to our model, silicon nanowires of large diameters choose the direction having the smallest interface tension, whereas, as a consequence of the increased surface-to-interface ratio, silicon nanowires with diameters smaller than 30 nm choose the direction with the smallest surface tension. This argument can also be used to explain the change of the growth direction that can also be observed for ZnSe nanowires, as reported by Cai et al. [Cai06]. The knowledge that the growth direction changes at a diameters of about 30 nm is without doubt very helpful for the production of silicon nanowires. However, this does not imply that well-aligned silicon nanowires with diameters smaller than 30 nm can be synthesized easily, as thin silicon nanowires may choose between different crystallographically equivalent directions of the <110> family. One way to solve this problem could be the synthesis of [100]-oriented nanowires on (100)-oriented substrates, as for these no equivalent possible growth directions exist. According to our model, the growth of <100>-oriented nanowires might be forced by a modification of the surface and interface tensions, which could possibly be achieved by changing the surface termination of the nanowires. However, whether this idea really works has not been demonstrated yet.

After these synthesis-related considerations, the electrical properties of p-doped and n-doped silicon nanowires are investigated in Chapter 5. One purpose of the investigations was to figure out whether our doping method is effective or not. In our case a doping of the nanowires was achieved by evaporating a small amount of boron for the p-doped and antimony for the n-doped wires onto the gold catalyst droplet directly prior to growth. The doped epitaxial grown silicon nanowires were then embedded in a SiO_2 matrix and the gold tips of the nanowires contacted with a metal top contact. Temperature-dependent two-terminal measurements were carried out, and the analysis of the measurements revealed a typical Schottky-contact signature, which could be identified as being caused by the Au/Si contact of the catalyst particle. In addition, and despite of the doping, the measurement indicated a low effective charge carrier concentration in the silicon nanowires. In order to explain the origin of this low charge carrier concentration, we derived a model to evaluate the effect of interface states and interface charges located at the Si/SiO_2 interface on the

charge carrier density of the silicon nanowires. It was found that depending on the interface state and the dopant density, a critical nanowire radius exists. Only for nanowires having a radius larger than this critical radius, the charge carrier density agrees approximately with the dopant density. If, however, the nanowire radius is smaller than the critical radius, the charge carrier density is strongly reduced by the presence of the interface states. We believe that the radius of the nanowires we investigated was below this critical radius, which in turn would explain the low charge carrier concentration observed. Both the measurements and the model underscored the importance of a controlled surface treatment of the silicon nanowires in order to achieve the desired electrical properties.

After these preparatory works we concentrated in Chapter 6 on the fabrication of an array of vertical surround-gate field-effect transistors (VS-FETs) based on VLS-grown silicon nanowires. This is the first time that the fabrication of VS-FETs based on epitaxial VLS-grown silicon nanowires has been demonstrated, although similar approaches have been published recently by different groups [Ng04, Tan05, Gol06]. The advantage of wrapping the transistor gate around the semiconductor is that it allows a better electrostatic control of the conducting channel compared to the standard device geometry, with the gate located only on one side of the semiconductor. To simplify the fabrication process, we used n-doped silicon nanowires grown epitaxially on a p-doped substrate instead of a p-n-p silicon structure, usually employed for field-effect transistors. In order to test the functionality of such a structure a numerical device simulation was performed using the WIAS TESCA program, and it was found that, given the gate voltage is high enough, a inversion region that spreads along the entire n-doped nanowire can be created. The transistor fabrication itself comprised a sequence of deposition and etching steps, by which the vertical nanowires were equipped with a short aluminum surround-gate located approximately at midheight. An electrical characterization of the thereby produced arrays of VS-FETs revealed the basic functionality of the devices.

Although this is a promising first step towards a potential application of silicon nanowires, it is still a long way till silicon nanowires might finally be used - in one way or the other - in functional integrated devices. Clearly, this requires a better understanding of the silicon nanowire growth process and a much better control of the nanowire morphology and the electrical properties. To achieve this will also be our task for future work in the field of silicon nanowires.

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Appendix

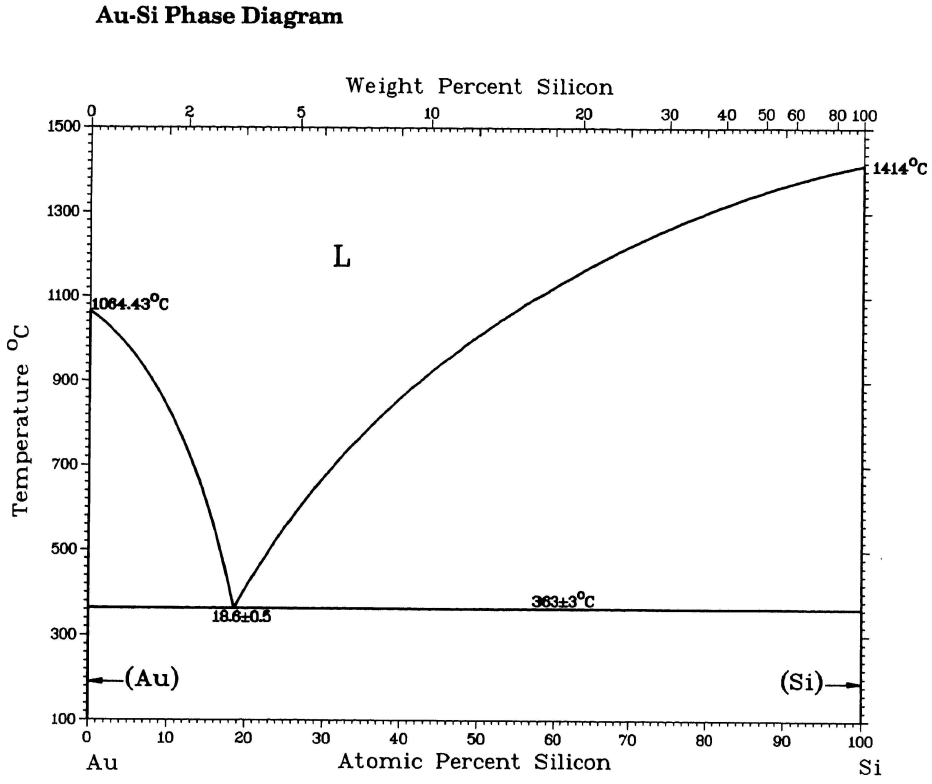

Figure A.1: Au-Si phase diagram [Mas90a], Fig. I.1(b) magnified.

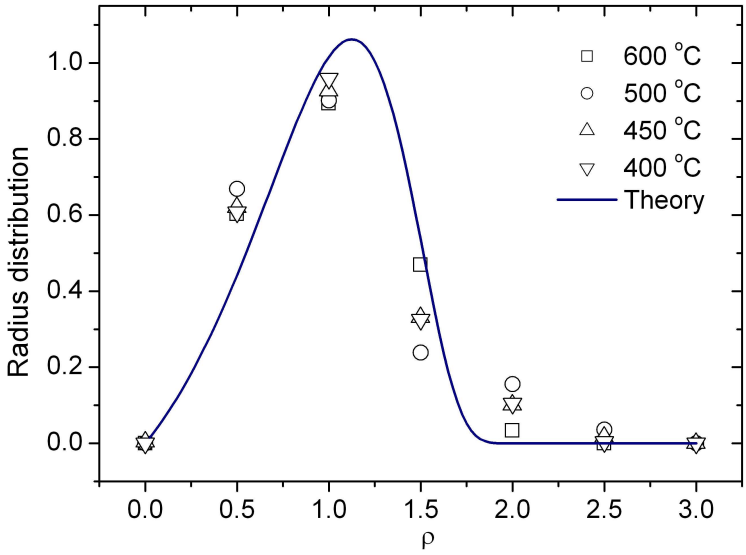

Figure A.2: Radius distribution of Au/Si droplets after 20 minutes of annealing at different temperatures, Fig. 1.2(a) magnified.

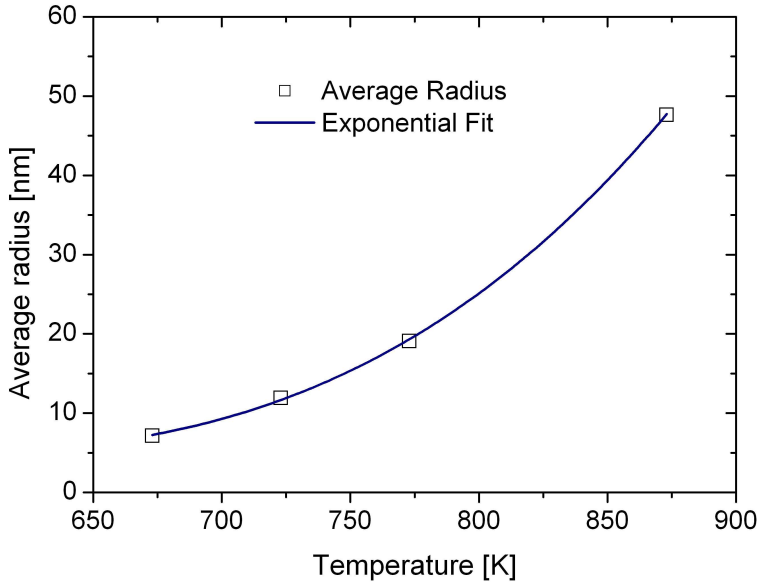

Figure A.3: Mean radius of Au/Si droplets as a function of the annealing temperature, Fig. 1.2(b) magnified.

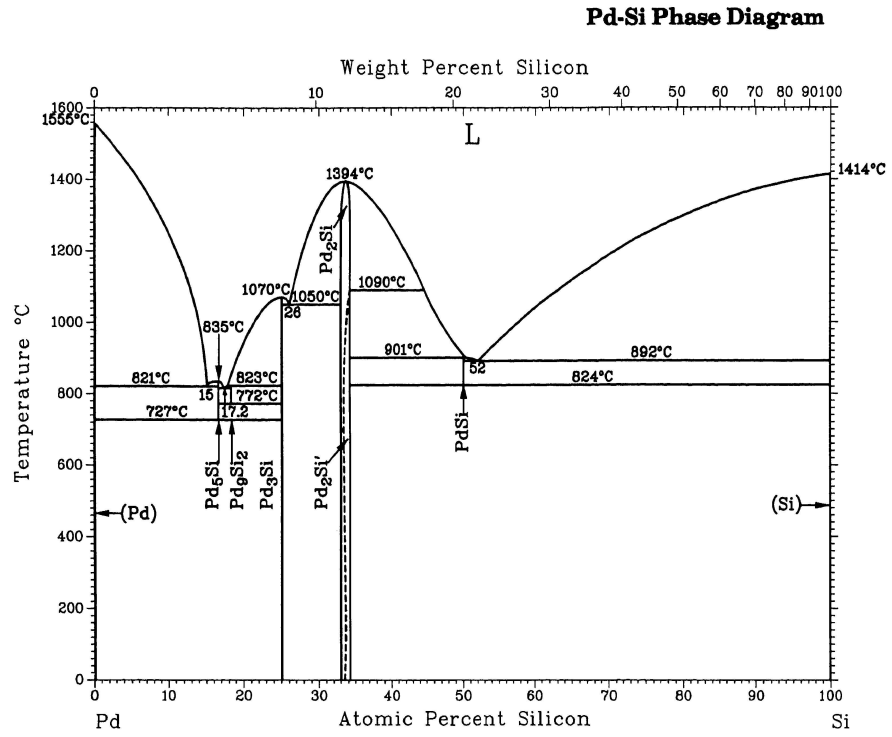

Figure A.4: Pd/Si phase diagram [Mas90b], Fig. 1.5(a) magnified.

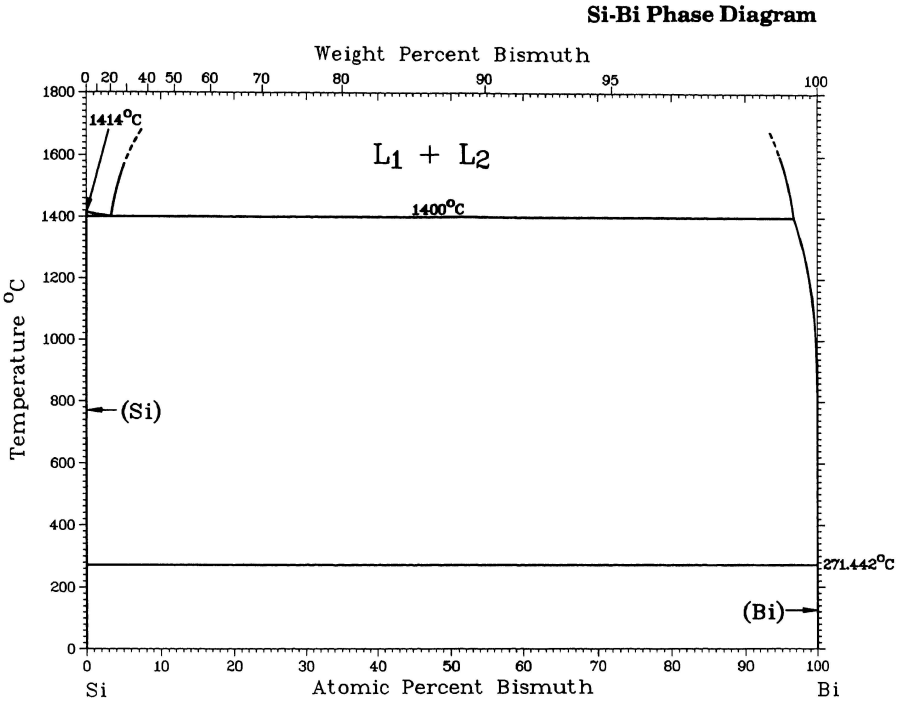

Figure A.5: Bi-Si phase diagram [Mas90a], Fig. 1.8(a) magnified.

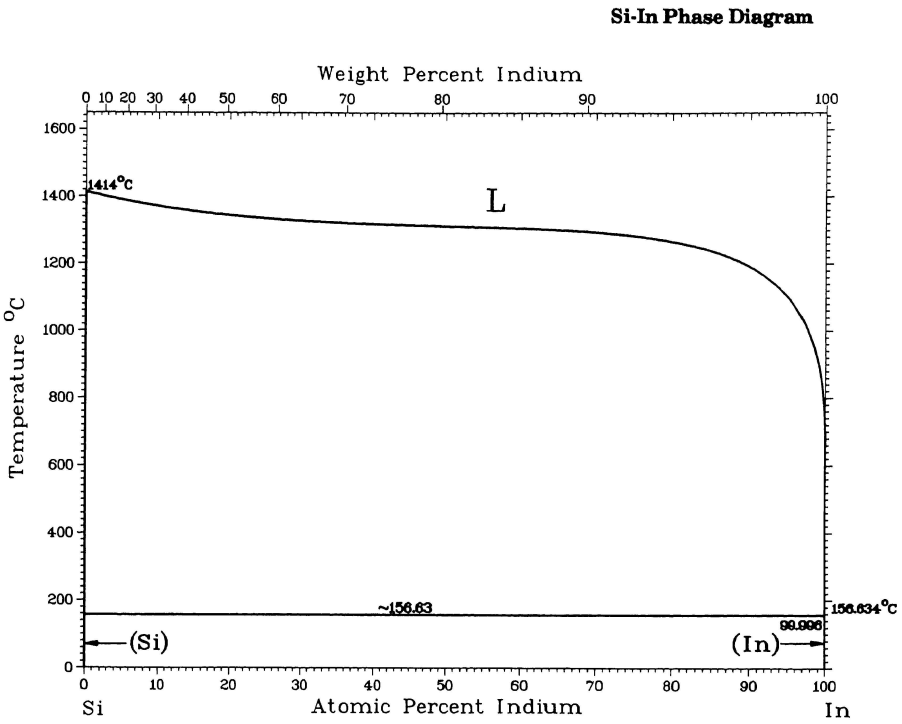

Figure A.6: In-Si phase diagram [Mas90b], Fig. 1.9(a) magnified.

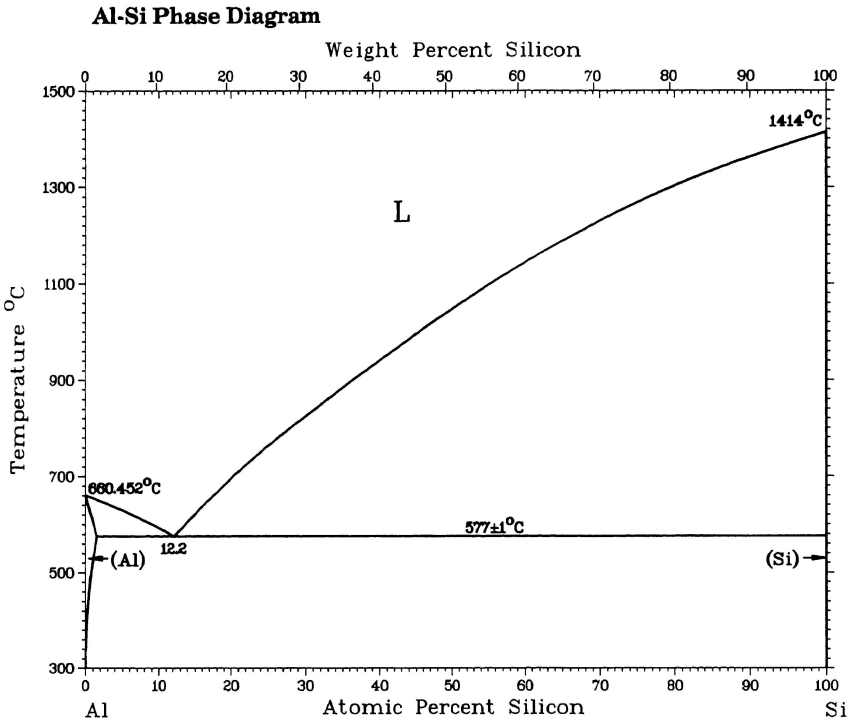

Figure A.7: Al-Si phase diagram [Mas90a], Fig. 1.10(a) magnified.

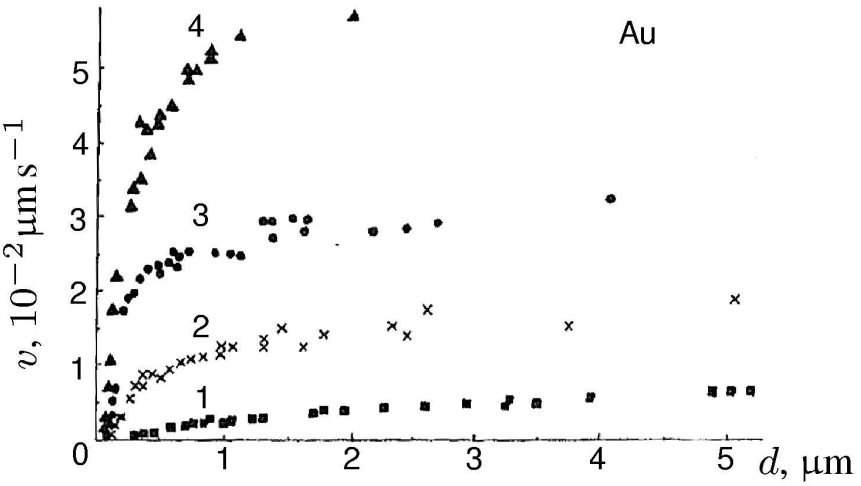

Figure A.8: Diameter dependence of the growth velocity; all experiments performed with $SiCl_4$ as precursor. Growth velocity v as a function of the wire diameter d; $SiCl_4$ pressure increases from 1 to 4; after [Giv75], Fig. 2.2(a) magnified.

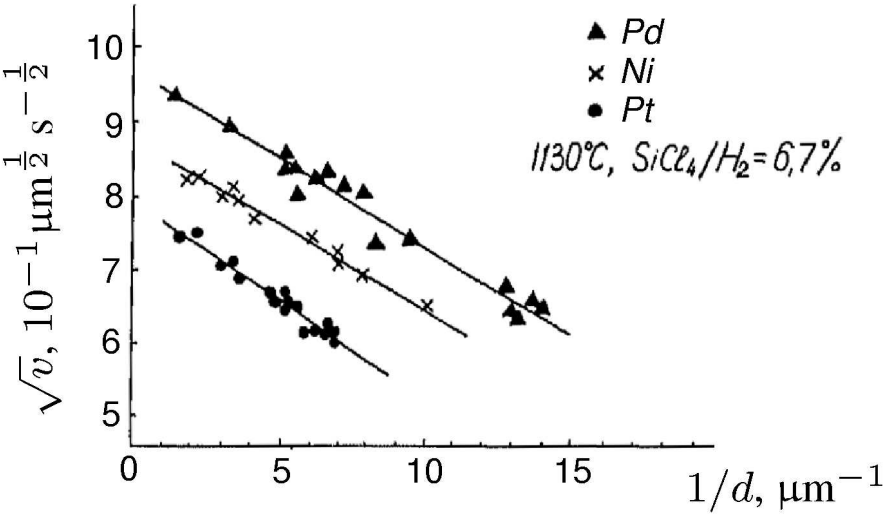

Figure A.9: Diameter dependence of the growth velocity; all experiments performed with $SiCl_4$ as precursor. $\sqrt{v}$ as a function of the inverse wire diameter $1/d$; after [Giv75], Fig. 2.2(b) magnified.

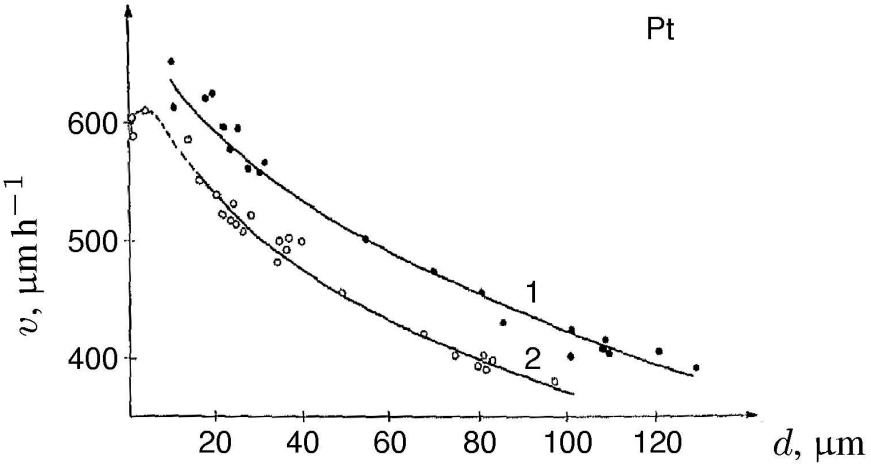

Figure A.10: Diameter dependence of the growth velocity; all experiments performed with $SiCl_4$ as precursor. v as a function of d; temperature $1000\,°C$ to $1100\,°C$; 1) $SiCl_4$:H_2 $= 0.9\%$ 2) $SiCl_4$:H_2 $= 0.95\%$; after [Wey78], Fig. 2.2(c) magnified.

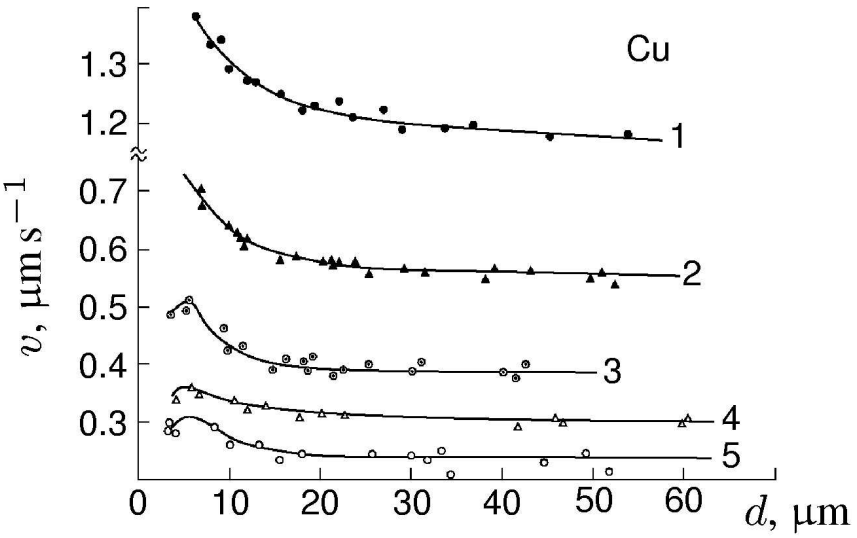

Figure A.11: Diameter dependence of the growth velocity; all experiments performed with $SiCl_4$ as precursor. v as a function of d; temperature: 1) $1027\,°C$, 2) $1047\,°C$, 3) $1067\,°C$, 4) $1087\,°C$, 5) $1107\,°C$; after [Neb05], Fig. 2.2(d) magnified.

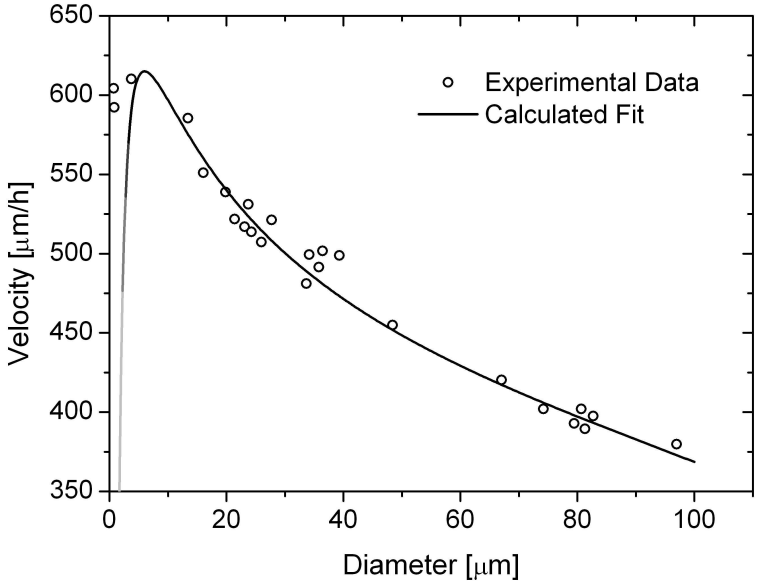

Figure A.12: Dataset Nº 2 of Fig. 2.2(c) after Weyher [Wey78] and calculated fit using equation (2.15) and the following parameters: $C^s = 30\,\mathrm{J mol^{-1}}\,\mu\mathrm{m}$, $r_o = 3\,\mu\mathrm{m}$, $v_o = 615\,\mu\mathrm{m\,h^{-1}}$, $\omega_1 = 33.6\,\mu\mathrm{m\,h^{-1}\,mol\,J^{-1}}$, $\alpha_2 = -0.88\,\mu\mathrm{m\,h^{-1}\,mol^2\,J^{-2}}$, Fig. 2.5 magnified.

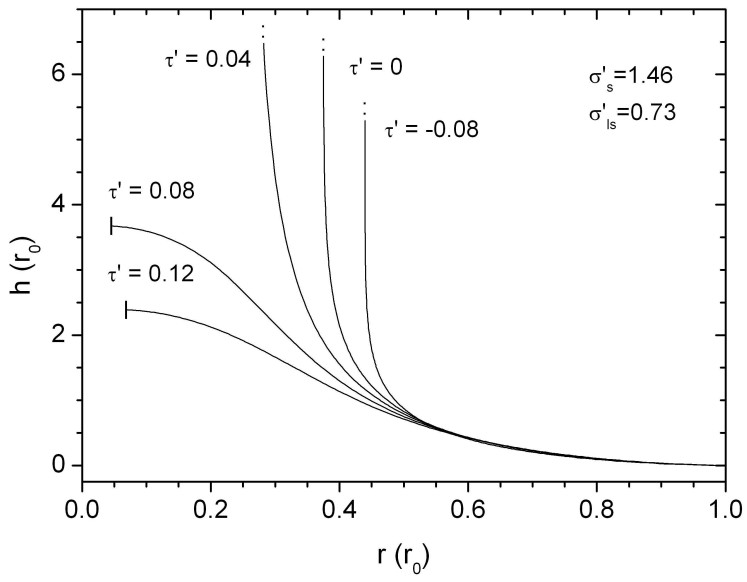

Figure A.13: Silicon nanowire shape for various line tension values τ', Fig. 3.4(a) magnified.

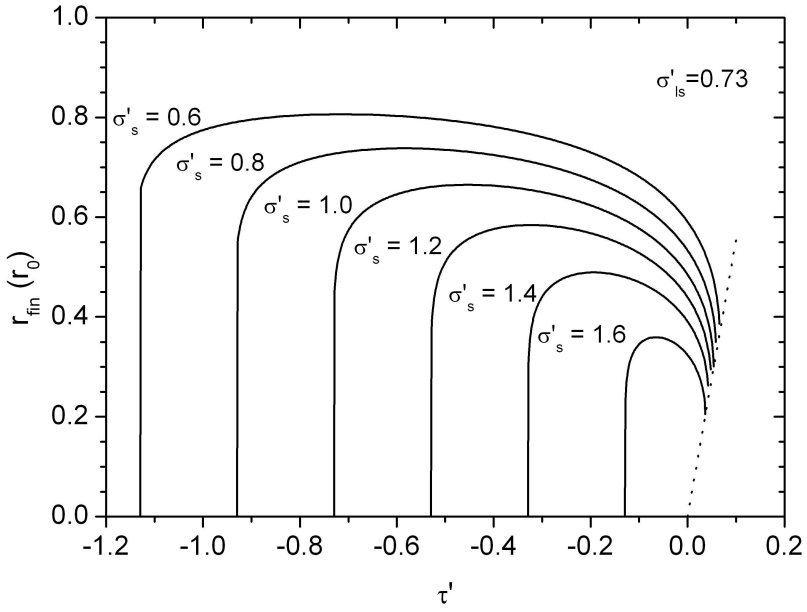

Figure A.14: Final nanowire radius r_{fin} as a function of the line tension τ' for $\sigma'_{ls} = 0.73$ and various σ'_s values, Fig. 3.6(a) magnified.

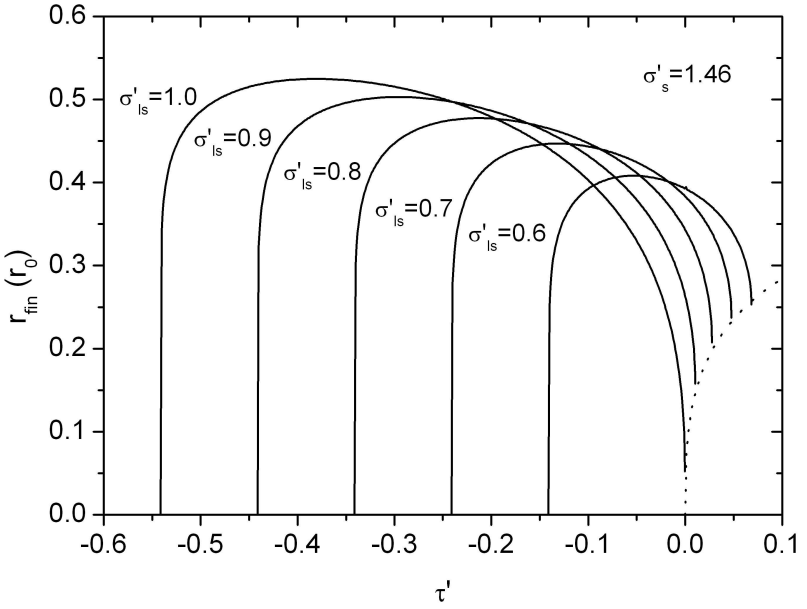

Figure A.15: Final nanowire radius r_{fin} as a function of the line tension τ' for $\sigma'_s = 1.46$ and various σ'_{ls} values, Fig. 3.6(b) magnified.

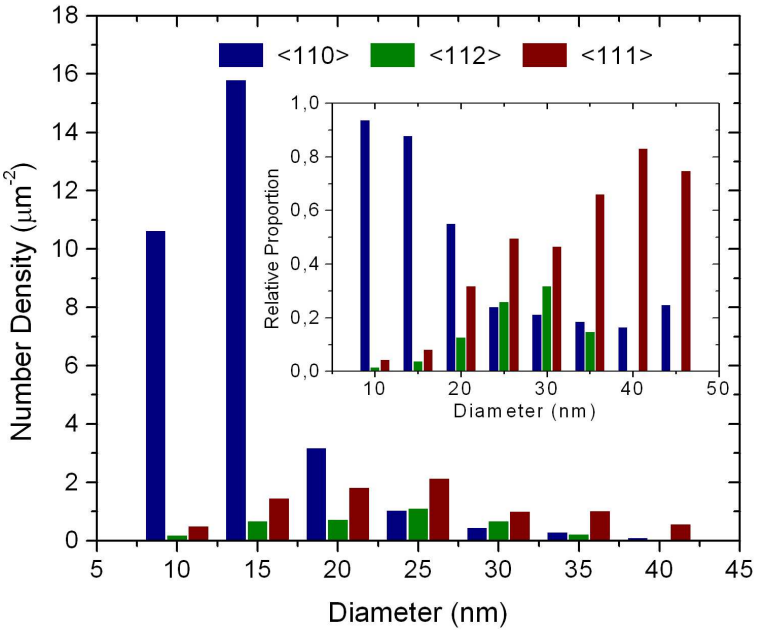

Figure A.16: Number density versus diameter for different growth directions. Inset: relative proportion of the different growth directions, Fig. 4.3 magnified.

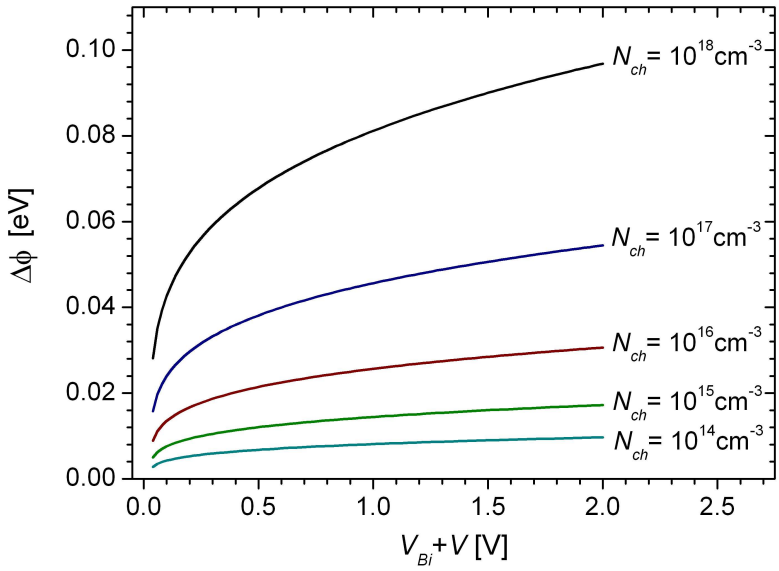

Figure A.17: Schottky barrier lowering $\Delta\phi$ as a function of $V_{Bi}+V$ at room temperature, Fig.5.2(b) magnified.

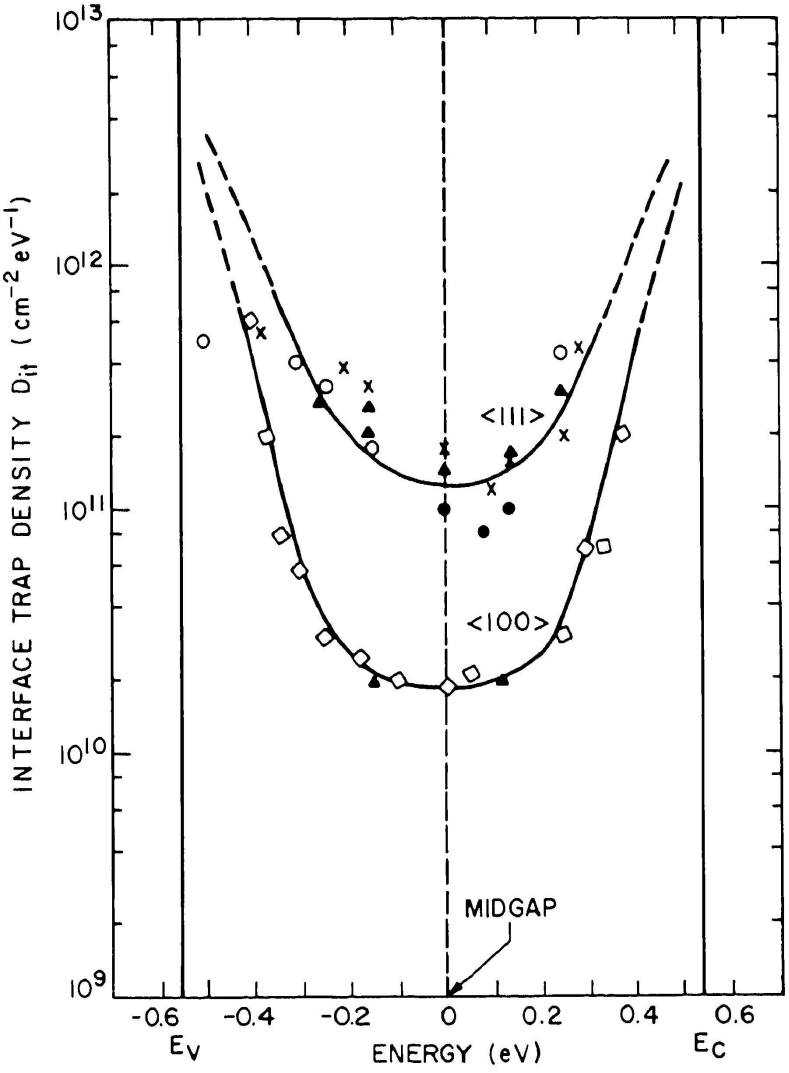

Figure A.18: (a) Density of interface traps for silicon (100) and (111) [Sze81e] after [Whi72], Fig. 5.3(a) magnified.

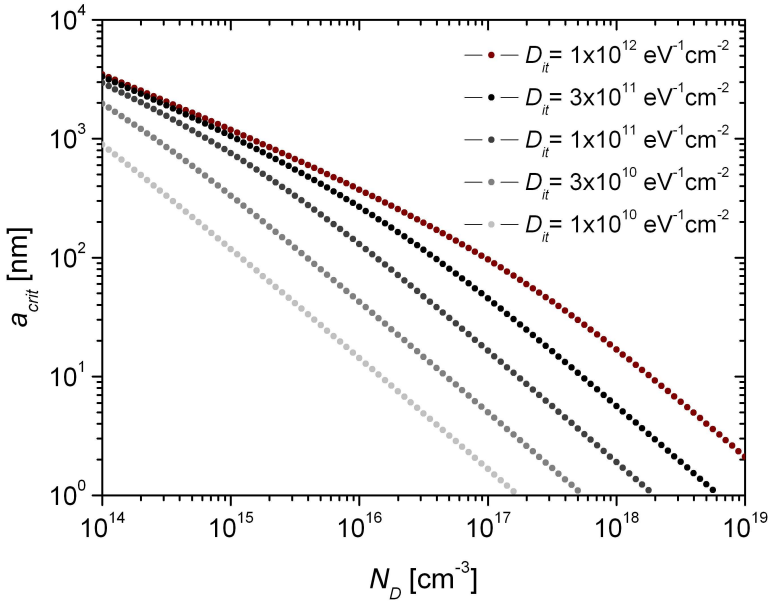

Figure A.19: Critical radius a_{crit} for different interface trap level densities D_{it} as a function of the donor concentration N_D; $Q_f = 0$, Fig. 5.4(a) magnified.

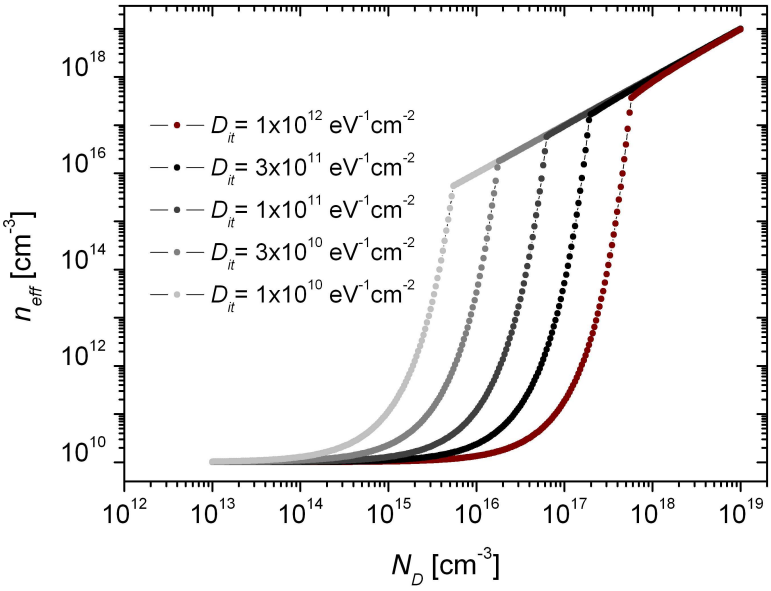

Figure A.20: Effective electron densities n_{eff} for different values of D_{it}, assuming $Q_f = 0$ and $a = 25$ nm, Fig. 5.4(b) magnified.

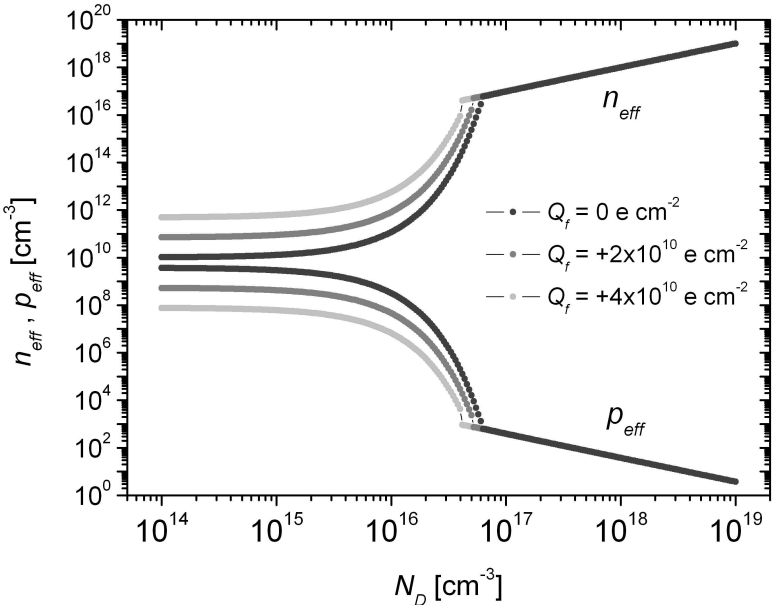

Figure A.21: Effective electron and hole density, n_{eff} and p_{eff}, as a function of N_D for $a = 25\,\text{nm}$, $D_{it} = 1\times10^{11}\,\text{eV}^{-1}\,\text{cm}^{-2}$ and different values of $Q_f \geq 0$, Fig. 5.4(c) magnified.

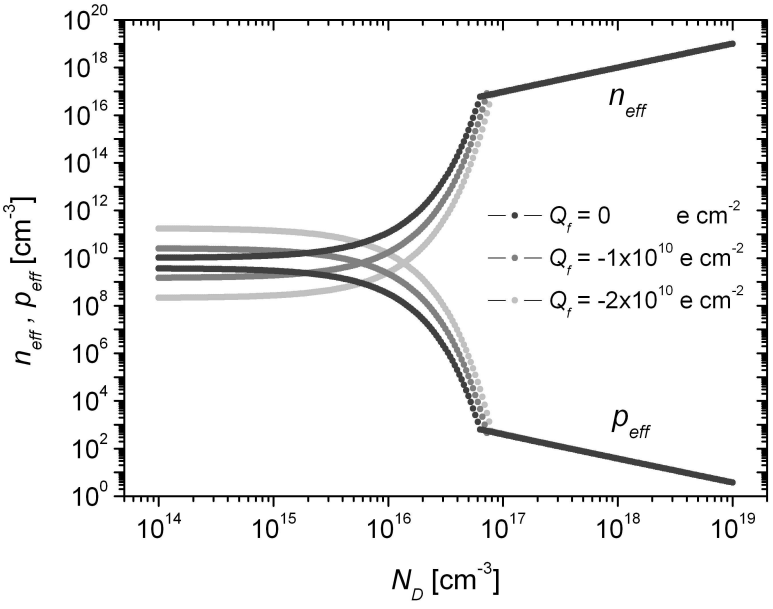

Figure A.22: n_{eff} and p_{eff} as a function of N_D for $a = 25\,\text{nm}$, $D_{it} = 1\times10^{11}\,\text{eV}^{-1}\,\text{cm}^{-2}$ and different values of $Q_f \leq 0$, Fig. 5.4(d) magnified.

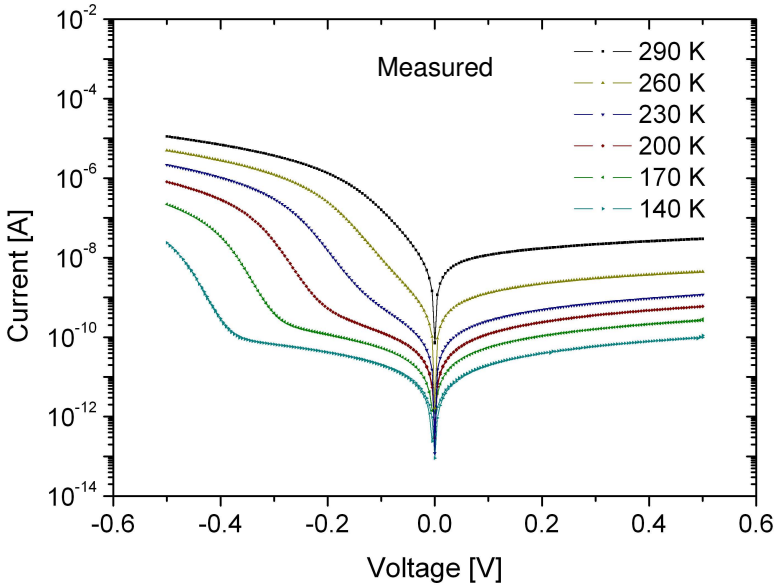

Figure A.23: Temperature dependent current-voltage measurement of an array of n-doped silicon nanowires, Fig. 5.6(a) magnified.

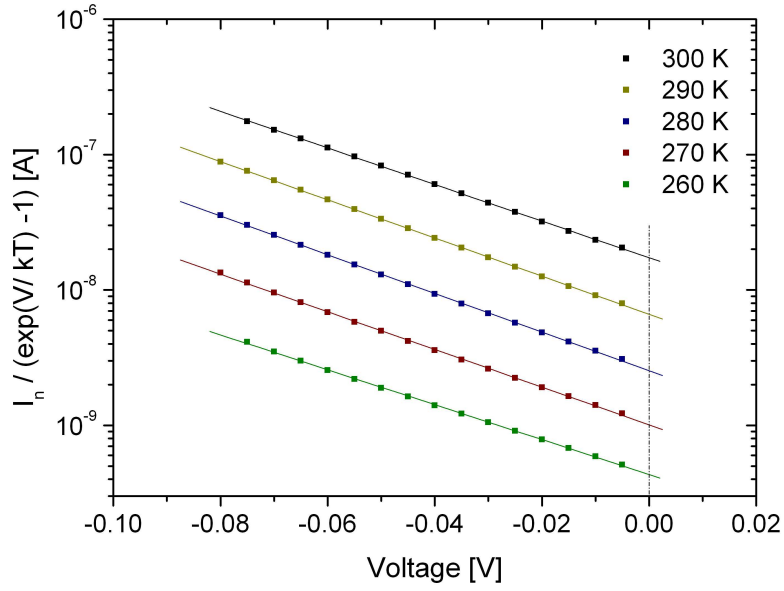

Figure A.24: $I_n/(\exp\left(\frac{qV}{kT}\right)-1)$ versus voltage for determination of n and I_s, Fig. 5.7(a) magnified.

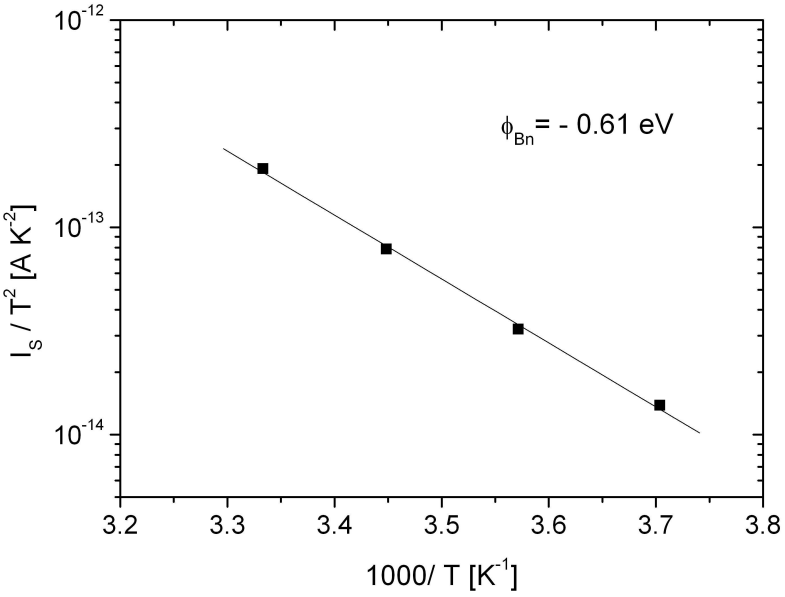

Figure A.25: Richardson plot for determination of the Schottky barrier height, Fig.5.7(b) magnified.

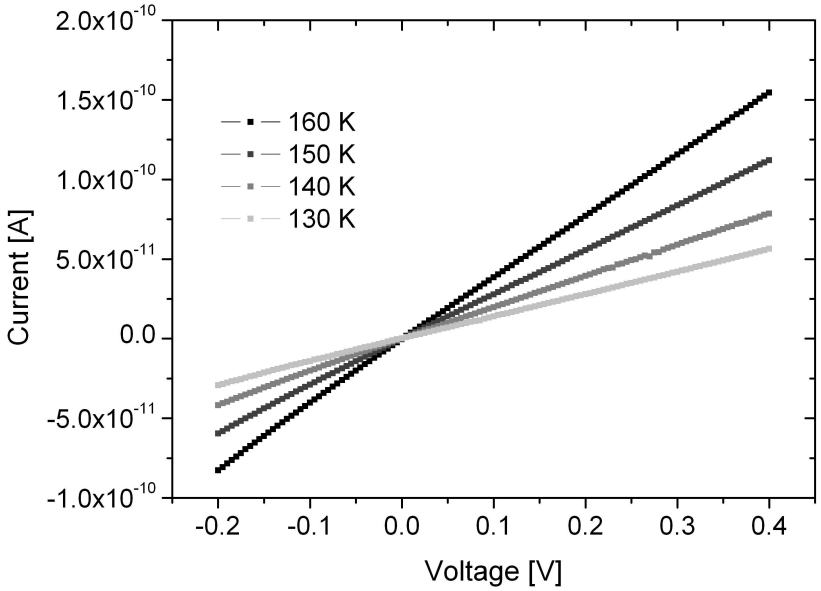

Figure A.26: Current-voltage characteristics for low temperatures on a linear scale, Fig. 5.8(a) magnified.

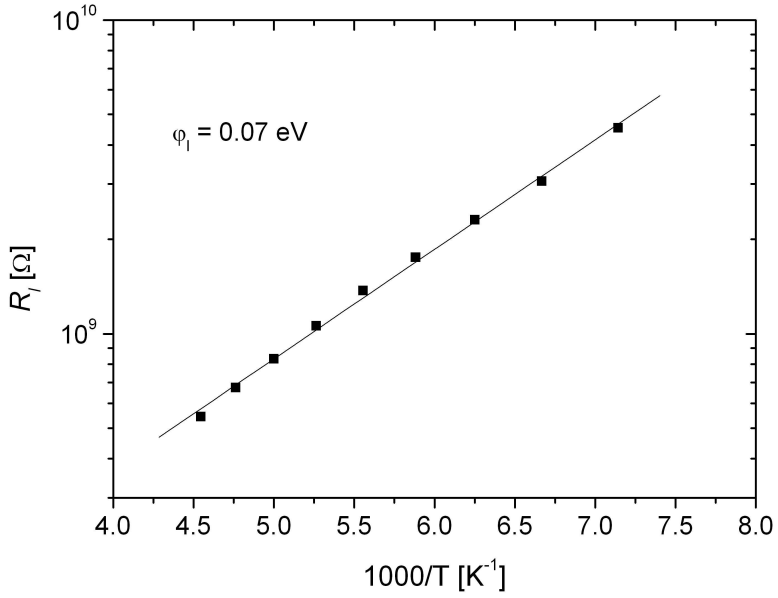

Figure A.27: Temperature dependence of the leak-resistance R_l, Fig. 5.8(b) magnified.

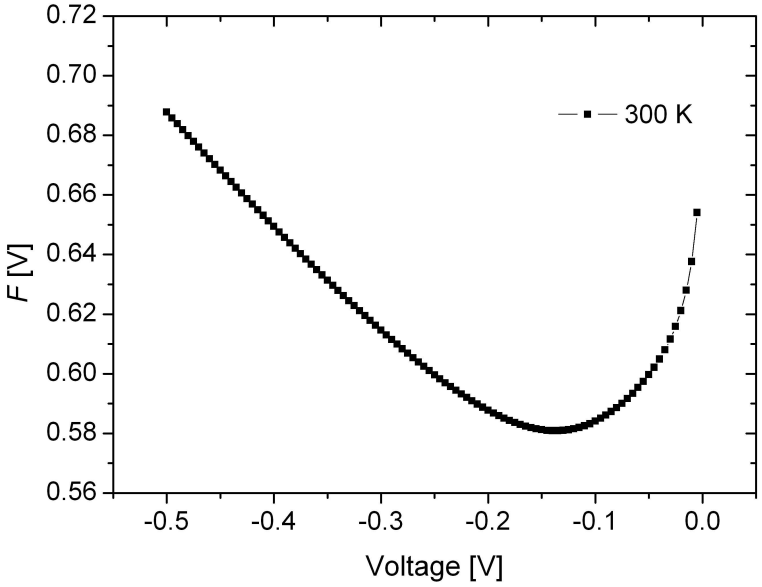

Figure A.28: Norde Plot of the forward current, Fig. 5.8(c) magnified.

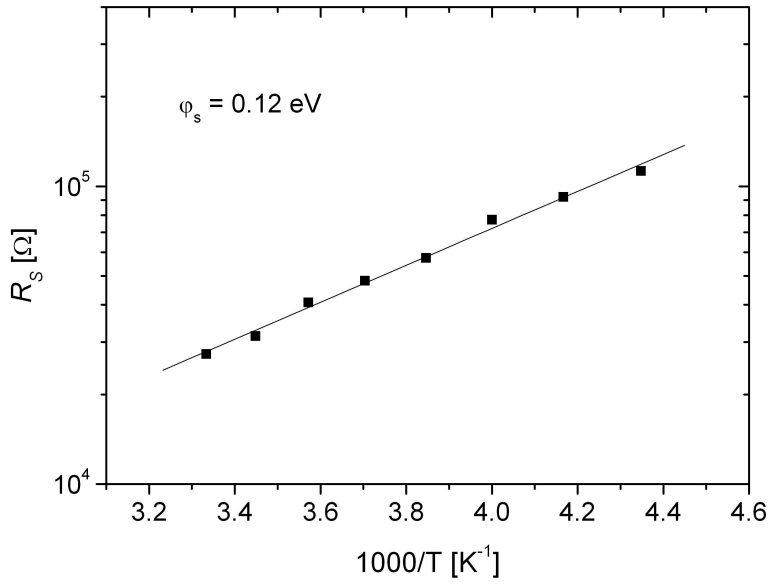

Figure A.29: Temperature dependence of the series resistance R_s, Fig. 5.8(d) magnified.

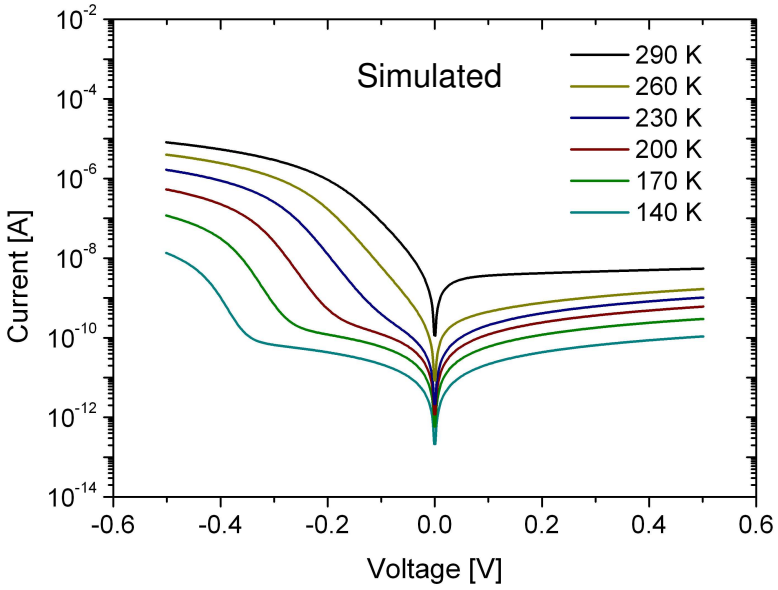

Figure A.30: Simulation of the measurement using the parameters extracted from Fig. A.23, Fig. 5.9(b) magnified.

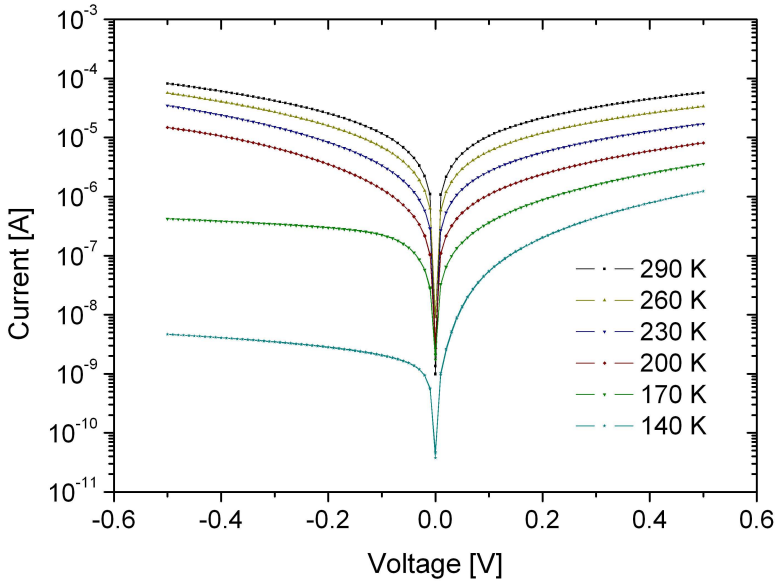

Figure A.31: Temperature dependent current-voltage measurement of an array of p-doped silicon nanowires, Fig. 5.11(b) magnified.

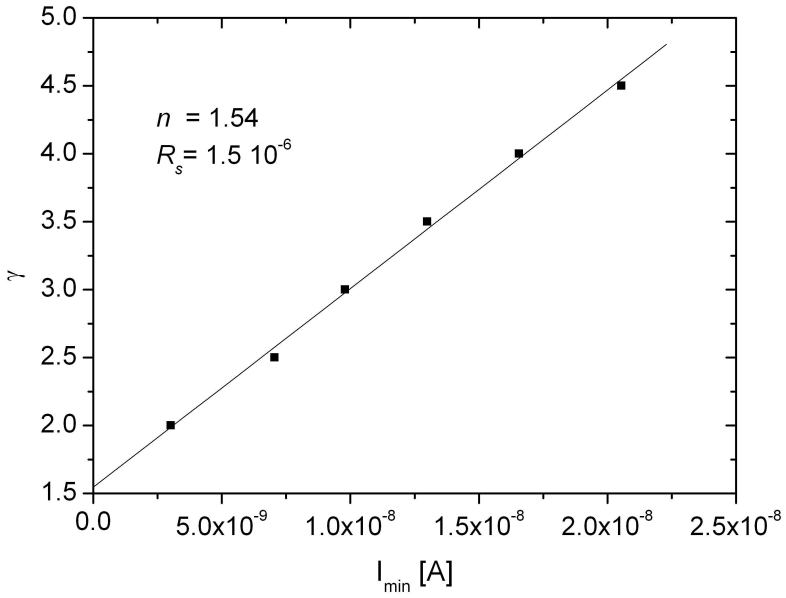

Figure A.32: γ as a function of I_{min}, Fig. 5.12(a) magnified.

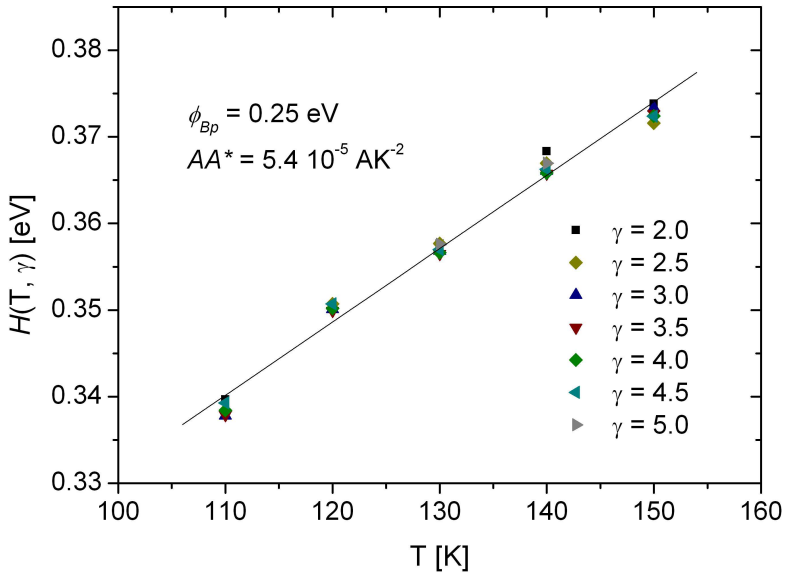

Figure A.33: $H(T, \gamma)$ as a function of the inverse temperature, Fig. 5.12(b) magnified.

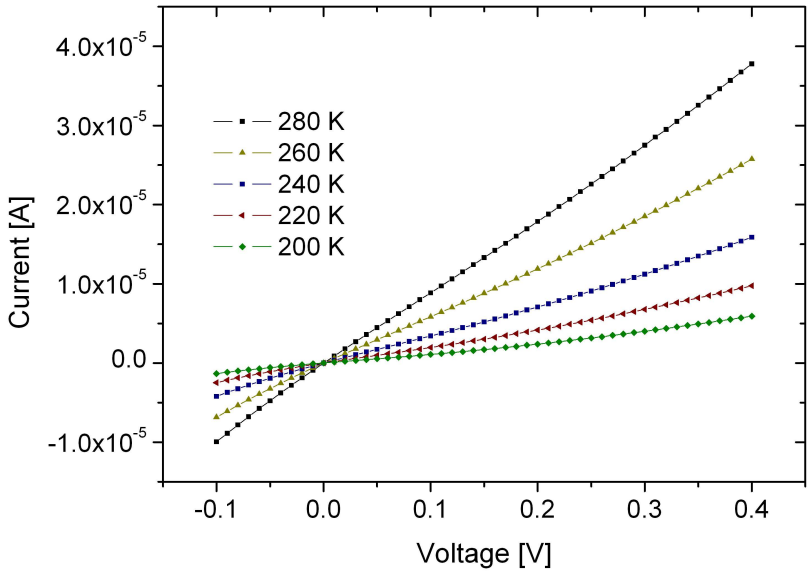

Figure A.34: Linear current-voltage relation at elevated temperatures, Fig. 5.12(c) magnified.

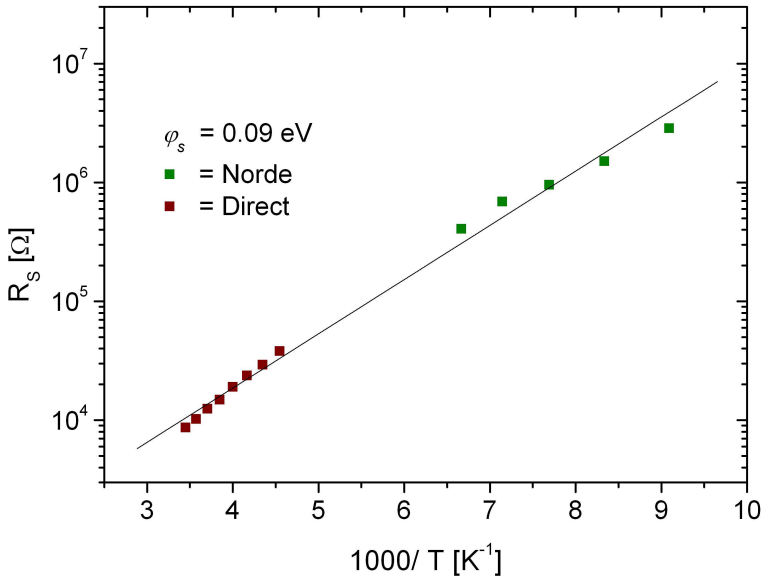

Figure A.35: Arrhenius plot of the series resistance, Fig. 5.12(d) magnified.

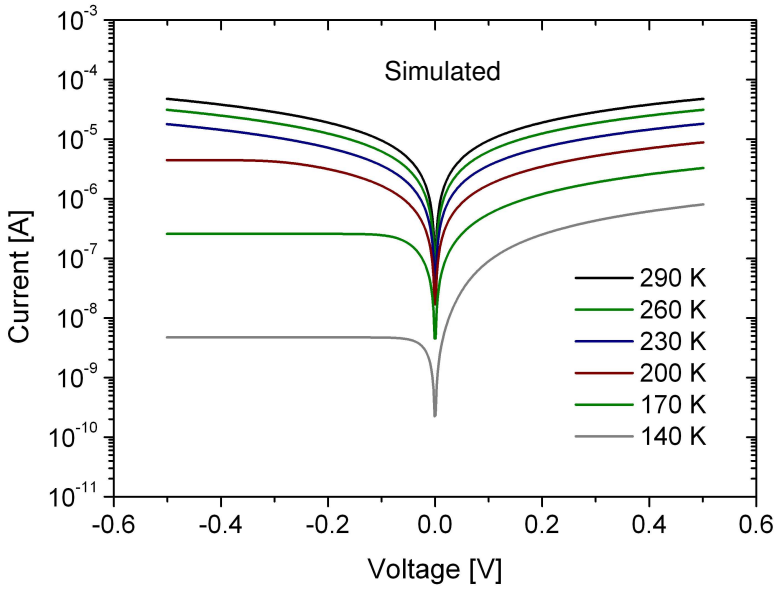

Figure A.36: Simulation of the measurement using the parameters extracted from Fig. A.31, Fig. 5.13(b) magnified.

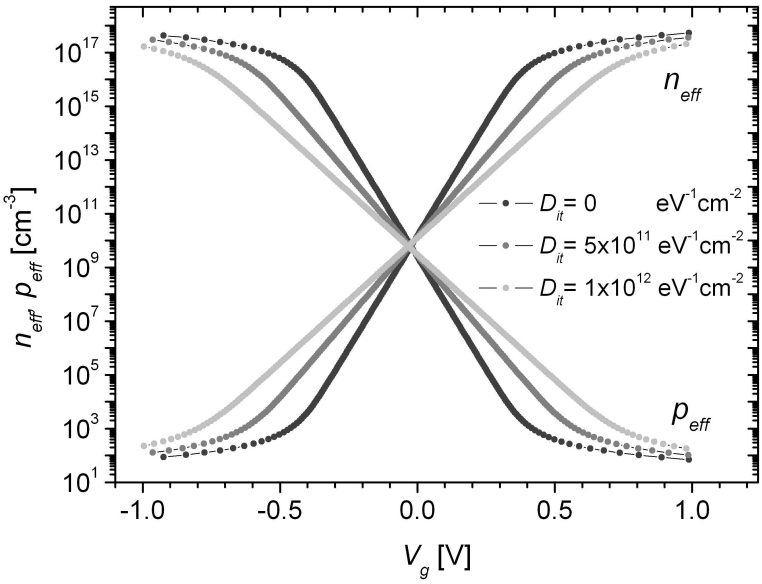

Figure A.37: Effective electron and hole density of an n-doped ($N_D = 1 \times 10^{16}\,\mathrm{cm}^{-3}$) circular surround-gate MOS capacitor for different interface trap level densities D_{it} as a function of the gate voltage V_g, Fig. 6.2(b) magnified.

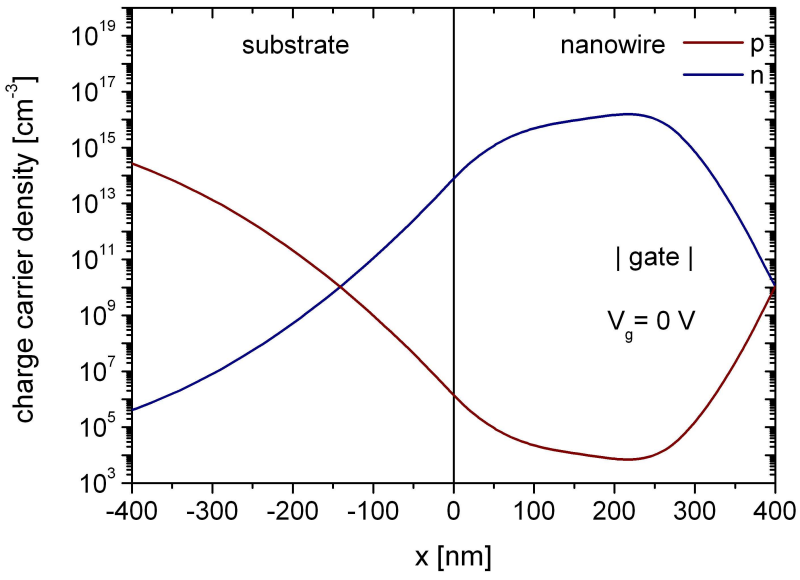

Figure A.38: $V_{DS} = 0\,\mathrm{V}$; charge carrier density for $V_g = 0\,\mathrm{V}$, Fig. 6.3(a) magnified.

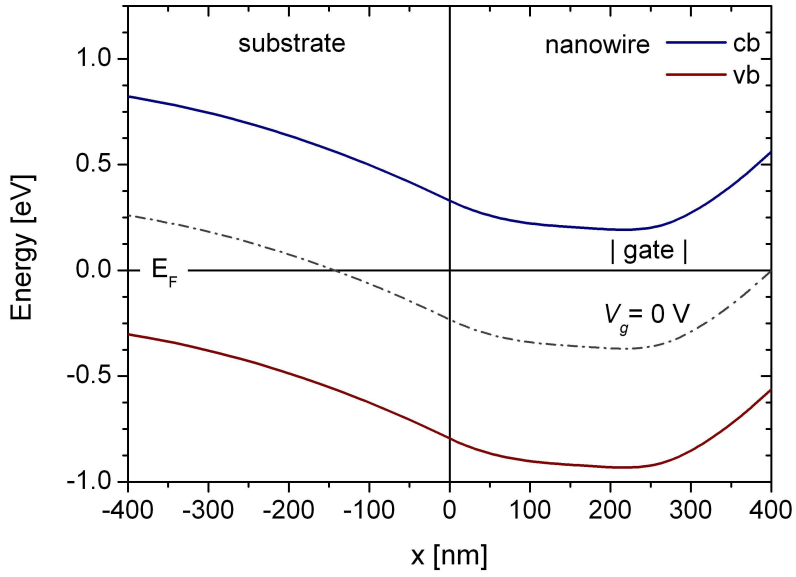

Figure A.39: $V_{DS} = 0\,\mathrm{V}$; bandstructure for $V_g = 0\,\mathrm{V}$, Fig. 6.3(b) magnified.

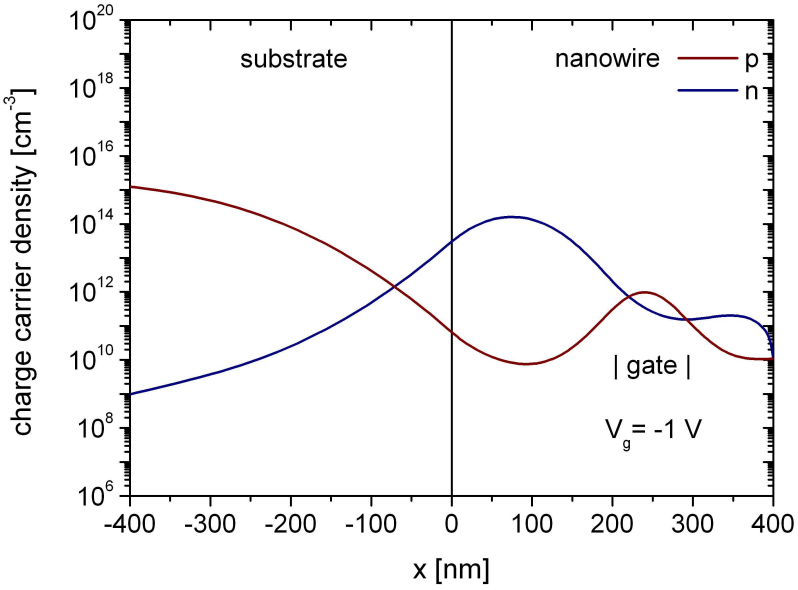

Figure A.40: $V_{DS} = 0\,\mathrm{V}$; charge carrier density for $V_g = -1\,\mathrm{V}$, Fig. 6.3(c) magnified.

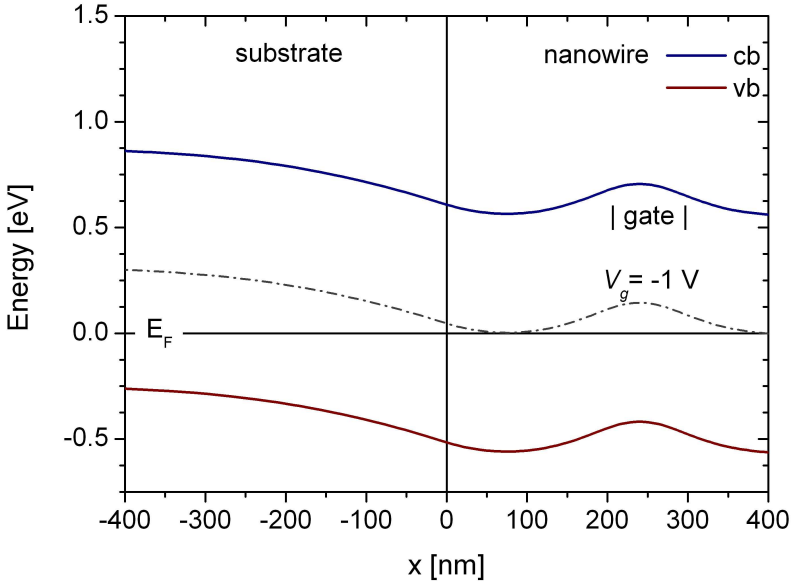

Figure A.41: $V_{DS} = 0$ V; bandstructure for $V_g = -1$ V, Fig. 6.3(d) magnified.

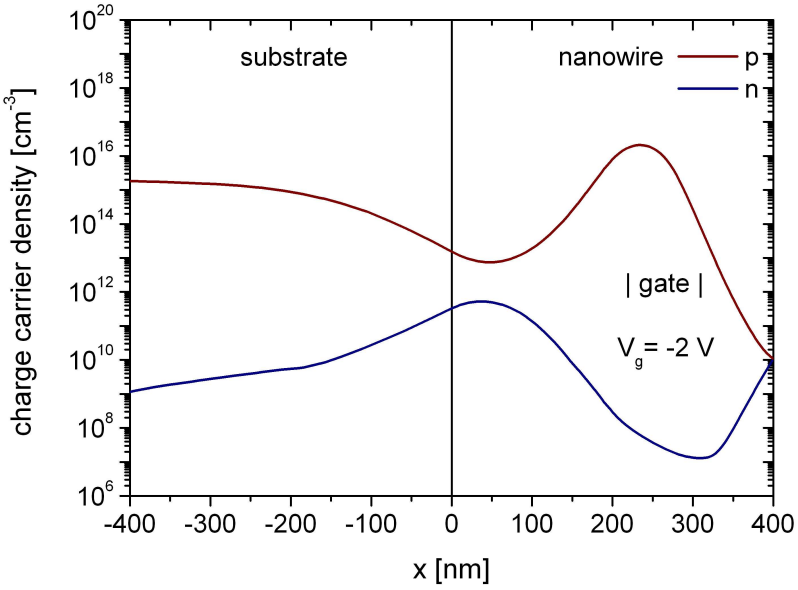

Figure A.42: $V_{DS} = 0$ V; charge carrier density for $V_g = -2$ V, Fig. 6.3(e) magnified.

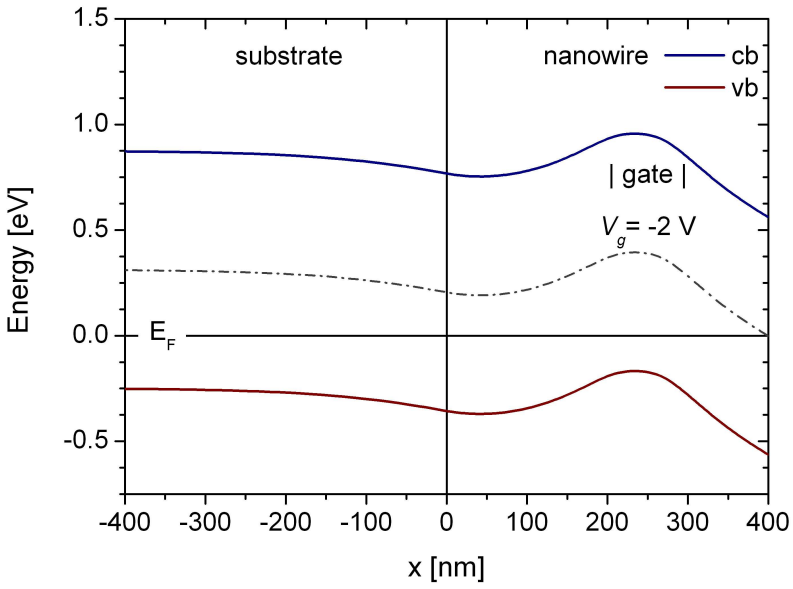

Figure A.43: $V_{DS} = 0$ V; bandstructure for $V_g = -2$ V, Fig. 6.3(f) magnified.

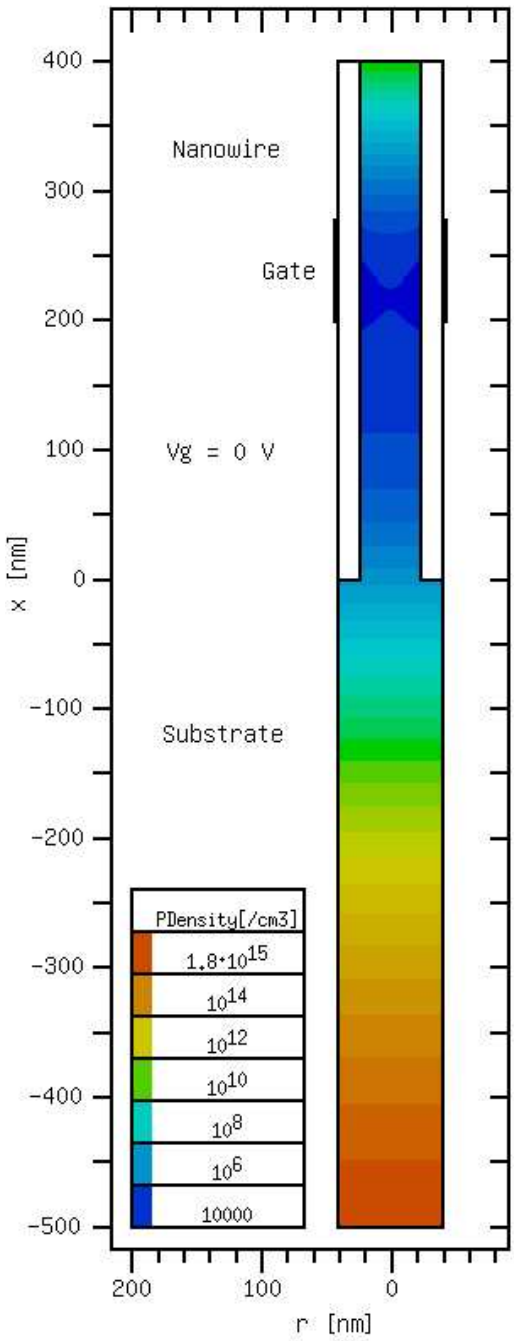

Figure A.44: $V_{DS} = 0$ V. (a) Charge carrier density for $V_g = 0$ V, Fig. 6.4(a) magnified.

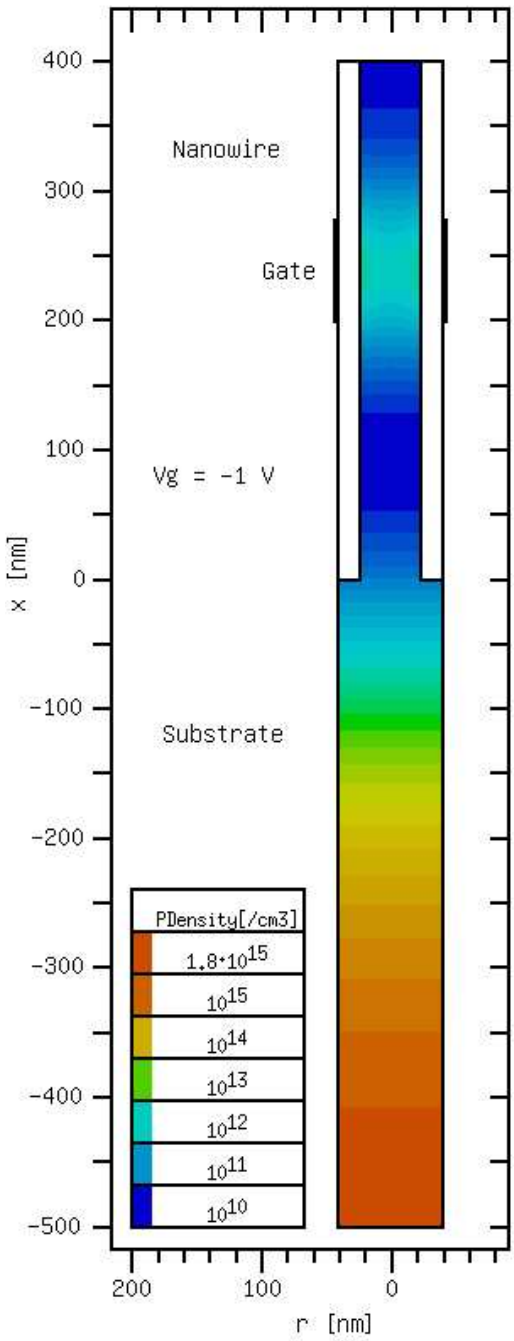

Figure A.45: $V_{DS} = 0$ V. (a) Charge carrier density for $V_g = -1$ V, Fig. 6.4(b) magnified.

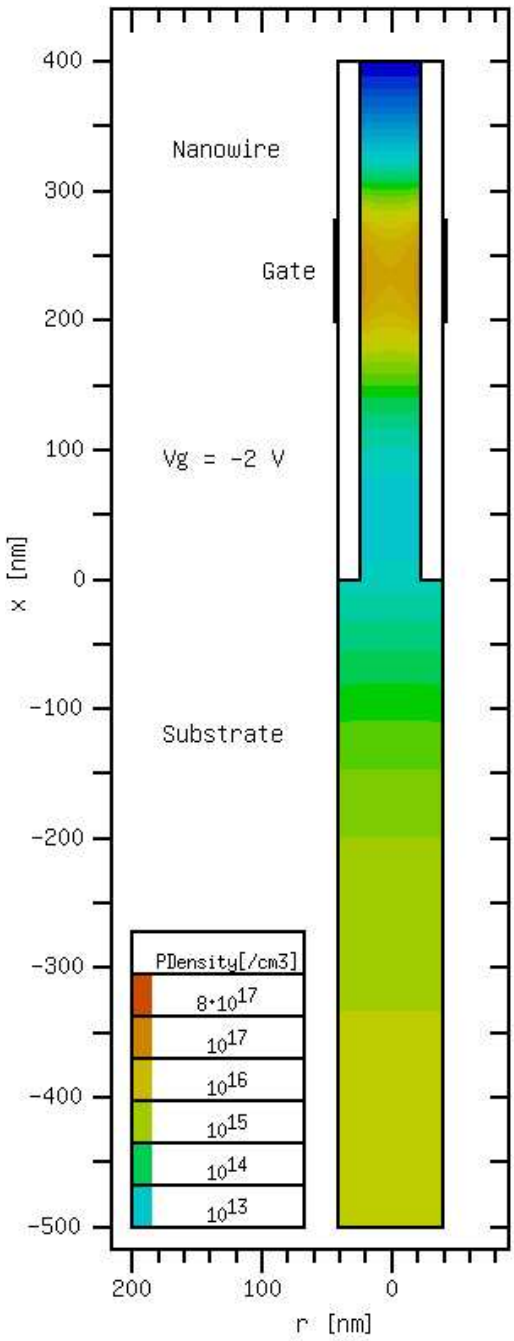

Figure A.46: $V_{DS} = 0\,\text{V}$. (a) Charge carrier density for $V_g = -2\,\text{V}$, Fig. 6.4(c) magnified.

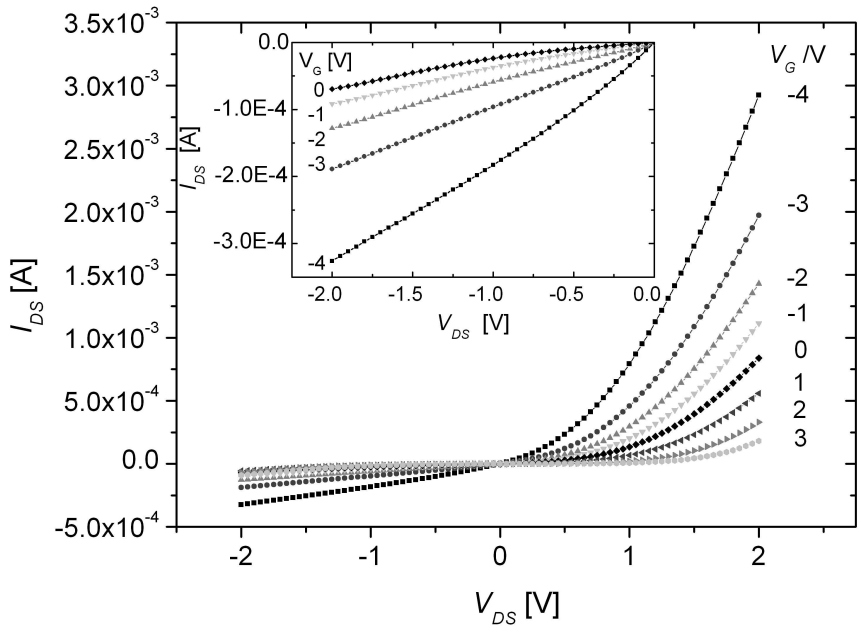

Figure A.47: Output characteristics of an array of VS-FETs for different gate voltages, Fig. 6.8(a) magnified.

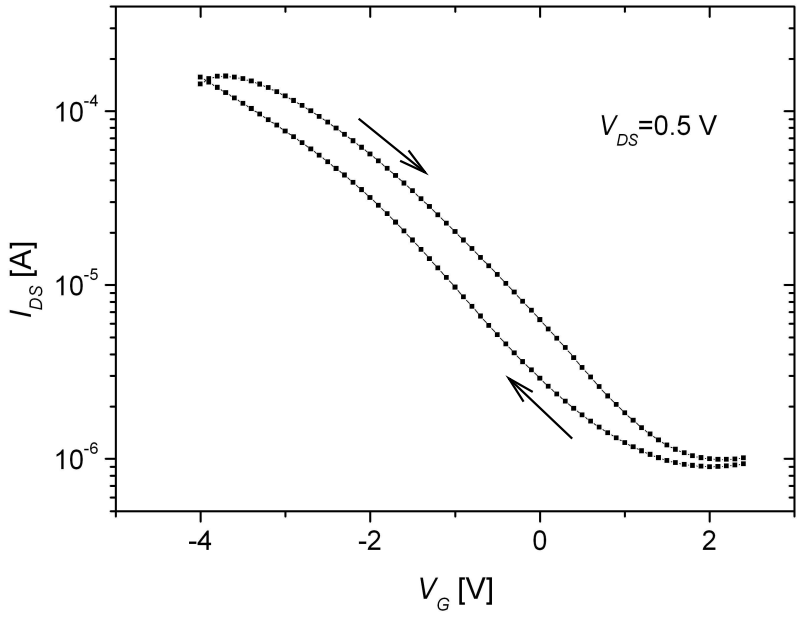

Figure A.48: Drain-source current I_{DS} vs. gate voltage V_G for $V_{DS} = 0.5$ V, Fig. 6.8(b) magnified.

Acknowledgement

First of all, I would like to express my gratitude to Prof. U. Gösele for his confidence and his support I experienced in the last three years. I tried my best to reward it. Yet, my work would not have been successful without the knowledge and support of my supervisor Dr. S. Senz. He is a great experimentalist. Besides, he also took responsibility for the transmission electron microscope investigations. I also want to thank Dr. habil. W. Riess, Dr. H. Riel, Dr. S. Karg, H. Schmid, and U. Drexler for their hospitality and their help during my four months stay at the IBM Zurich research lab. This, without doubt, strongly facilitated the realization of the silicon nanowire surround-gate field-effect transistor. I am also indebted to Dr. W. Erfurth and Mrs. U. Doss for their efforts in contacting single nanowires with the help of the e-beam lithography, to Dr. A. Graff for taking some of the transistor images, to Mrs. S. Swatek for the numerous transmission electron microscope samples she prepared for us, to Dr. D. Hesse for the proof-reading, and to many others who helped in one way or the other but are not mentioned here by name.

Publikationsliste

1) Measurement of the Bending Strength of Vapor-Liquid-Solid Grown Silicon Nanowires
S. Hoffmann, I. Utke, B. Moser, J. Michler, S. H. Christiansen, V. Schmidt, S. Senz, P. Werner, U. Gösele, C. Ballif, *Nano Lett.* 6(4), 622-625 (2006).

2) Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effect Transistor
V. Schmidt, H. Riel, S. Senz, S. Karg, W. Riess, U. Gösele, *Small* 2(1), 85-88, (2005).

3) Diameter-Dependent Growth Direction of Epitaxial Silicon Nanowires
V. Schmidt, S. Senz, U. Gösele, *Nano Lett.*, 5(5), 931-935, (2005).

4) The Shape of Epitaxially Grown Silicon Nanowires and the Influence of Line Tension
V. Schmidt, S. Senz, U. Gösele, *Appl. Phys. A*, 80(3), 445-450, (2005).

5) UHV Chemical Vapour Deposition of Silicon Nanowires
V. Schmidt, S. Senz, U. Gösele, *Z. Metallk.*, 96(5), 427-428, (2005).

Zusammenfassung

Diese Arbeit befasst sich mit der Synthese von Siliziumnanodrähten, verschiedenen fundamentalen Aspekten des Wachstums von Siliziumnanodrähten und der Herstellung eines ersten Bauteils basierend auf Siliziumnanodrähten.

In Kapitel 1 wird die experimentelle Herstellung von mittels des Vapor-Liquid-Solid (VLS) Mechanismus und unter Verwendung von Gold als Katalysator epitaktisch auf Siliziumsubstraten gewachsenen Siliziumnanodrähten demonstriert und im Detail beschrieben. Da die Verwendung von Gold als Katalysator jedoch zumeist als unvereinbar mit industriellen Halbleiterfertigungsmethoden angesehen wird, ist speziell in Hinblick auf die mögliche Anwendung von Siliziumnanodrähten in integrierten Schaltkreisen der Austauch von Gold durch einen alternativen Katalysator von großem Interesse. Sechs verschiedene Materialien (Palladium, Eisen, Dysprosium, Wismut, Indium und Aluminium) wurden auf ihre Verwendbarkeit als alternative Katalysatoren hin getestet. Die Ergebnisse werden in Kapitel 1 diskutiert.

Die drei darauf folgenden Kapitel befassen sich mit jeweils einem spezifischen Aspekt der Synthese von Siliziumnanodrähten. In Kapitel 2 wird die Abhängigkeit der Wachstumsgeschwindigkeit vom Nanodrahtdurchmesser untersucht. Dies ist von grundlegender Bedeutung, da die Länge der Siliziumnanodrähte gewöhnlich über die Wachstumsdauer eingestellt wird, was ein Verständnis der Faktoren, die die Wachstumsgeschwindigkeit bestimmen, voraussetzt. Bezüglich der Abhängigkeit der Wachstumsgeschwindigkeit vom Durchmesser wurden von verschiedenen Gruppen unterschiedliche, scheinbar widersprüchliche Beobachtungen gemacht. In Kapitel 2 wird ein Modell abgeleitet, das, stationäres Wachstum voraussetzend, das Wechselspiel zweier Unterprozesse des VLS Mechanismus berücksichtigt. Im Rahmen dieses Modells können die scheinbar widersprüchlichen Beobachtungen schlüssig erklärt werden. Darüber hinaus liefert das Modell eine Erklärung für den beobachteten Zusammenhang zwischen der Druckabhängigkeit und der Durchmesserabhängigkeit der Wachstumsgeschwindigkeit.

Kapitel 3 befasst sich mit der Durchmesservergrößerung von epitaktisch gewachsenen Siliziumnanodrähten an der Stelle, wo diese mit dem Substrat verbunden sind. Diese Verbreiterung der Nanodrähte kann auf eine Änderung des Kontaktwinkels des Katalysatortropfens in der initialen Wachstumsphase zurückgeführt werden. In Kapitel 3 wird ein Modell zur quantitativen Beschreibung der Durchmesservergrößerung abgeleitet, dass die Gleichgewichtsform des Katalysatortropfens in Beziehung zur jeweiligen Nanodrahtgeometrie und zur Balance zwischen Oberflächenspannungen und Linienspannung setzt.

Ein Vergleich der experimentell beobachteten Form der Verbreiterung mit den Ergebnissen aus der Modellrechnung erlaubt Rückschlüsse auf die Grösse der Linienspannung. Darüber hinaus ergeben sich als Ergebnis der Modellrechnung, abhängig von Größe und Vorzeichen der Linienspannung, zwei unterschiedliche Wachstumsmoden.

Kapitel 4 befasst sich mit der kristallographischen Wachstumsrichtung der Siliziumnanodrähte, einem Parameter der speziell für epitaktisch gewachsene Nanodrähte von großer Bedeutung ist. Interessanterweise zeigt sich aus experimentellen Beobachtungen, dass die Wachstumsrichtung vom Durchmesser der Nanodrähte abhängt. Ein Modell wird postuliert, demzufolge die Änderung der Nanodraht-Wachstumrichtung auf das Wechselspiel zwischen der Oberflächenspannung und der Au/Si Grenzflächenspannung der Nanodrähte und das unterschiedliche Skalierungsverhalten der beiden Parameter zurückgeführt werden kann.

Im Anschluss an diese teilweise theoretischen Betrachtungen zur Morphologie befasst sich Kapitel 5 mit den elektrischen Eigenschaften von dotierten Siliziumnanodrähten. Es werden temperaturabhängige Messungen präsentiert und im Detail diskutiert. Es zeigt sich, dass die Drähte zwar ein aufgrund der Dotierung zu erwartendes Verhalten zeigen, dass jedoch die effektive Ladungsträgerkonzentration in den Siliziumnanodrähten überraschend gering ist. Dies kann vermutlich auf den Einfluss von Si/SiO_2 Grenzflächenzuständen an der Außenhaut der Nanodrähte zurückgeführt werden. Um dies aufzuzeigen wird ein allgemeines Modell zum Einfluss von Si/SiO_2 Grenzflächenzuständen und Grenzflächenladungen auf die effektive Ladungsträgerkonzentration in Siliziumnanodrähten abgeleitet.

Zuletzt wird in Kapitel 6 die Herstellung eines Feldeffekt-Transistors basierend auf epitaktisch gewachsenen und dotierten Siliziumnanodrähten präsentriert. Hierbei ist besonders hervorzuheben, dass, im Gegensatz zur herkömmlichen planaren Anordnung, in unserem Fall das Transistor-Gate den vertikalen Nanodraht radial umschließt, was theoretisch eine bessere elektrostatische Kontrolle ermöglicht. Die Durchführbarkeit des vorgeschlagenen Herstellungsprozesses und die Funktionalität der auf diese Weise hergestellten Nanodraht-Transistoren wird durch elektrische Messungen demonstriert.

Lebenslauf

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Eidesstattliche Erklärung

Hiermit erkläre ich, dass ich meine Dissertation selbständig und ohne fremde Hilfe verfasst und keine anderen als die von mir angegebenen Quellen und Hilfsmittel zur Erstellung meiner Dissertation verwendet habe. Den benutzten Werken wörtlich oder inhaltlich entnommene Stellen sind als solche gekennzeichnet.

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